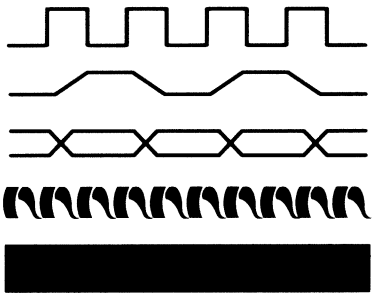
1990



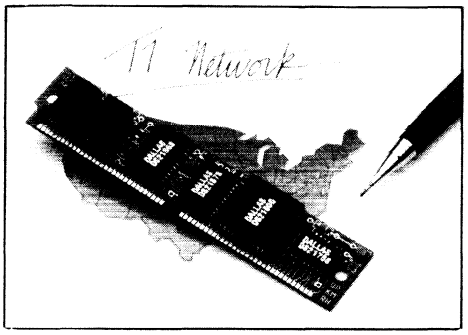
TELECOM

DATA BOOK

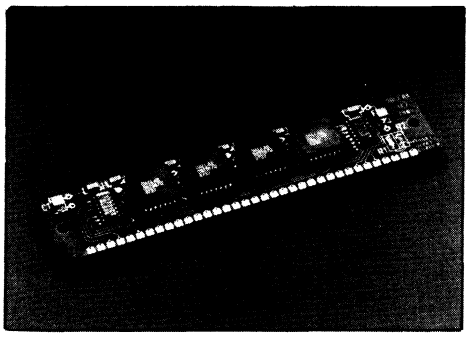
DALLAS SEMICONDUCTOR

SETTING DIGITAL COMMUNICATION TRENDS

Dallas Semiconductor has introduced chip sets that completely support the T1,CEPT and ADPCM standards. In addition, we offer subsystems called SipStiks™. These snap in subassemblies use JEDEC standard configurations recently made popular by DRAMs.Their low profile form factor achieves high functional density, yet offers advantages of modularity.



North American or European Short Loop Interface:
The DS2280 and DS2281 are complete T1 and CEPT Line Cards with transformers in less than 3 square inches. Both provide all of the interface circuitry necessary for digital telephone networks.



Multi-Channel Voice Compression:
The DS2264 and DS2268 offer 4 and 8 channel ADPCM processing in the same compact format. ADPCM increases the effective bandwidth of the digital telephone network by compressing and decompressing speech.

DALLAS
SEMICONDUCTOR

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GENERAL INFORMATION

1

CORPORATE FACT SHEET

Dallas Semiconductor designs, manufactures, and markets electronic chips and chip-based subsystems called Stiks™. Rather than build products that others have already made, the company concentrates on one-of-a-kind solutions that span many application areas. Through the use of late definition technologies, Soft Silicon™ chips can be tailored after they are made -- even during use.

Founded February 1, 1984, Dallas Semiconductor has a multiproduct strategy to serve the needs of a variety of industries. The company's seven development teams constantly attack unsolved problems and introduce new products to the marketplace.

In its six-year history, Dallas Semiconductor has shipped 97 base products, with over 500 distinct variations, to more than 6,000 customers worldwide. These include Original Equipment Manufacturers (OEMs) in instrumentation, factory automation, personal computers, office equipment, telecommunications, medical equipment, and mainframe computers.

Chips and subsystems are sold through a direct sales force, distributors and manufacturers' representatives worldwide. Sales for 1989 totaled $82 million; the company shipped over $23 million worth of products during the first quarter of 1990. As of March 19, 1990, the company is traded on the New York Stock Exchange under the symbol DS.

TECHNOLOGY

Dallas Semiconductor's special technologies make possible Soft Silicon™ solutions -- dynamic, flexible, chip-based products that can be molded in the final manufacturing stages or during use. Soft Silicon™ is made possible by the Late Definition technologies of lithium energy and direct laser writing.

Lithium

Using micro energy management techniques, Dallas Semiconductor has reduced power requirements to the point where a miniature lithium energy source powers products for the useful life of the equipment. Chips and Stiks are made virtually crashproof with minimum current design techniques and special freshness seals that keep lithium cells from expending any energy until power is applied for the first time. Through these technologies, Dallas products remember data throughout their operating life and can accept change.

Laser

Direct laser writing makes each chip unique at low cost. A sub-micron positioning laser and control software developed at Dallas can engrave individual chips with digital patterns. This ability to routinely alter, reconfigure, or program individual chips after completion of wafer fabrication broadens the application base of products having a similar design. Direct laser writing also allows Dallas Semiconductor to develop highly accurate products for applications where precision is paramount.

As a result of these Late Definition technologies, exact chip definition can be left to the OEM. Certain chips can even be defined and redefined by the end system itself.

MANUFACTURING AND FACILITIES

The Company occupies 184,000 square feet of facilities in north Dallas. This location includes a six-inch, submicron chip-making plant, one of the most sophisticated wafer production plants in the world. It features Class One cleanliness; automated wafer processing; dry etch using plasma techniques; and 0.15 micron direct step alignment tolerances. Automated modular process technology provides substantial flexibil-

ity in the manufacturing process and significantly reduces the number of people required for operation, thereby decreasing manufacturing costs. As an example, our pick and place machine assembles Stik subassemblies under computer control and can position up to 4,500 chips per hour. All products are shipped from Dallas after final quality assurance and testing.

MARKETING AND SALES

Dallas Semiconductor coordinates its selling activity from its Dallas, Texas headquarters. Twelve area sales managers call on OEM accounts and coordinate the activities of 46 sales representative offices in North America and 34 in Europe and Asia. Dallas Semiconductor also markets its products in North America through national and regional stocking distributors.

I'm interested. Who do I call?

* To order, call Credit Card Sales at 1-800-336-6933. You can order any Dallas Semiconductor product for next-day shipment with a Visa, MasterCard, or American Express.
* For technical information, call (214) 450-0448. We can answer questions or arrange for a local Dallas Semiconductor representative to call you.

You can also contact our nearest distributor, representative, or sales office.

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(317) 573-3999
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Lightwater Surrey, England
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(609) 235-1900
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(201) 515-3000
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(305) 428-8877
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Sweden
Commit Electronics AB
46-8732-6213
Switzerland
Kontron Electronics AG
41-1-435-4111
Taiwan
Landcol Enterprises, Ltd.
886-2-709-3515
Thailand
Dynamar Computer Products Co. Ltd.
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West Germany
Atlantik Elektronik GmbH
49-89-857-000
Astek Elektronik Vertriebs GmbH
49-4191-8007-0

PRODUCT OVERVIEW

Dallas Semiconductor designs and manufactures problem-solving products based on CMOS integrated circuits. Special Late Definition technologies make possible SoftSilicon™ solutions -- products that can be altered in the final manufacturing stages or during use. Dallas Semiconductor's growing product families of chips and SipStik Prefabs are outlined below.

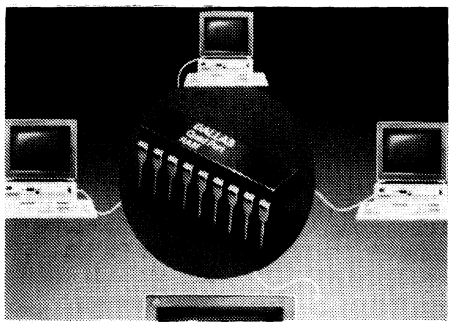
Silicon Timed Circuits

All-silicon time delay lines can withstand the high temperatures associated with surface mounting in small outline packages. They also offer better accuracy than the hybrid approach to delay lines. Standard values ranging from 3ns to 500ns are available from stock, or chips can be made to order. Laser writing techniques used to customize chips offer maximum flexibility from tailor-made products at off-the-shelf prices.

DS1005 5-Tap Delay Line
DS1007 7-in-1 Delay Line
DS1010 10-Tap Delay Line
DS1013 3-in-1 Delay Line
DS1020 Programmable Delay Line

Multiport Memory

Quad Port memory links four computers at low cost.



A complete family of FIFOs features identical pinouts that allow them to be interchanged. Designed for first-in, first-out procedures in storing and retrieving data, the products are dual-ported for simultaneous reads and writes.

The Quad Port Serial RAM multiport memory chip loosely couples up to four computers at low cost.

DS2009 512 x 9 FIFO
DS2010 1024 x 9 FIFO
DS2011 2048 x 9 FIFO
DS2012 4096 x 9 FIFO
DS2013 8192 x 9 FIFO
DS2015 Quad Port Serial RAM
DS2212 FIFO SipStik

Nonvolatile SRAM

Dallas Semiconductor has combined its circuitry and understanding of ultra low-power CMOS SRAM with improvements in long-life lithium power sources to develop a family of nonvolatile SRAMs that retain data for 10 years in the absence of main power. When power goes out of tolerance, the built-in lithium energy source automatically switches on and write protection guards data from garbling during power loss.

DS1200 1024-Bit Serial RAM
DS1220 2K x 8 NV SRAM
DS1225 8K x 8 NV SRAM
DS1235 32K x 8 NV SRAM
DS1245 128K x 8 SRAM
DS2217 128K x 8 SRAM SipStik
DS2222 256-Bit EconoRAM

Intelligent Sockets

Intelligent sockets incorporate active electronics in connectors that can be plugged into a system. Each adds an important capability without requiring substantive changes in the system. SmartSockets, with densities from 16/64K to 64/256K/1M, safeguard data in RAM for more than 10 years in the absence of external power. Smart-

Watches can time stamp and date events as well as nonvolatize RAM. They are available for SRAM densities from 16/64K to 64/256K to 1M or ROM densities from 64/256K to 64/256K/1M.

DS1213 SmartSocket
DS1216 SmartWatch/RAM
DS1216E SmartWatch/ROM

User-Insertable Memory

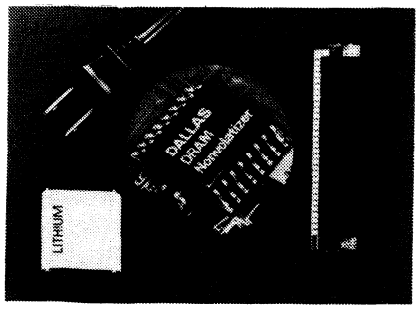
Nonvolatile memories with densities from 1024 to four million bits are packaged so that they can be simply plugged in. A built-in lithium energy source ensures storage of programs and data for more than 10 years in the absence of power. Applications for such products include software authorization, computer identification, system access control, secure personnel areas, calibration, automatic system setup, and traveling work record.

The KeyRing adapts our keys and tags to JEDEC bytewide memory signals without affecting system operation.

DS1201 Electronic Tag
DS1217 Nonvolatile Read/Write Cartridge
DS1250 KeyRing
DS6085 CyberCard

Integrated Battery Backup

This CMOS chip set crashproofs microprocessor-based systems, ensuring that no information is lost when main power fails. When power returns, computing resumes as if the failure had not occurred.



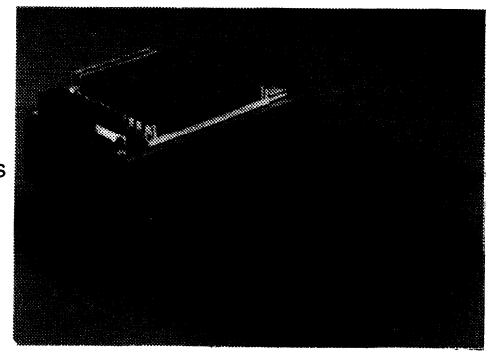
DRAM Nonvolatizer safeguards data and increases memory density.

The Power Monitor warns a processor of an impending power failure and provides for orderly shutdown and automatic restart. Various nonvolatile controllers are available for 1, 4, 8, or 16 CMOS SRAMs. The DRAM Nonvolatizer crashproofs DRAM memory. The SmartBattery is a low-cost backup energy source for portable and nonvolatile electronic equipment.

DS1210/11/12/21 Nonvolatile Controllers
DS1231 Power Monitor
DS1234 Conditional NV Controller
DS1237 DRAM Nonvolatizer
DS1259 Battery Manager
DS1260 Lithium SmartBattery

SipStik™ Prefabs

SipStiks are pretested subassemblies that snap into locking connectors for rapid construction of electronic systems. SipStiks increase density over traditional packing schemes five times by taking advantage of three, rather than the standard two, dimensions. SipStiks insert perpendicularly into the motherboard, making efficient use of the height dimension.



Up to 12 SipStiks can be snapped into this prototype motherboard for quick and compact system mock-up.

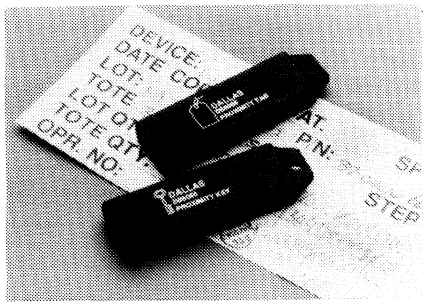
The Dallas Semiconductor SipStik family can provide approximately 80 percent of the circuitry in a typical system. With SipStik prototype accessories, a complete

system can be mocked up quickly and compactly.

DS2201 UHF Receiver
DS2212 FIFO
DS2217 128K x 8 NV SRAM
DS2219 1M x 9 NV DRAM
DS2230 Dual Port NV SRAM
DS2244 TeleMicro Controller
DS2245 1200 or 2400 bps Soft Modem
DS2249 DAA
DS2249PH Phantom DAA
DS2250 Soft Microcontroller
DS2250T Time Microcontroller
DS2255 Instrumentation
DS2265 Wireless Transceiver
DS2268 ADPCM Speech Compressor
DS2270 Speech Recorder
DS2280/2281 T1/CEPT Line Card
DS2287 Supervisory

Prototyping Accessories
DS9005 Eurocard Enclosure
DS9006 SipStik Motherboard
DS9006K SipStik Prototyping Kit

Automatic Identification



Proximity keys and tags automatically identify a person or object upon approach of a base station.

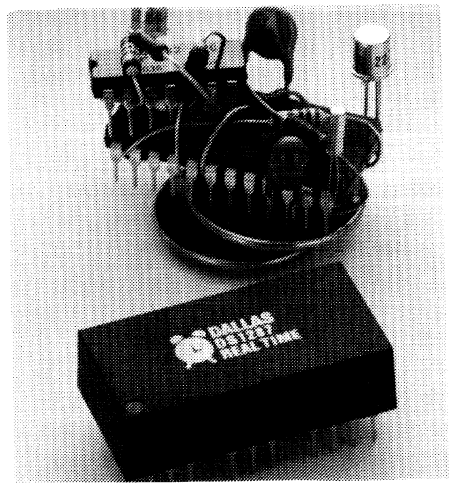
A new microchip structures two-way transmission of data through the air. The result is ID by proximity: a tagged item or person need only pass within five feet of a base station to be identified. Because the Wireless chips can be read *or* written, the tag's information can be updated while attached to an object. Products based on the chip can automatically track a work piece as it travels along an assembly line, identify a person for access control, or link a hand-held terminal to a host system.

A wide range of wireless devices can be created with our versatile Micro Power Receiver/Interpreter. In addition, we offer ready-to-use proximity devices, optional chips for building high capacity tags, wireless hand-helds, a complete subassembly that provides computer-to-computer wireless links, and a starter kit for evaluation.

DS1203 Micro Power Receiver
DS1209B Micro Power Receiver/ Interpreter
DS1280 Bytewide to Serial Converter
DS2201 UHF Receiver SipStik
DS2265 Wireless SipStik
DS6065 Proximity Key
DS6066 Proximity Tag
DS6068 RF Communicator
DS6068K Wireless Starter Kit

Timekeeping

A self-contained lithium energy source in conjunction with a silicon chip and quartz



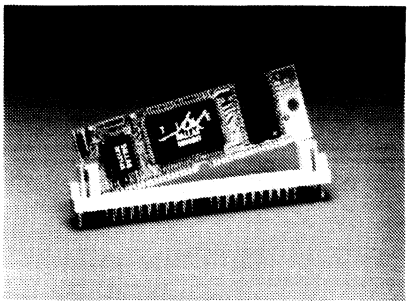
Real Time Clock replaces 20 parts used in IBM AT and PS 2 compatible computers.

form a permanently powered clock/ calendar within a single component. Various computer interfaces are available including phantom, serial, PC DOS, and bytewide memory.

DS1202 Serial Timekeeper
DS1215 TimeChip
DS1243Y Clock Plus 64K NV SRAM
DS1283 Watchdog Timechip
DS1286 Watchdog Timekeeper
DS1287 RealTime Clock
DS1387 RAMified Real Time

Microcontrollers

Unlike rigid ROM/EPROM-based microcontrollers, the DS5000 soft microcontrollers are designed for change: all memory is high-performance, read/write, and nonvolatile for more than ten years. They are equipped with up to 64K bytes of nonvolatile SRAM that can be dynamically partitioned to fit program and data storage requirements. They can even improve performance based on cumulative knowledge. A built-in lithium energy source and crashproof circuitry permit task processing to resume after a power outage. An encryptor protects proprietary application software and confidential data. The pinout and instruction set match the industry standard 8051 microcontroller.



Time Microcontroller SipStik schedules events and stores data for 10 years.

The Time Microcontroller adds the ability to log events and schedule activities by date and time.

DS2250 Soft Microcontroller SipStik
DS2250T Time Micro SipStik
DS5000 Soft Microcontroller
DS5000T Time Microcontroller
DS5000FP CMOS Microcontroller
DS5000TK Evaluation Kit
DS5000DK Development Kit

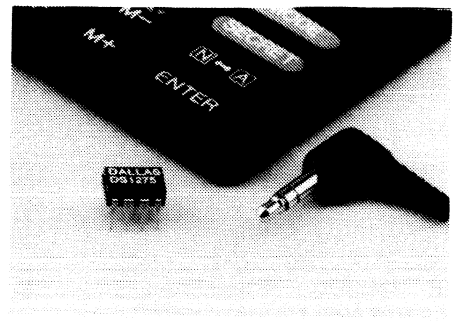
Security Products

These products provide security for intellectual property and assets. The Electronic Key controls access to software, buildings, and equipment. The TimeKey lets software authors and publishers limit the use of their products to a set period of time.

DS1204U Electronic Key
DS1207 TimeKey
DS1255 Printer Port KeyRing
DS1255C Software Authorization Cookbook

System Extension

These CMOS products add a variety of special features to systems without encumbering design.



Line Powered Transceiver connects portable systems to PCs without consuming battery energy.

DS1206 *Phantom Interface*: intercepts a standardized memory bus and adapts it to a three-wire serial port.
DS1222 *BankSwitch*: selects one of 16 memory banks under software control.
DS1223 *Electronic Configurator*: a nonvolatile switch, comparator, and read/write memory circuit that configures electronic equipment remotely.
DS1227 *KickStarter*: orchestrates power conservation in battery-operated systems.
DS232/DS1228 (1229) *+5V Powered Dual (Triple) RS-232 Transmitter/Receiver*: meets all EIA specifications while operating from a single +5 volt supply.

DS1232 *MicroMonitor*: acts as a watchdog for system malfunction by monitoring the microprocessor and restarting when it is out of control.

DS1236 *Micro Manager*: provides all necessary functions for power supply monitoring, reset control, and memory back-up in microprocessor-based systems.

DS1267 *Digital Potentiometer*: all-silicon pot can be set under software control and withstands the high temperatures associated with surface mounting.

DS1275 *Line Powered Transceiver*: connects portable systems to personal computers without consuming battery energy. Mates to the host with the DS9035 Mini RS-232 Cable, a three-conductor flexible cable with a miniature stereo jack at one end and an RJ11-to-DB25 at the other.

DS1290-1293 *Eliminator*: replaces eight manual switches used to option printed circuit boards.

Teleservicing

Teleservicing products turn the personal computer into a service manager. Teleservicing monitors equipment performance 24 hours a day, releases software revisions, performs diagnostics, and makes adjustments — all from a desktop computer connected to an ordinary telephone line. A growing family of hardware and software products offers solutions to service problems at a price well under the cost of a single airplane ticket.

DS0010 PC Service Manager Program
DS2230 TeleMemory Stik
DS2244 TeleMicro Stik
DS2245 Soft Modem Stik
DS2245K PC/XT/AT Add-In Card Modem
DS2249 DAA Stik
DS2249PH DAA Phantom
DS6070 TeleMicro Kit
DS6071 TeleMemory Kit

VOICE COMPRESSION

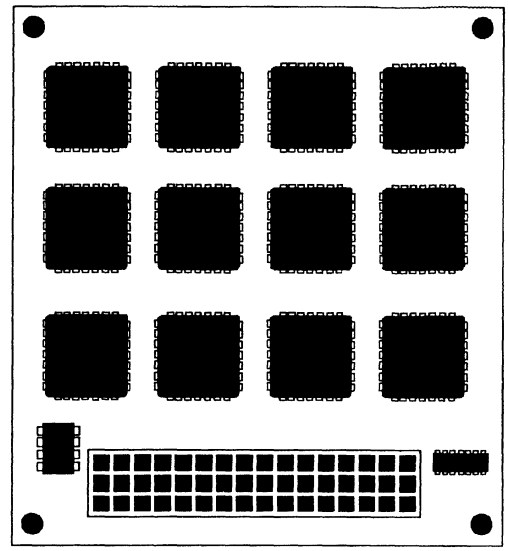
2

DALLAS SEMICONDUCTOR

DS2157/DS2158
ADPCM Array

FEATURES

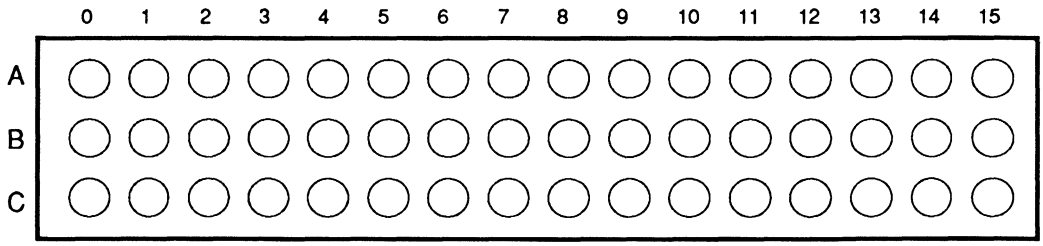
- High-density, multi-channel speech compression system provides full-duplex channels on a 3 x 3 inch board.
- Based on high-performance DS2167/68 ADPCM processors. DS2157 uses the DS2167 and supports the July 1986 T1Y1 recommended algorithm. DS2158 supports the "old" CCITT G.721 algorithm.
- Flexible data bussing scheme accommodates user's backplane data format and rate.
- Microcontroller-compatible port for system configuration. Onboard power monitor provides system reset.



DESCRIPTION

The DS2157 and DS2158 ADPCM Arrays use surface-mount technology and the DS2167/68 ADPCM processors to yield 12 or 24 full-duplex channels in nine square inches. The DS2157 array features the DS2167Q processor, which implements the July 1986 T1Y1 recommended ADPCM algorithm. The DS2158 array features the DS2168Q processor, which implements the "old" CCITT G.721 algorithm. The PCM data interfaces are organized into four independent busses which can be configured to best suit the data format on the user's system backplane. The array also includes input signal buffering and a power-monitor reset circuit.

SYSTEM PIN-OUT Figure 1



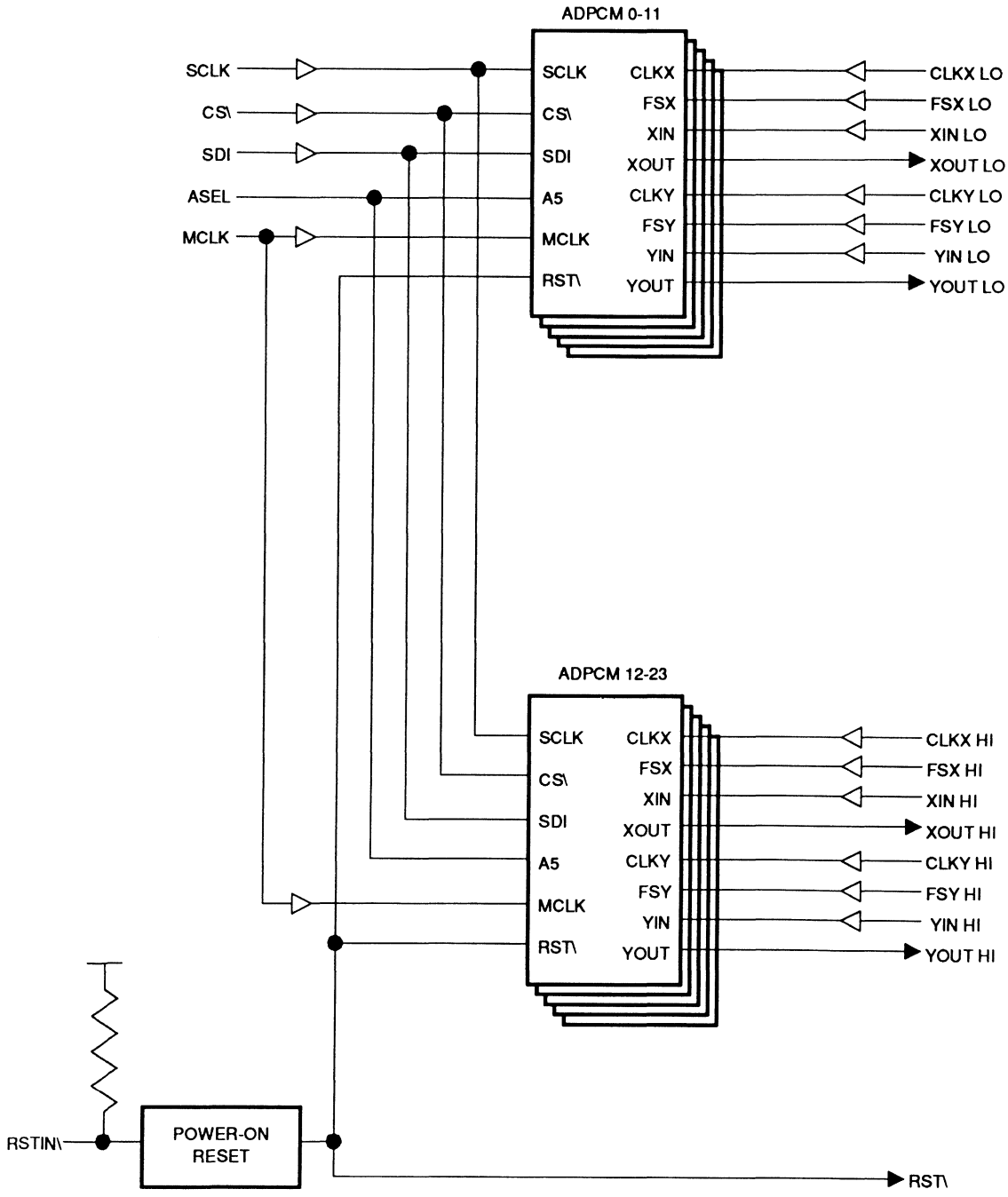
PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
Low X-Side Data Interface			
A3	CLKX LO	I	**Data Clock**
B5	FSX LO	I	**Frame Sync**
A4	XIN LO	I	**Data Input**
B3	XOUT LO	O	**Data Output**
Low Y-Side Data Interface			
C4	CLKY LO	I	**Data Clock**
B6	FSY LO	I	**Frame Sync**
C7	YIN LO	I	**Data Input**
C6	YOUT LO	O	**Data Output**
High X-Side Data Interface			
C11	CLKX HI	I	**Data Clock**
B12	FSX HI	I	**Frame Sync**
C9	XIN HI	I	**Data Input**
C8	XOUT HI	O	**Data Output**
High Y-Side Data Interface			
B13	CLKY HI	I	**Data Clock**
B10	FSY HI	I	**Frame Sync**
B11	YIN HI	I	**Data Input**
B9	YOUT HI	O	**Data Output**

PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
Serial Configuration Port			
B7	ASEL	I	**Array Address Select.** Selects processor addresses 0 through 23 (ASEL = VSS) or 32 through 55 (ASEL = VDD).
B4	CS\	I	**Serial Port Chip Select.** Drive low to initiate a serial port write sequence.
C3	SCLK	I	**Serial Data Clock.** Rising edge clocks in the configuration data.
C5	SDI	I	**Serial Data Input.** Configuration data, written LSB first.
System Control			
B1	MCLK	I	**Master Clock.** 10 MHz clock for ADPCM processing engine. May be asynchronous with other clocks.
C10	RST\	O	**Reset Output.** Normally high signal which transitions low at power-on or when RSTIN\ is activated.
C12	RSTIN\	I	**Reset Input.** A high-low-high transition initializes the array and sets all processors idle. Input is internally pulled high with a nominal 10K ohm resistor; can be left unconnected if not used.
Power			
A5-A9, B8			
	VDD		**Positive Supply.** 5.0 volts.
A0-2, A10-15, B0, B2, B14-15, C0-2, C13-15			
	VSS		**Signal Ground.** 0.0 volts.

BLOCK DIAGRAM Figure 2



MASTER CLOCK

The MCLK master clock input drives the ADPCM processors. This clock is 10 MHz and should be generated by a stable, crystal-based oscillator.

DATA BUSSING

The 24 ADPCM processors are split into two groups of 12, and each group is bussed separately. In addition, each processor has two independent data interfaces (X-side and Y-side) which are also bussed separately. Therefore, there are four data busses on the array: the low-X, low-Y, high-X and high-Y busses. Each bus consists of four signals: a data clock (typically running at 1.544 MHz, 2.048 MHz or 4.096 MHz), a frame synchronization signal (typically 8 KHz), a PCM/ADPCM data input, and a PCM/ADPCM data output. Please refer to the DS2167/68 data sheet for information on the PCM interface clocking and data signals. The busses can be operated separately, processing 12 channels per bus, or tied together to increase the number of channels processed per bus.

SYSTEM CONFIGURATION

All processors on the array share a common three-wire serial control port interface (CS\, SCLK, and SDI). This interface is directly compatible with popular microcontrollers such as the DS5000 and 8051. The port is used to define operating modes and timeslots for the processors in the array. Data written to the control port is either two bytes (address/command and control) or four bytes (address/command, control, input timeslot and output timeslot) in length. The address/command byte contains a field which specifies processor address (between 0 and 63) and a bit which selects a data interface (either X or Y). If the address in this byte matches the address assigned to a processor in the array, then that processor will accept the configuration data that follows.

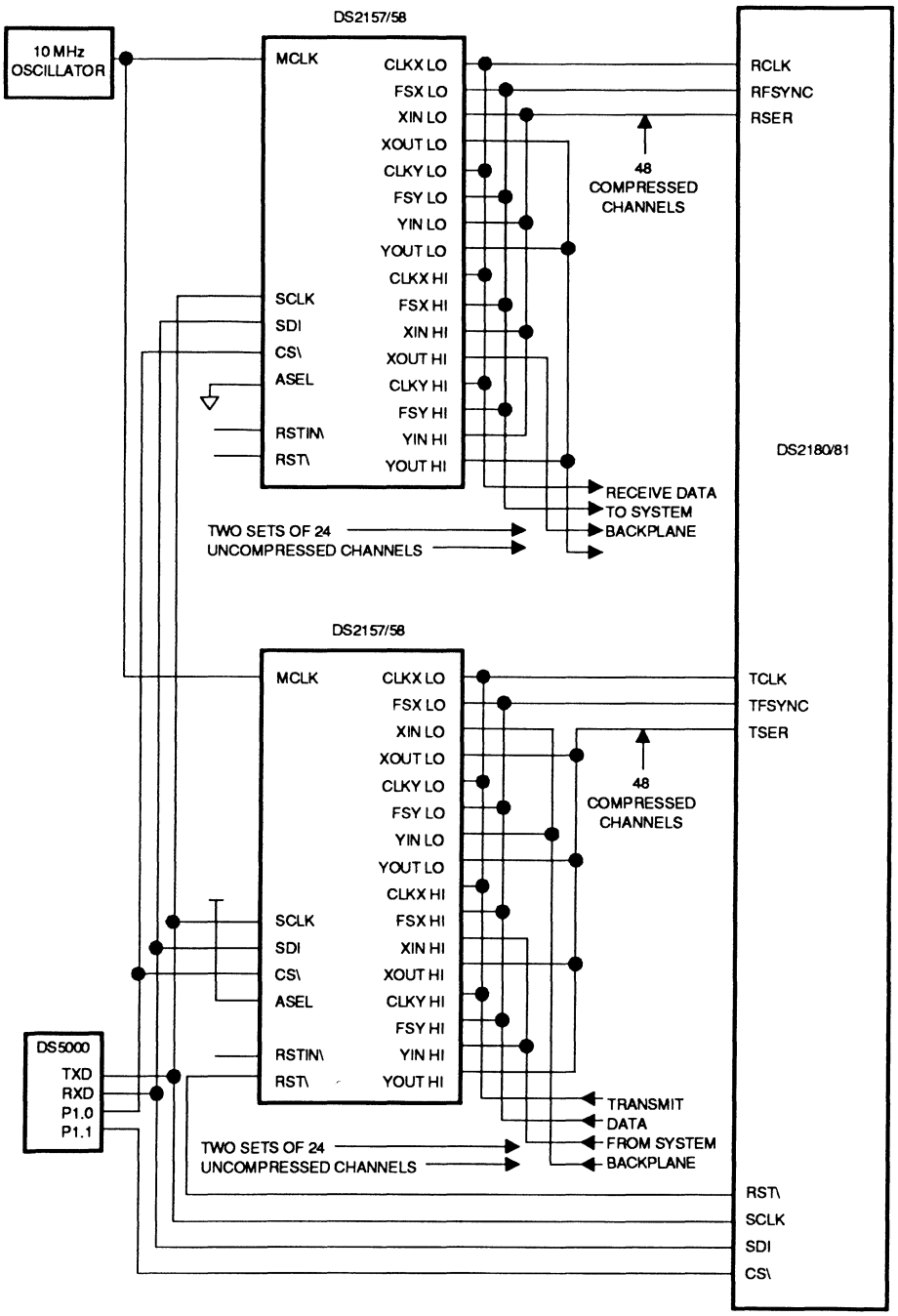
The ASEL input selects the addressing to the processors. With ASEL tied to VSS, the twelve processors on the low-X and low-Y busses are addressed as 0 through 11, and the 12 processors on the high-X and high-Y busses are addressed as 12 through 23. With ASEL tied to VDD, the processors on the low-X and low-Y busses are addressed as 32 through 43, and the processors on the high-X and high-Y busses are addressed as 44 through 55. This feature allows two arrays to share the same three-wire control port.

Please refer to the DS2167/68 data sheet for information on the processor configuration registers and writing to the serial control port.

SYSTEM RESET

A system reset initializes all processors in the array and places them into an idle mode. An on-board power monitor automatically generates a reset when power is applied. In addition, the RSTIN\ input allows the array to be reset externally. This input is internally tied high with a nominal 10K ohm resistor and can be left unconnected if not used. The system reset signal is available at the output RST\.

48-CHANNEL SYSTEM EXAMPLE Figure 3



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to 70°C

*This is a stress rating only and functional operation of the system at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.55		5.5	V	

CAPACITANCE

(T_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			20	pF	
Output Capacitance	C_{OUT}			120	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{DD}			985	mA	1,2
Standby Current	I_{DDPD}			75	mA	1,2,3
Input Leakage	I_{IL}					
MCLK		-200		+40	uA	
RSTIN\		-725		+50	uA	
all other inputs		-100		+20	uA	
Output Current @ 2.4V	I_{OH}					
RST\		-0.7			mA	
all other outputs		-1.0			mA	
Output Current @ 0.4V	I_{OL}	4.0			mA	
I/O Leakage	I_{IO}	-12.0		+12.0	uA	

NOTES:

1. CLKX LO = CLKY LO = CLKX HI = CLKY HI = 1.544 MHz, MCLK = 10 MHz.
2. Outputs open, inputs swinging full supply levels.
3. All channels of all processors programmed to "idle power down" mode.

PCM INTERFACE
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{DD}= 5V + 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK	t_{PM}		100		ns	
MCLK Pulse Width	t_{WMH},t_{WML}		50		ns	
MCLK Rise and Fall Times	t_{RM},t_{FM}		5	10	ns	
CLKX, CLKY Period	t_{PXY}		488		ns	4
CLKX, CLKY Pulse Width	t_{WXYH}, t_{WXYL}		244		ns	
CLKX, CLKY Rise and Fall Times	t_{RXY}, t_{FXY}		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	t_{HOLD}	0			ns	1
Setup Time from FSX ,FSY to CLKX, CLKY Low	t_{SF}	50			ns	1
Hold Time from CLKX, CLKY Low to FSX, FSY Low	t_{HF}	100			ns	1
XIN, YIN Setup to CLKX, CLKY Low	t_{SD}	50			ns	1
XIN, YIN Hold CLKX, CLKY Low	t_{HD}	50			ns	1
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	t_{DXYO}	5		150	ns	2
Delay Time from CLKX, CLKY to XOUT, YOUT Tri-stated	t_{DXYZ}	20		150	ns	1,2,3

NOTES:
1. Measured at V_{IH} = 2.0 OR V_{IL} = 0.8V and 10 ns maximum rise and fall times.
2. Load = 150 pF + 2 LSTTL loads.
3. For LSB of PCM byte or ADPCM nibble.
4. Maximum width of FSX, FSY is one CLKX, CLKY period.

MASTER CLOCK/RESET AC ELECTRICAL CHARACTERISTICS

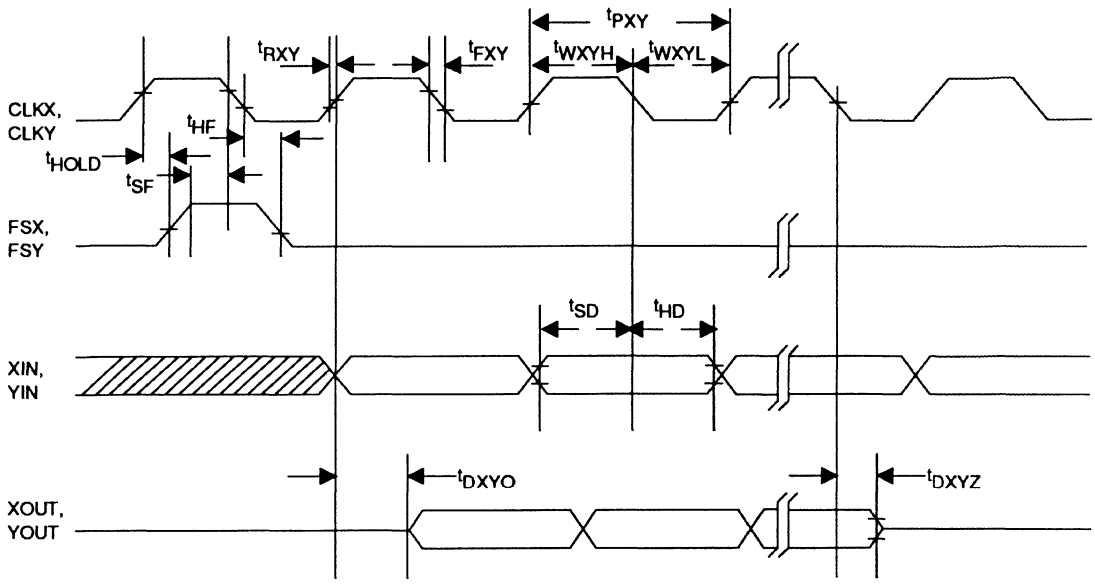
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	
MCLK Pulse Width	t_{WMH}, t_{WML}	50			ns	
V_{DD} Low Detect to RST\ Low	t_{RSTPD}			100	ns	
V_{DD} High Detect to RST\ High	t_{RSTX}	250		1000	ms	
Delay Time from RSTIN\ Low to RST\ Low	t_{RSTIN}	20			ms	
Delay Time from RSTIN\ High to RST\ High	t_{RSTX}	250		1000	ms	
RSTIN\ Pulse Width	t_{WRL}		1		ms	

SERIAL PORT AC ELECTRICAL CHARACTERISTICS

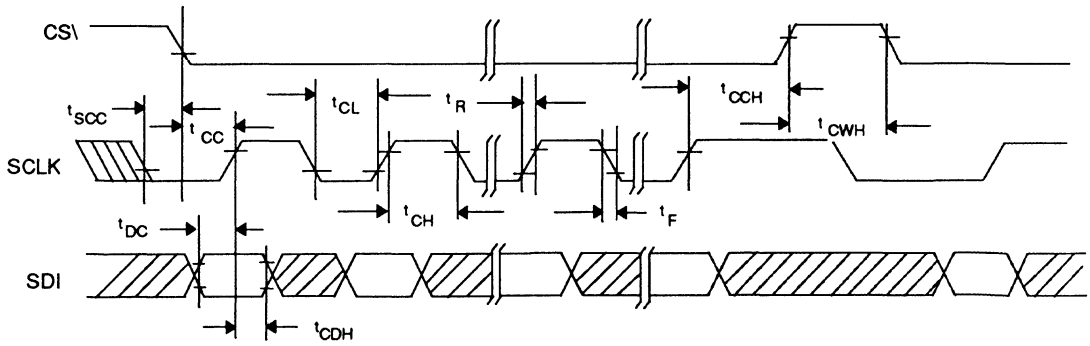
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Setup	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Times	t_R, t_F			100	ns	1
CS to SCLK Setup	t_{CC}	50			ns	1
SCLK to CS Hold	t_{CCH}	250			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
SCLK Setup to CS Falling	t_{SCC}	50			ns	1

NOTE: 1. Measured at V_{IH} = 2.0 or V_{IL} = 0.8V and 10ns maximum rise and fall times.

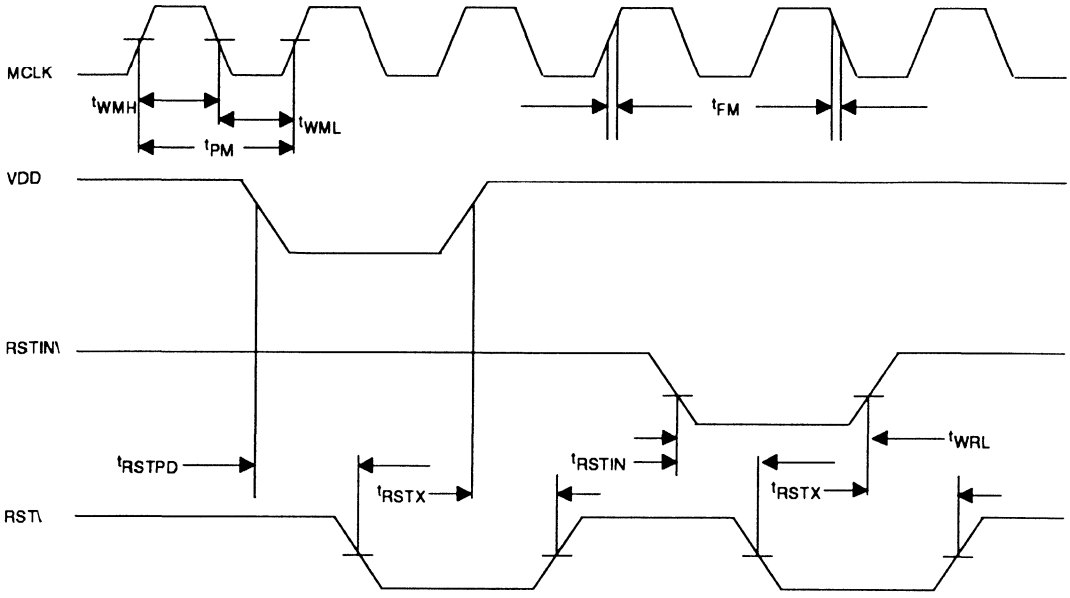
PCM INTERFACE AC TIMING DIAGRAM Figure 4



SERIAL PORT WRITE AC TIMING DIAGRAM Figure 5



MASTER CLOCK/RESET AC TIMING Figure 6



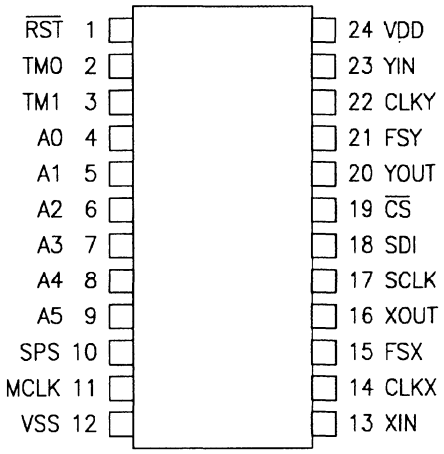
DALLAS SEMICONDUCTOR

DS2165/DS2165Q
16/24/32KBPS ADPCM PROCESSOR

FEATURES

- Compresses/expands 64Kbps PCM voice to/from either 32Kbps, 24Kbps, or 16Kbps
- Dual fully independent channel architecture; device can be programmed to perform either:
  - two expansions
  - two compressions
  - one expansion and one compression
- Interconnects directly to combo-codec devices
- Input to output delay is less than 375us
- Simple serial port used to configure the device
- Onboard Time Slot Assigner Circuit (TSAC) function allows data to be input/output at various time slots
- Supports Channel Associated Signaling
- Each channel can independently be idled or placed into bypass
- Available hardware mode requires no host processor; ideal for voice storage applications
- Backward-compatible with the DS2167
- Single +5V supply; low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC

PIN DESCRIPTION



DESCRIPTION

The DS2165 is a dedicated Digital Signal Processing (DSP) chip that has been optimized to perform Adaptive Differential Pulse Code Modulation (ADPCM) speech compression at three different rates. The chip can be programmed to compress (expand) 64Kbps voice data down to (up from) either 32Kbps, 24Kbps, or 16Kbps. The compression to 32Kbps follows the algorithm specified by CCITT Recommendation G.721 (July 1986) and ANSI document T1.301 (April 1987). The compression to 24Kbps follows ANSI document T1.303. The compression to 16Kbps follows a proprietary algorithm developed by Dallas Semiconductor. The DS2165 can switch compression algorithms on-the-fly. This allows the user to make maximum use of the available bandwidth on a dynamic basis.

OVERVIEW

The DS2165 contains three major functional blocks: a high performance (10 MIPS) DSP engine, two independent PCM interfaces (X and Y) which connect directly to serial Time Division Multiplexed (TDM) backplanes, and a serial port that can configure the device on-the-fly via an external controller. A 10 MHz master clock is required by the DSP engine. The DS2165 can be configured to perform either two expansions, two compressions, or one expansion and one compression. The PCM/ADPCM data interfaces support data rates from 256KHz to 4.096MHz. Typically, the PCM data rates will be 1.544MHz for U - law and 2.048MHz for A - law. Each channel on the device samples the serial input PCM or ADPCM bit stream during a user-programmed input time slot, processes the data and outputs the result during a user-programmed output time slot.

Each PCM interface has a control register which specifies functional characteristics (compress, expand, bypass, and idle), data format (U - law or A - law), and algorithm reset control. With the SPS pin strapped high, the software mode is enabled and the serial port can be used to configure the device. In this mode, a novel addressing scheme allows multiple devices to share a common three-wire control bus, simplifying system-level interconnect.

With SPS low, the hardware mode is enabled. This mode disables the serial port and maps certain control register bits to some of the address and serial port pins. Under the hardware mode, no external host controller is required and all PCM/ADPCM input and output time slots default to time slot 0.

PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**RST**	I	**Reset.** A high-low-high transition resets the algorithm. The device should be reset on power up and when changing to or from the hardware mode.
2 3	**TM0** **TM1**	I	**Test Modes 0 and 1.** Tie to VSS for normal operation.
4 5 6 7 8 9	**A0** **A1** **A2** **A3** **A4** **A5**	I	**Address Select.** A0 = LSB; A5 = MSB Must match address/command word to enable the serial port.
10	**SPS**	I	**Serial Port Select.** Tie to VDD to select the serial port; tie to VSS to select the hardware mode.
11	**MCLK**	I	**Master Clock.** 10 MHz clock for the ADPCM processing engine; may be asynchronous to SCLK, CLKX, and CLKY.
12	**VSS**	-	**Signal Ground.** 0.0 volts.

13	XIN	I	**X Data In.** Sampled on falling edge of CLKX during selected time slots.
14	CLKX	I	**X Data Clock.** Data clock for the X side PCM interface; must be synchronous with FSX.
15	FSX	I	**X Frame Sync.** 8 KHz frame sync for the X side PCM interface.
16	XOUT	O	**X Data Output.** Updated on rising edge of CLKX during selected time slots.
17	SCLK	I	**Serial Data Clock.** Used to write to the serial port registers.
18	SDI	I	**Serial Data In.** Data for onboard control registers; sampled on the rising edge of SCLK. LSB sent first.
19	CS	I	**Chip Select.** Must be low to write to the serial port.
20	YOUT	O	**Y Data Output.** Updated on rising edge of CLKY during selected time slots.
21	FSY	I	**Y Frame Sync.** 8 KHz frame sync for the Y side PCM interface.
22	CLKY	I	**Y Data Clock.** Data clock for the Y side PCM interface; must be synchronous with FSY.
23	YIN	I	**Y Data In.** Sampled on falling edge of CLKY during selected time slots.
24	VDD	-	**Positive Supply.** 5.0 volts.

HARDWARE RESET

RST allows the user to reset both channel algorithms and the contents of the internal registers. This pin must be held low for at least 1 millisecond on system power-up after the master clock is stable to ensure that that the device has intialized properly. RST should also be asserted when changing to or from the hardware mode. RST clears all bits of the Control Register for both channels except the IPD bits; the IPD bits for both channels are set to one.

SOFTWARE MODE

Tying SPS high enables the software mode. In this mode, an external host controller writes configuration data to the DS2165 via the serial port through inputs SCLK, SDI, and CS. (See Figure 2.) Each write to the DS2165 is either a two-byte write or a four-byte write. A two-byte write consists of the Address/Command Byte (ACB) followed by a byte to configure the Control Register (CR) for either the X or Y channel. The four-byte write consists of the ACB followed by a byte to configure the CR and then one byte to set the input time slot and another byte to set the output time slot.

ADDRESS/COMMAND BYTE

In the software mode, the address/command byte is the first byte written to the serial port; it identifies which of the 64 possible ADPCM processors sharing the port wiring is to be updated. Address data must match that at inputs A0 to A5. If no match occurs, the device ignores the following configuration data. If an address match occurs, the next three bytes written are accepted as control, input and output time slot data. Bit ACB.6 determines which side (X or Y) of the device is to be updated.

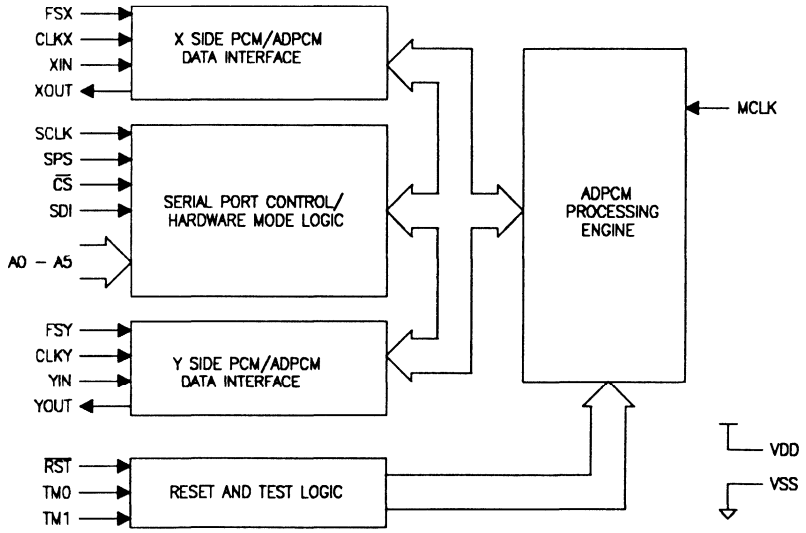
CONTROL REGISTER

The control register establishes idle, algorithm reset, bypass, data format and channel coding for the selected channel.

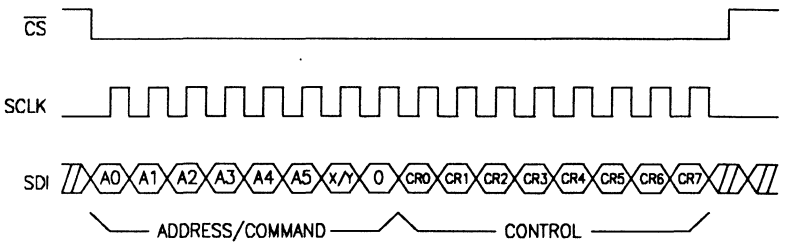
The X and Y side PCM interfaces may be independently disabled (output 3-stated) via IPD. When IPD is set for both channels, the device enters a low-power stand by mode. In this mode, the serial port must not be operated faster than 39KHz.

ALRST resets the algorithm coefficients for the selected channel to their initial values. ALRST

DS2165 BLOCK DIAGRAM Figure 1



SERIAL PORT WRITE Figure 2



NOTE:
A two-byte write is shown.

will be cleared by the device when the algorithm reset is complete.

The bypass feature is enabled when BYP is set and IPD is cleared. During bypass, no expansion or compression occurs. Bypass operates on byte-wide (8 bits) slots when CP/EX is set and on nibble-wide (4 bits) slots when CP/EX is cleared.

A-law (U/A = 0) and U-law (U/A = 1) PCM coding is independently selected for the X and Y channels via CR.2. If BYP and IPD are cleared, then CP/EX determines if the input data is to be compressed or expanded.

ADDRESS/COMMAND BYTE Figure 3

(MSB)							(LSB)
-	X/Y	A5	A4	A3	A2	A1	A0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	ACB.7	Reserved; must be zero for proper operation
X/Y	ACB.6	X/Y Channel Select 0 = update channel Y characteristics 1 = update channel X characteristics
A5	ACB.5	MSB of Device Address
A4	ACB.4	
A3	ACB.3	
A2	ACB.2	
A1	ACB.1	
A0	ACB.0	LSB of Device Address

CONTROL REGISTER Figure 4

(MSB)							(LSB)
AS0	AS1	IPD	ALRST	BYP	U/A	AS2	CP/EX

SYMBOL	POSITION	NAME AND DESCRIPTION
AS0	CR.7	Algorithm Select 0. See Table 2.
AS1	CR.6	Algorithm Select 1. See Table 2.
IPD	CR.5	Idle and Power Down. 0 = channel enabled 1 = channel disabled (output 3-stated)
ALRST	CR.4	Algorithm Reset. 0 = normal operation 1 = reset algorithm for selected channel
BYP	CR.3	Bypass. 0 = normal operation 1 = bypass selected channel
U/A	CR.2	Data Format. 0 = A - law 1 = U - law
AS2	CR.1	Algorithm Select 2. See Table 2.
CP/EX	CR.0	Channel Coding. 0 = expand (decode) selected channel 1 = compress (encode) selected channel

ALGORITHM SELECT BITS Table 2

ALGORITHM SELECTED	AS2	AS1	AS0
64Kbps to/from 32Kbps	0	0	0
64Kbps to/from 24Kbps	1	1	1
64Kbps to/from 16Kbps	1	0	1

INPUT TIME SLOT REGISTER Figure 5

(MSB)							(LSB)
-	-	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	ITR.7	Reserved; must be zero for proper operation.
-	ITR.6	Reserved; must be zero for proper operation.
D5	ITR.5	MSB of input time slot register.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input time slot register.

OUTPUT TIME SLOT REGISTER Figure 6

(MSB)							(LSB)
-	-	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	OTR.7	Reserved; must be zero for proper operation.
-	OTR.6	Reserved; must be zero for proper operation.
D5	OTR.5	MSB of output time slot register.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output time slot register.

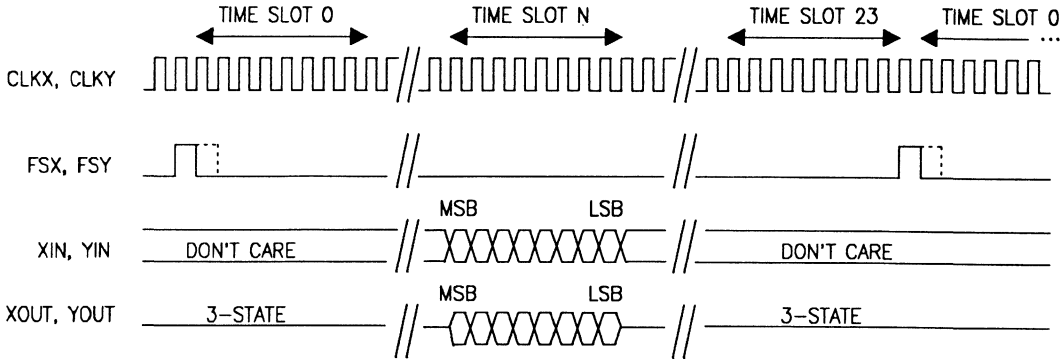
TIME SLOT ASSIGNMENT/ ORGANIZATION

Onboard counters establish when PCM and ADPCM I/O occurs. The counters are programmed via the time slot registers. Time slot size (number of bits wide) is determined by the state of CP/EX. The number is time slots available is determined by both the state of CP/EX and U/A. (See Figures 7 through 10.) For example, if the X channel is set to compress (CP/EX = 1) and it is set to expect U -law data (U/A = 0), then the input port (XIN) is set up for 24 8-bit time slots and the output port (XOUT) is set up for 48 4-bit time slots. (See Table 3.) The time slot organization is not dependent on which algorithm has been selected. NOTE: Time slots are counted from the frame sync signal starting at the first rising edge of either CLKX or CLKY after the frame sync.

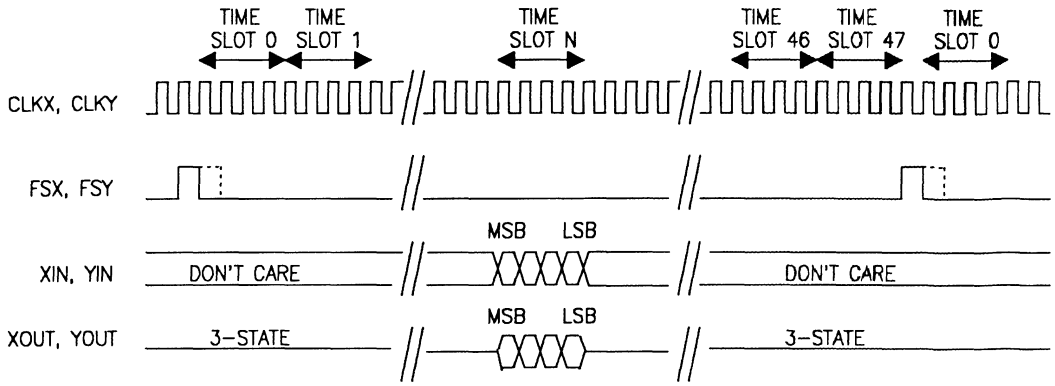
TIME SLOT ORGANIZATION Table 3

CHANNEL CONFIGURATION	# OF INPUT TIME SLOTS	# OF OUTPUT TIME SLOTS
CP/EX = 0; U/A = 1	48	24
CP/EX = 1; U/A = 1	24	48
CP/EX = 0; U/A = 0	64	32
CP/EX = 1; U/A = 0	32	64

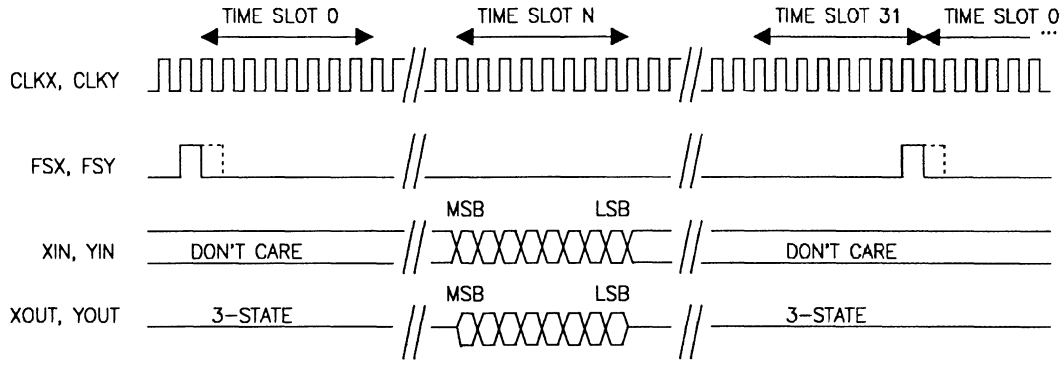
DS2165 U-LAW PCM INTERFACE Figure 7



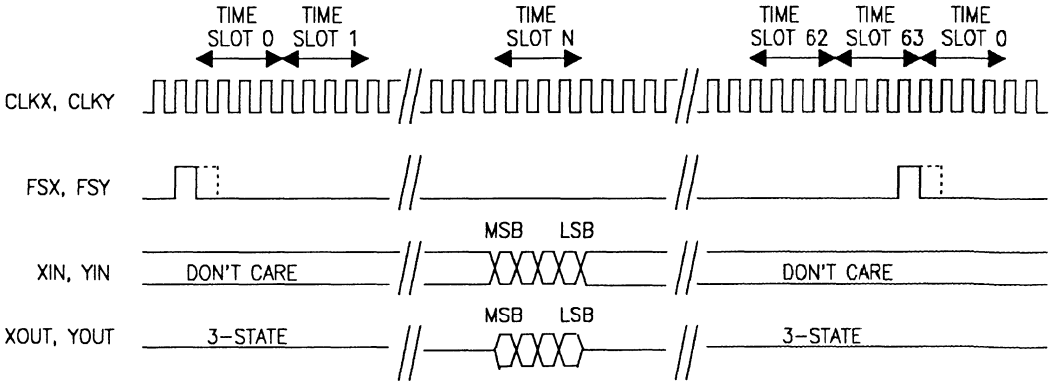
DS2165 U-LAW ADPCM INTERFACE Figure 8



DS2165 A-LAW PCM INTERFACE Figure 9



DS2165 A-LAW ADPCM INTERFACE Figure 10



HARDWARE MODE

The hardware mode is intended for applications that do not have an external controller available or do not require the extended features offered by the serial port. Tying the SPS pin to VSS disables the serial port, clears all internal register bits and maps the IPD, U/A, and CP/EX bits for both channels to external bits. (See Table 3.) In the hardware mode, both the input and output time slots default to time slot zero.

2

HARWARE MODE Table 4

PIN # / NAME	REG. LOCATION	NAME AND DESCRIPTION
4 / A0	CP / EX (Channel X)	Channel X Coding Configuration 0 = Expand 1 = Compress
5 / A1	AS0 / AS1 / AS2 (Channel X & Y)	Algorithm Select (see Table 5)
6 / A2	U / A (Channel X)	Channel X Data Format 0 = A - law 1 = U - law
7 / A3	CP / EX (Channel Y)	Channel Y Coding Configuration 0 = Expand 1 = Compress
8 / A4	AS0 / AS1 / AS2 (Channel X & Y)	Algorithm Select (see Table 5)
9 / A5	U / A (Channel Y)	Channel Y Data Format 0 = A - law 1 = U - law
18 / SDI	IPD (Channel Y)	Channel Y Idle Select 0 = Channel active 1 = Channel idle
19 / CS	IPD (Channel X)	Channel X Idle Select 0 = Channel active 1 = Channel idle

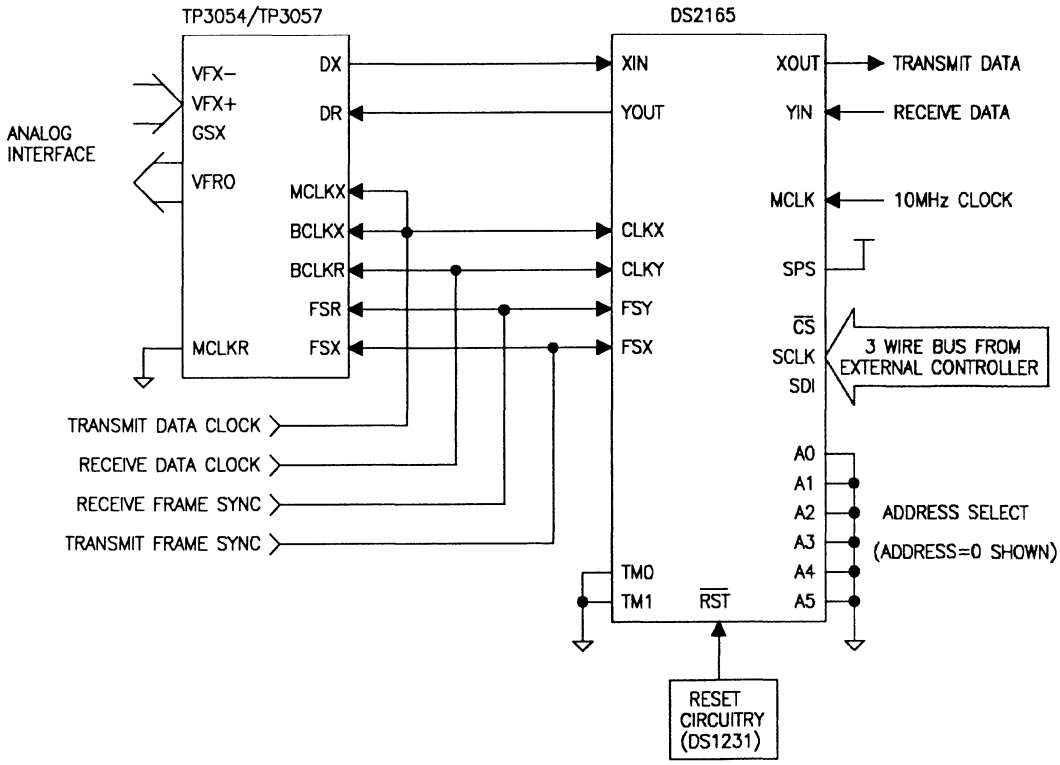
NOTES:

1. SCLK must be tied to VSS when the hardware mode is selected.
2. When both channels are idled, power consumption is significantly reduced.
3. The DS2165 will power-up within 800 milliseconds after either channel is returned to active from an idle state.

ALGORITHM SELECT FOR HARDWARE MODE Table 5

ALGORITHM	CONFIGURATION OF A1 AND A4
64Kbps to/from 32Kbps	tie both A1 and A4 to VSS
64Kbps to/from 24Kbps	hold A1 and A4 low during a hardware reset; take both A1 and A4 high after the RST pin has returned high (allow 3us after RST returns high before taking A1 and A4 high)
64Kbps to/from 16Kbps	tie both A1 and A4 to VDD

DS2165 CONNECTION TO COMBO CODEC Figure 11

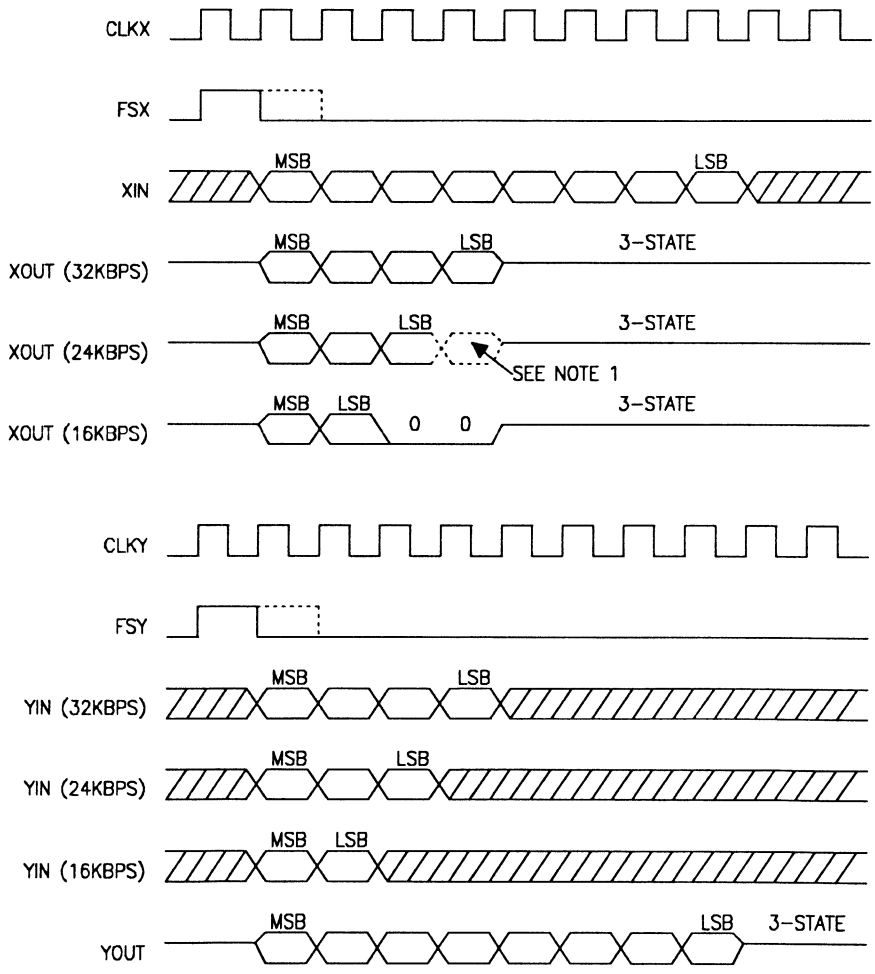


NOTE:
TP3054 and TP3057 are National Semiconductor Combo Codecs.

PCM AND ADPCM INPUT/OUTPUT

Since the organization of the input and output time slots on the DS2165 does not depend on the algorithm selected, it always assumes that PCM input and output will be in 8-bit bytes and that ADPCM input and output will be in 4-bit bytes. Figure 12 demonstrates how the DS2165 handles the I/O for the three different algorithms. In the figure, it is assumed that channel X is in the compression mode (CP/EX = 1) and channel Y is in the expansion mode (CP/EX = 0). Also, it is assumed that both the input and output time slots for both channels are set to zero.

PCM AND ADPCM I/O EXAMPLE Figure 12



NOTE:

1. The bit after the LSB in the 24Kbps ADPCM output will only be a one when the DS2165 is operated in the software mode and is programmed to perform 24Kbps compression; in all other configurations, it will be a zero.

TIME SLOT RESRICTIONS

Under certain conditions, the DS2165 does contain some restrictions on the output time slots that are available. These restrictions are covered in detail in Appendix A. No restrictions occur if the DS2165 is operated in the hardware mode.

INPUT TO OUTPUT DELAY

With all three compressions algorithms, the total delay from the time the PCM data sample is captured by the DS2165 to the time it is output is always less than 375us. The exact delay is determined by the input and output time slots selected for each channel.

CHANNEL ASSOCIATED SIGNALING

The DS2165 supports Channel Associated Signaling (CAS) via its ability to automatically change from the 32Kbps compression algorithm to the 24Kbps algorithm. If the DS2165 is configured to perform the 32Kbps algorithm, then in both the hardware and software mode, it will sense the frame sync inputs (FSX and FSY) for a double wide frame sync pulse. Whenever the DS2165 receives a double wide pulse, it will automatically switch from the 32Kbps algorithm to the 24Kbps algorithm. Switching to the 24Kbps algorithm allows the user to insert signaling data into the LSB bit position of the ADPCM output because this bit does not contain any useful speech information.

ON-THE-FLY ALGORITHM SELECTION

In the software mode, the user can switch between the three available algorithms on-the-fly. That is, the DS2165 does not need to be reset or stopped to make the change from one algorithm to another. The DS2165 reads the Control Register before it starts to process each PCM or ADPCM sample. If the user wishes to switch algorithms, then the Control Register must be updated via the serial port before the first input sample to be processed with the new algorithm arrives at either XIN or YIN.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Cap.	C_{IN}			5	pF	
Output Cap.	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{DDA}		30		mA	1,2
Idle Supply Current	I_{DDPD}		1		mA	1,2,3
Input Leakage	I_I	-1.0		+1.0	uA	
Output Leakage	I_O	-1.0		+1.0	uA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. CLKX = CLKY = 1.544MHz; MCLK = 10MHz
2. Outputs open; inputs swinging full supply levels
3. Both channels in idle mode
4. XOUT and YOUT are 3-stated

PCM INTERFACE
AC ELECTRICAL CHARACTERISTICS

($0^{o}C$ to $70^{o}C$; V_{DD}=5V +/-10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLKX, CLKY Period	t_{PXY}	244		3906	ns	1
CLKX, CLKY Pulse Width	t_{WXYL} t_{WXYH}	100			ns	
CLKX, CLKY Rise Fall Times	t_{RXY} t_{FXY}		10	20	ns	
Hold Time from CLKX,CLKY to FSX, FSY	t_{HOLD}	0			ns	2
Setup Time from FSX, FSY high to CLKX, CLKY Low	t_{SF}	50			ns	2
Hold Time from CLKX, CLKY Low to FSX, FSY Low	t_{HF}	100			ns	2
Setup Time for XIN,YIN to CLKX, CLKY Low	t_{SD}	50			ns	2
Hold Time for XIN, YIN to CLKX, CLKY low	t_{HD}	50			ns	2
Delay Time from CLKX,CLKY to Valid XOUT, YOUT	t_{DXYO}	10		150	ns	3
Delay Time from CLKX, XOUT, YOUT 3-stated	t_{DXYZ}	20		150	ns	2,3,4

NOTES:
1. Maximum width of FSX and FSY is one CLKX or CLKY period (except for signaling frames).
2. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.
3. Load = 150pF + 2 LSTTL loads.
4. For LSB of PCM or ADPCM byte.

MASTER CLOCK / RESET
AC ELECTRICAL CHARACTERISTICS

($0^{o}C$ to $70^{o}C$; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	1
MCLK Pulse Width	t_{WMH} t_{WML}	45	50	55	ns	
MCLK Rise/Fall Times	t_{RM}, t_{FM}			10	ns	
RST Pulse Width	t_{RST}	1			ms	

NOTE:
1. MCLK = 10MHz +/- 500ppm

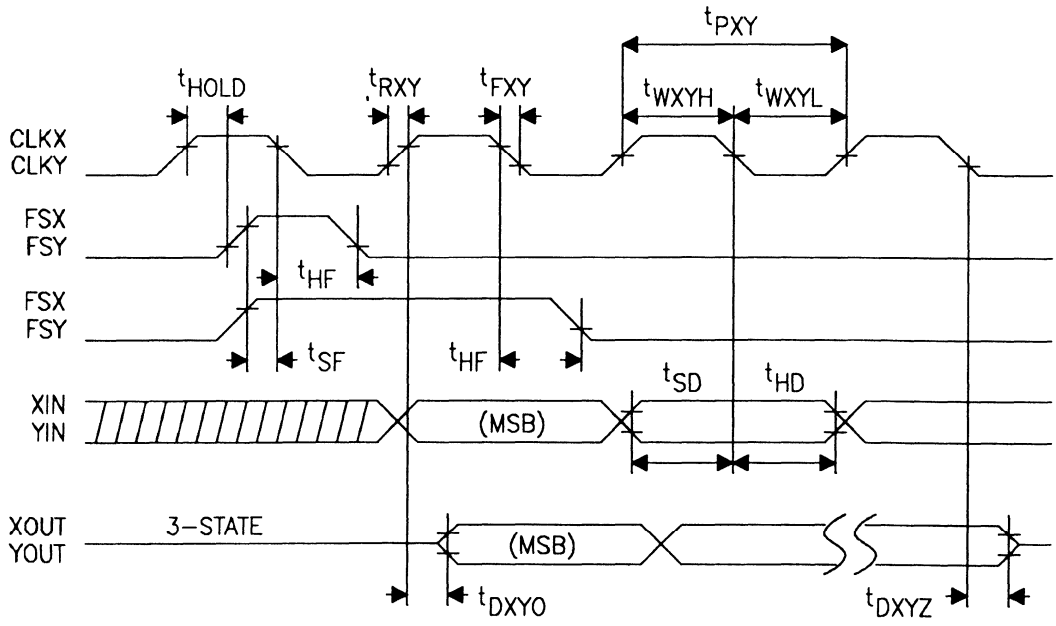
SERIAL PORT
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/- 10%)

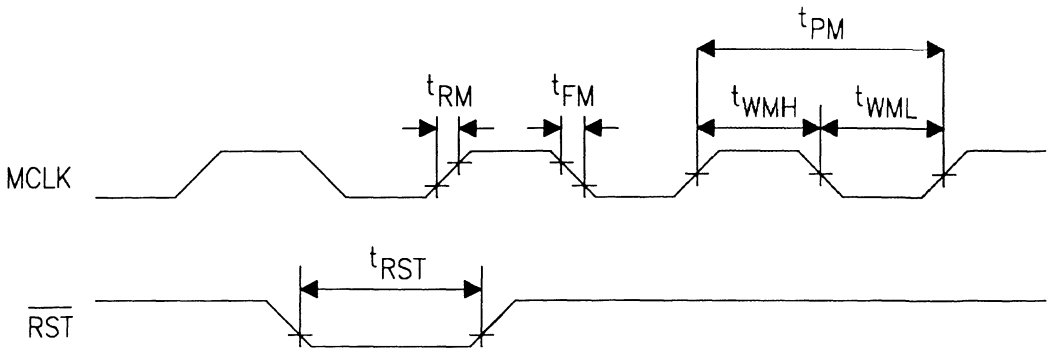
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Setup	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Time	t_R, t_F			100	ns	1
CS to SCLK Setup	t_{CC}	50			ns	1
SCLK to CS Hold	t_{CCH}	250			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
SCLK Setup to CS Falling	t_{SCC}	50			ns	1

NOTE:
1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.

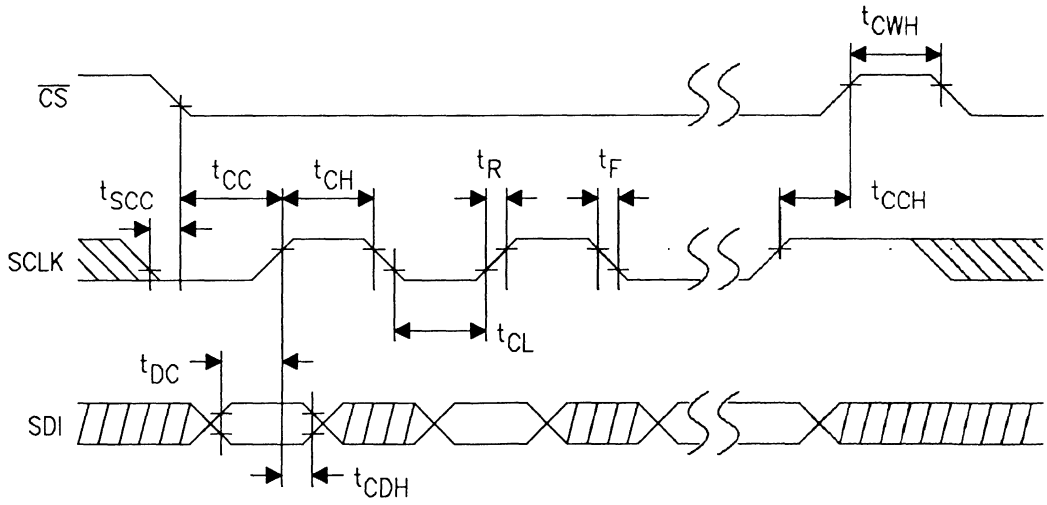
PCM INTERFACE AC TIMING DIAGRAM Figure 13



MASTER CLOCK / RESET AC TIMING DIAGRAM Figure 14



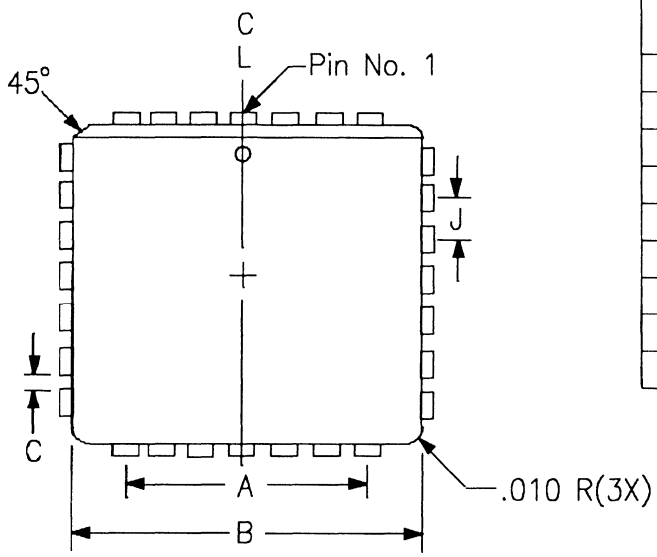
SERIAL PORT AC TIMING DIAGRAM Figure 15



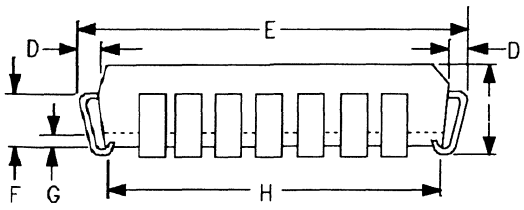
NOTE:
SCLK may be either high or low when CS is taken low.

16/24/32KBPS ADPCM Processor
DS2165Q
28-Pin PLCC

2

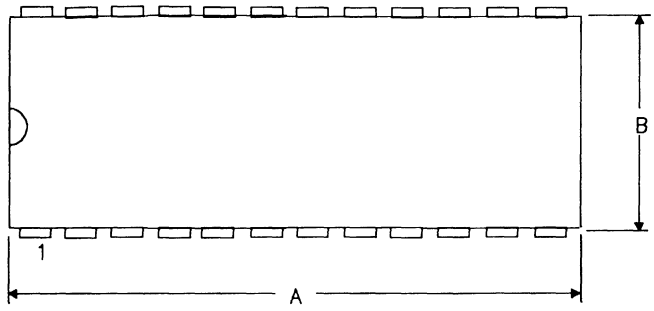


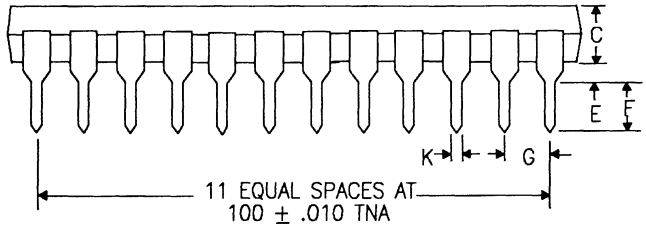
DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
J	.048	.052

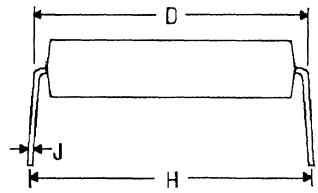


16/24/32KBPS ADPCM Processor
DS2165
24-Pin DIP

DIM.	INCHES	
	MIN.	MAX.
A	1.240	1.280
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021







DALLAS SEMICONDUCTOR

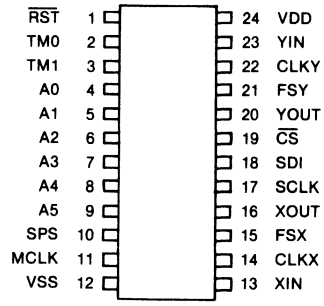
DS2167
DS2168
ADPCM PROCESSOR

2

FEATURES

- Speech compression chip compatible with standard ADPCM algorithms:
  - DS2167 supports "new" T1Y1 recommendations (July 1986) and "new" CCITT G.721 recommendations
  - DS2168 supports "old" CCITT G.721 recommendations
- Dual independent channel architecture—device may be programmed to perform full duplex , 2-channel expansions, or 2-channel compressions
- Interconnects directly with *u*-law or A-law combo-codec devices
- Serial PCM and control port interfaces minimize "glue logic" in multiple channel applications
  - On-chip channel counters identify input and output timeslots in TDM-based systems
  - Unique addressing scheme simplifies device control; 3-wire port shared among 64 devices
  - Bypass and idle features allow dynamic allocation of channel bandwidth, minimize system power requirements
- Hardware mode intended for stand-alone use
  - No host processor required
  - Ideal for voice mail applications
- 28-pin surface-mount package available, designated DS2167Q/ DS2168Q

PIN CONNECTIONS



DESCRIPTION

The DS2167 and DS2168 are dedicated digital signal processor (DSP) CMOS chips optimized for Adaptive Differential Pulse Code Modulation (ADPCM) based speech compression algorithms. The devices halve the transmission bandwidth of "toll quality" voice from 64K to 32K bits/second and are utilized in PCM-based telephony networks.

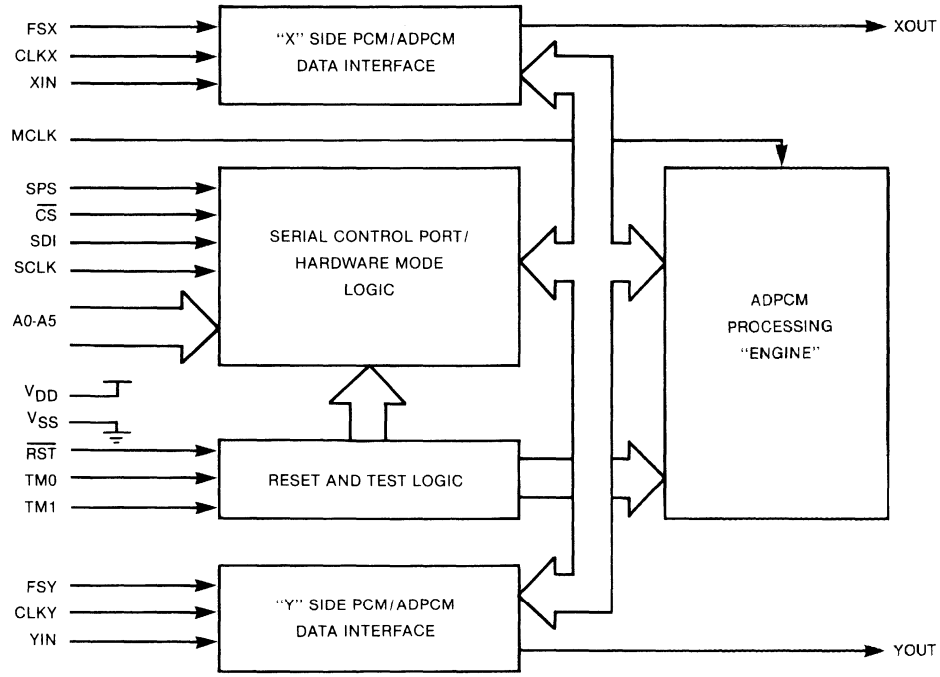
PRODUCT OVERVIEW

The DS2167 and DS2168 contain three major functional blocks: a high performance (10 MIPS) DSP "engine," two independent PCM data interfaces ("X" and "Y") which connect directly to serial time division multiplexed (TDM) backplanes and a microcontroller-compatible serial port for "on-the-fly" device configuration. A 10 MHz master clock is required by the DSP engine. The devices' dual channel architecture supports full duplex, dual compression or dual expansion operation. The PCM data interfaces support 1.544, 2.048 and 4.096 MHz data rates. Each device samples the serial PCM or ADPCM bit stream during a user-programmed input timeslot, processes the data, and outputs the result during a user-programmed output timeslot.

Each PCM interface has a control register which specifies functional characteristics (compress, expand, bypass and idle), data format (μ-law or A-law) and algorithm reset control. With the SPS pin strapped high, the software mode is enabled and the serial port is used to program control and timeslot registers. In this mode, a novel addressing scheme allows multiple devices to share a common three-wire control bus, simplifying system level interconnect.

With SPS low the hardware mode is enabled. This mode disables the serial port and maps appropriate control register bits to address and port inputs. Under hardware mode, no host controller is required and all PCM I/O defaults to timeslot 0. This stand-alone mode is compatible with popular codecs.

DS2168 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	$\overline{\text{RST}}$	I	**Reset.** A high-low-high transition clears all internal registers and resets both algorithms. The device should be reset on system power-up, and/or when changing to/from hardware mode.
2 3	**TM0** **TM1**	I	**Test Modes 0 and 1.** Tie to VSS for normal operation.
4 5 6 7 8 9	**A0** **A1** **A2** **A3** **A4** **A5**	I	**Address Select.** A0 = LSB; A5 = MSB. Must match address/ command word to enable serial port write.
10	**SPS**	I	**Serial Port Select.** Tie to VDD to select the serial port, to VSS to select the hardware mode.
11	**MCLK**	I	**Master Clock.** 10 MHz clock for ADPCM processing "engine;" may asynchronous to SCLK, CLKX AND CLKY.
12	**VSS**	—	**SIGNAL GROUND.** 0.0 volts.
13	**XIN**	I	**X Data In.** Sampled on falling edge of CLKX during selected timeslots.
14	**CLKX**	I	**X Data Clock.** Data clock for X side PCM interface, must be coherent and rising edge aligned with FSX.
15	**FSX**	I	**X Frame Sync.** 8 KHz frame sync for X side PCM interface.
16	**XOUT**	O	**X Data Out.** Updated on rising edge of CLKX during selected timeslots.
17	**SCLK**	I	**Serial Data Clock.** Used to write serial port registers.
18	**SDI**	I	**Serial Data In.** Data for on-board control registers. Sampled on rising edge of SCLK.
19	$\overline{\text{CS}}$	I	**Chip Select.** Must be low to write the serial port.
20	**YOUT**	O	**Y Data Out.** Updated on rising edge of CLKY during selected timeslots.
21	**FSY**	I	**Y Frame Sync.** 8 KHz frame sync for Y side PCM interface.
22	**CLKY**	I	**Y Data Clock.** Data clock for Y side PCM interface; must be coherent and rising edge aligned with FSY.
23	**YIN**	I	**Y Data In.** Sampled on falling edge of CLKY during selected timeslots.
24	**VDD**	—	**Positive Supply.** 5.0 volts.

HARDWARE RESET
$\overline{RST}$ allows the user to reset both channel algorithms and internal register contents. This input must be held low for at least 1 millisecond on system power-up after master clock is stable to assure proper initialization of the device. $\overline{RST}$ should also be asserted when changing to/from the hardware mode. $\overline{RST}$ clears all bits of the control register except IPD; IPD is set for both channels, powering down the device.

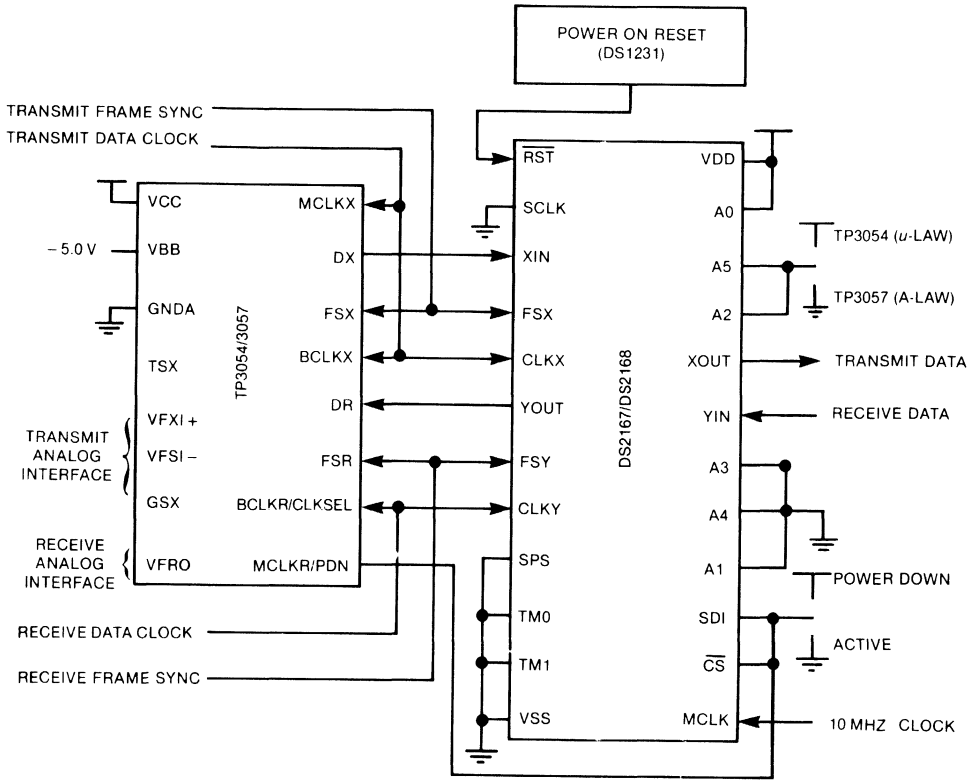
HARDWARE MODE
The hardware mode is intended for preliminary system prototyping or for applications which do not require the features of the serial port. Tying SPS to VSS disables the serial port, clears all internal registers and maps IPD, *u*/$\overline{A}$ and CP/$\overline{EX}$ of the X and Y side interfaces to the port and address inputs. Input and output timeslots for the X and Y side interfaces are fixed at 0. Such applications include, but are not limited to: 1) systems in which timeslot and algorithm are fixed, 2) stand-alone ADPCM combo applications, 3) "hardware" oriented systems where no host controller is available.

HARDWARE MODE Table 2

PIN #/NAME	REG. LOCATION	NAME AND DESCRIPTION
4/A0	CP/$\overline{EX}$ (X)	**Channel X coding** 0 = Expand 1 = Compress
6/A2	*u*/$\overline{A}$ (X)	**Channel X data format** 0 = A-law 1 = *u*-law
7/A3	CP/$\overline{EX}$ (Y)	**Channel Y coding** 0 = Expand 1 = Compress
9/A5	*u*/$\overline{A}$ (Y).2	**Channel Y data format** 0 = A-law 1 = *u*-law
18/SDI	IPD (Y)	**Y idle select** 0 = Channel active 1 = Channel idle
19/$\overline{CS}$	IPD (X)	**X idle select** 0 = Channel active 1 = Channel idle

NOTES:
1. SCLK, A1 and A4 must be tied to VSS when the hardware mode is selected.
2. When both X and Y sides are idled; the devices enter a stand-by mode which significantly reduces power consumption.
3. The DS2167 will power-up within 200 milliseconds after the X or Y side is reactivated (SDI and/or $\overline{CS}$ not equal to 0) from standby.
4. The DS2168 must be hardware reset when reactivated from stand-by. Power-up occurs immediately after the reset.

COMBO CODEC HARDWARE MODE INTERCONNECT Figure 2



NOTE:
1. TP3054/3057 are National Semiconductor combo-codecs.

SOFTWARE MODE
Tying SPS high enables the software mode. In this mode a host microcontroller writes configuration data to the DS2167/68 serial port via inputs SCLK, SDI and $\overline{CS}$. Independent control and timeslot registers establish operating characteristics for the X-side and Y-side PCM interfaces.

ADDRESS/COMMAND BYTE
In the software mode the address/command byte is the first byte written to the serial port; it identifies which of 64 possible ADPCM processors sharing the port wiring is to be updated. Address data must match that at inputs A0-A5. If no match occurs, the device ignores the following configuration data. If an address match occurs, the next three bytes written are accepted as control, input and output timeslot data. Bit ACB.6 determines which side (X or Y) of the device is to be updated.

CONTROL REGISTER
The control register establishes idle, algorithm reset, bypass, data format and channel coding for the selected PCM interface.

The X and Y side PCM interfaces may be independent disabled (output tri-stated) via IPD; when IPD is set for both X and Y interfaces, the device enters a low power stand-by mode. The DS2167 will power-up within 200 milliseconds after the X or Y side is reactivated (IPD = 0) from standby. The DS2168 requires an external hardware reset after IPD is cleared to "wake-up" from standby. The DS2168 will power-up immediately after the low-high transition on $\overline{RST}$.

ALRST resets the algorithm coefficients for the selected channel to their initial values. ALRST will be cleared by the device when the algorithm reset is complete.

The bypass feature is enabled when BYP is set and IPD is clear. During bypass, no expansion or compression of data occurs. This feature allows the user to interchange timeslots under control of the timeslot registers. Bypass operates on "byte-wide" slots when CP/$\overline{EX}$ = 1; on "nibble-wide" slots when CP/$\overline{EX}$ = 0.

A-law ($u/\overline{A}$ = 0) or u-law PCM ($u/\overline{A}$ = 1) coding is independently selected for the X and Y side interfaces by bit u/A. If BYP and IPD are clear, CP/$\overline{EX}$ determines if input data is to be compressed or expanded.

TIMESLOT ASSIGNMENT
On-chip counters establish when PCM data I/O occurs and are programmed via the timeslot registers. Timeslot size (4 or 8 bits wide) is determined by the state of CP/$\overline{EX}$. Timeslots are counted from the rising edge of FSX and FSY.

ADDRESS/COMMAND BYTE Figure 3

(MSB) (LSB)

—	X/$\overline{Y}$	A5	A4	A3	A2	A1	A0

2

SYMBOL	POSITION	NAME AND DESCRIPTION
—	ACB.7	Reserved, must be 0 for proper operation.
X/$\overline{Y}$	ACB.6	**X/$\overline{Y}$ Channel Select.** 0 = Update channel Y characteristics 1 = Update channel X characteristics
A5	ACB.5	**MSB of Device Address.**
A4	ACB.4	
A3	ACB.3	
A2	ACB.2	
A1	ACB.1	
A0	ACB.0	**LSB of Device Address.**

CONTROL REGISTER Figure 4

(MSB) (LSB)

—	—	IPD	ALRST	BYP	u/$\overline{A}$	—	CP/$\overline{EX}$

SYMBOL	POSITION	NAME AND DESCRIPTION
—	CR.7	Reserved, must be 0 for proper operation.
—	CR.6	Reserved, must be 0 for proper operation.
IPD	CR.5	**Idle and Power Down.** 0 = channel enabled 1 = channel disabled (output tri-stated)
ALRST	CR.4	**Algorithm Reset.** 0 = Normal operation 1 = Reset algorithm for selected channel
BYP	CR.3	**Bypass.** 0 = Normal operation 1 = Bypass selected channel
u/$\overline{A}$	CR.2	**Data Format.** 0 = A-law 1 = *u*-law
—	CR.1	Reserved, must be 0 for proper operation.
CP/$\overline{EX}$	CR.0	**Channel Coding.** 0 = Expand (decode) selected channel 1 = Compress (encode) selected channel

INPUT TIMESLOT REGISTER Figure 5

(MSB) (LSB)

—	—	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
—	ITR.7	Reserved, must be 0 for proper operation.
—	ITR.6	Reserved, must be 0 for proper operation.
D5	ITR.5	MSB of input timeslot word.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input timeslot word.

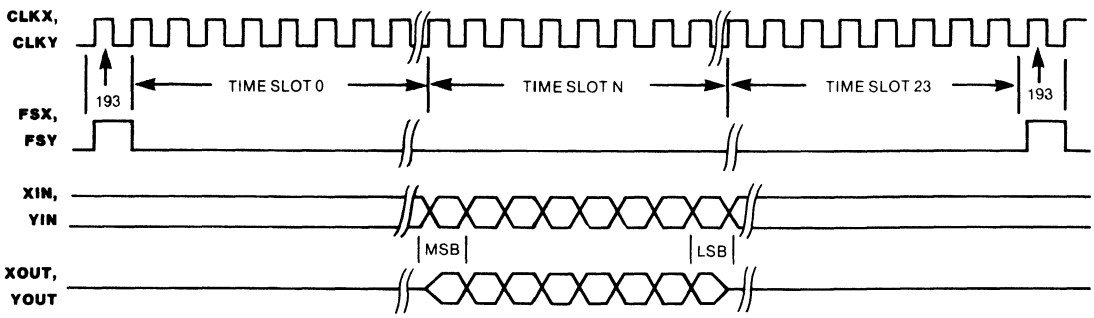
OUTPUT TIMESLOT REGISTER Figure 6

(MSB) (LSB)

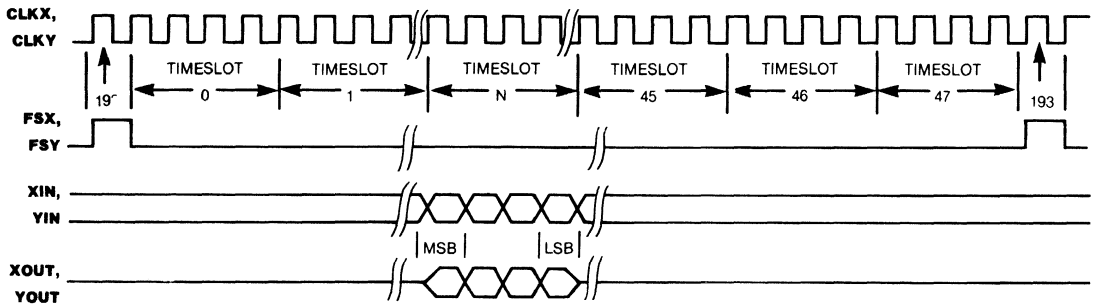
—	—	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
—	OTR.7	Reserved, must be 0 for proper operation.
—	OTR.6	Reserved, must be 0 for proper operation.
D5	OTR.5	MSB of output timeslot word.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output timeslot word.

PCM I/O TIMING (1.544 MHZ BACKPLANE) Figure 7



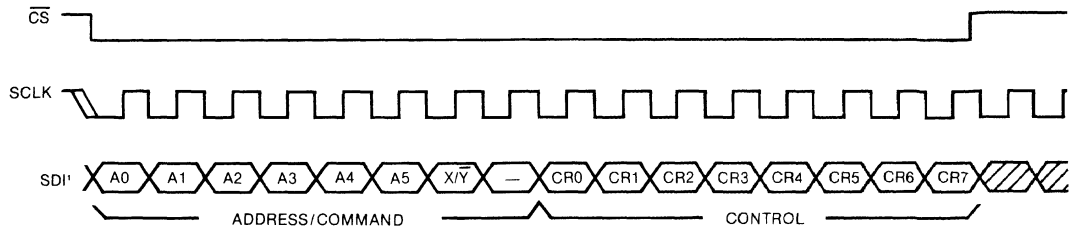
ADPCM I/O TIMING (1.544 MHZ BACKPLANE) Figure 8



SERIAL PORT WRITE

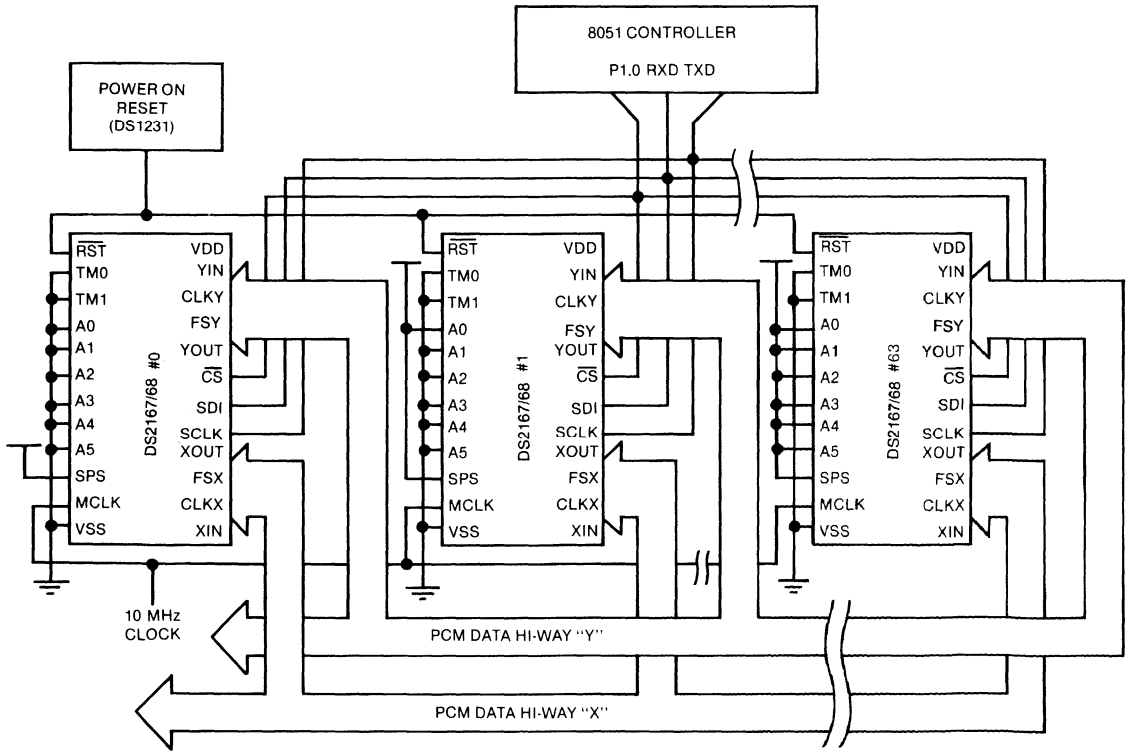
All port writes are initiated by driving $\overline{CS}$ low and terminated when $\overline{CS}$ returns high. *Data is sampled on the rising edge of SCLK and must be written to the device LSB first.* Writes to the device may be 2 bytes (address/command and control) or 4 bytes (address/command, control, input timeslot and output timeslot) in length. Writes should be terminated on byte boundaries to insure data integrity.

SERIAL PORT WRITE Figure 9



NOTES:
1. 2 byte write shown.

8051-BASED CONTROL SYSTEM Figure 10



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -1.0V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Soldering Temperature 260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		$V_{CC}+0.3$	V	
Logic 0	V_{IL}	−0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE ($t_A = 25$ °C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	10	pF	

D.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current (Active)	I_{DDA}		30		mA	1,2
Supply Current (Idle)	I_{DDPD}		1		mA	1,2,3
Input Leakage	I_{IL}	−1.0		+1.0	*u*A	
Output Leakage	I_{TRI}	−1.0		+1.0	*u*A	4
Output Current @2.4 V	I_{OH}	−1.0			mA	
Output Current @0.4 V	I_{OL}	4.0			mA	

NOTES:

1. CLKX = CLKY = 1.544 MHz; MCLK = 10 MHz.
2. Outputs open; inputs swinging full supply levels.
3. Both channels in idle mode.
4. XOUT and YOUT when tristated.

PCM INTERFACE
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	5
MCLK Pulse Width	t_{WMH}, t_{WML}	45	50	55	ns	
MCLK Rise and Fall Times	t_{RM}, t_{FM}		5	10	ns	
CLKX, CLKY Period	t_{PXY}	244	488	5208	ns	4
CLKX, CLKY Pulse Width	t_{WXYH}, t_{WXYL}	100	244		ns	
CLKX, CLKY Rise and Fall Times	t_{RXY}, t_{FXY}		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	t_{HOLD}	0			ns	1
Set-Up Time from FSX, FSY to CLKX, CLKY low	t_{SF}	50			ns	1
Hold Time from CLKX, CLKY low to FSX, FSY Low	t_{HF}	100			ns	1
XIN, YIN Set Up to CLKX, CLKY Low	t_{SD}	50			ns	1
XIN, YIN Hold to CLKX, CLKY Low	t_{HD}	50			ns	1
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	t_{DXYO}	10		150	ns	2
Delay Time from CLKX, CLKY to XOUT, YOUT Tristated	t_{DXYZ}	20		150	ns	1,2,3

NOTES:
1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8 V, and 10 ns maximum rise and fall times.
2. Load = 150 pF + 2 LSTTL loads.
3. For LSB of PCM byte or ADPCM nibble.
4. Maximum width of FSX, FSY is one CLKX, CLKY period.
5. MCLK = 10MHz ± 500ppm.

MASTER CLOCK/RESET
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{DD} = 5V ± 10%)

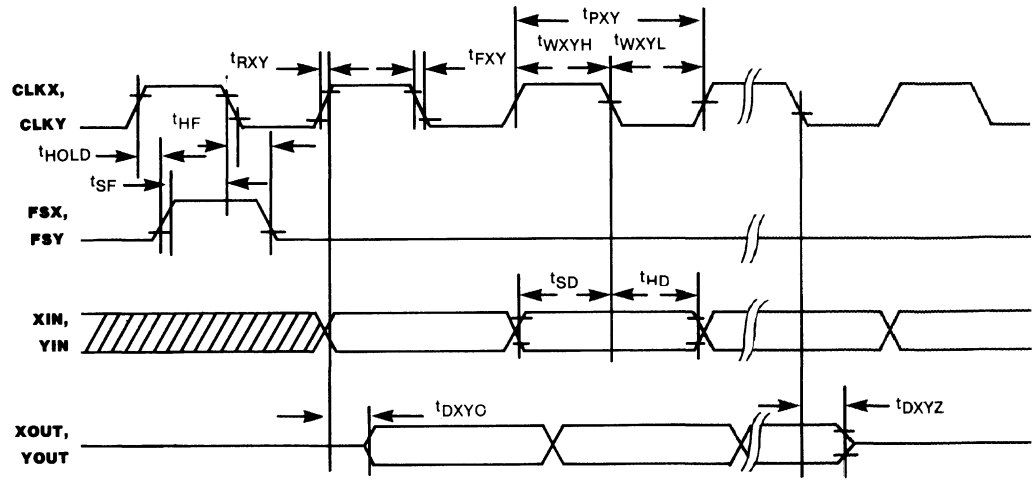
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	5
MCLK Pulse Width	t_{WMH}, t_{WML}	45	50	55	ns	
$\overline{RST}$ Pulse Width	t_{WRL}		1		ms	

SERIAL PORT
A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{DD} = 5V ± 10%)

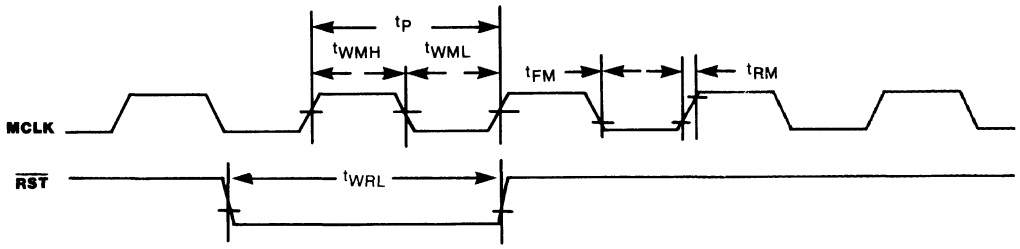
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Set Up	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Times	t_R, t_F			100	ns	1
$\overline{CS}$ to SCLK Set Up	t_{CC}	50			ns	1
SCLK to $\overline{CS}$ Hold	t_{CCH}	250			ns	1
$\overline{CS}$ Inactive Time	t_{CWH}	250			ns	1
SCLK Set Up to $\overline{CS}$ Falling	t_{SCC}	50			ns	1

NOTES:
1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times.
5. MCLK = 10MHz ± 500ppm.

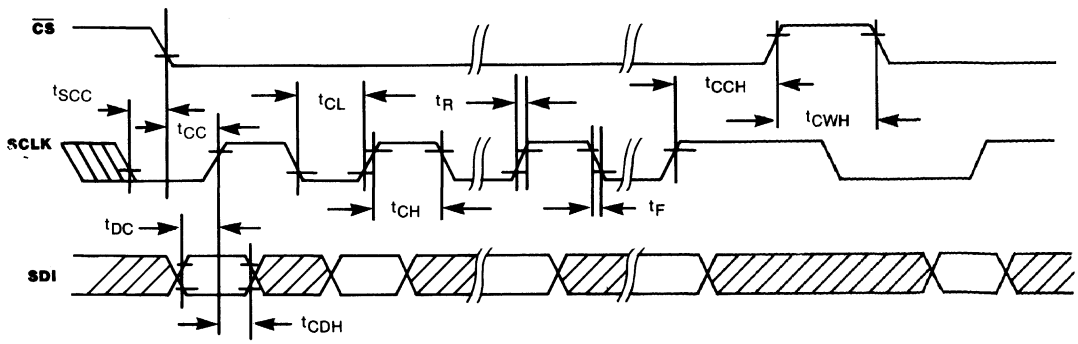
PCM INTERFACE A.C. TIMING DIAGRAM Figure 11



MASTER CLOCK/RESET A.C. TIMING DIAGRAM Figure 12

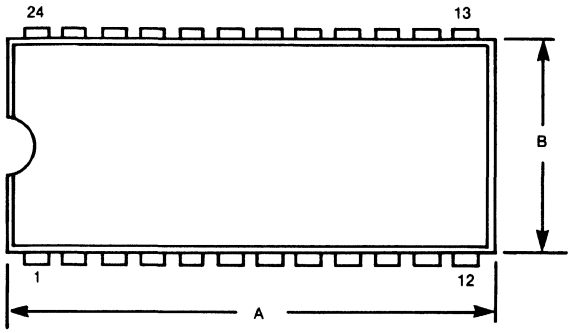


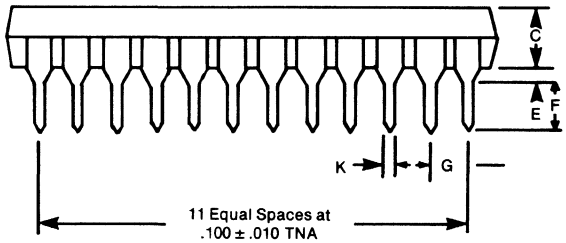
SERIAL PORT WRITE A.C. TIMING DIAGRAM Figure 13

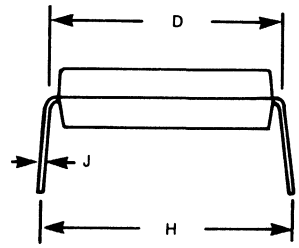


DS2167/68
ADPCM Processor

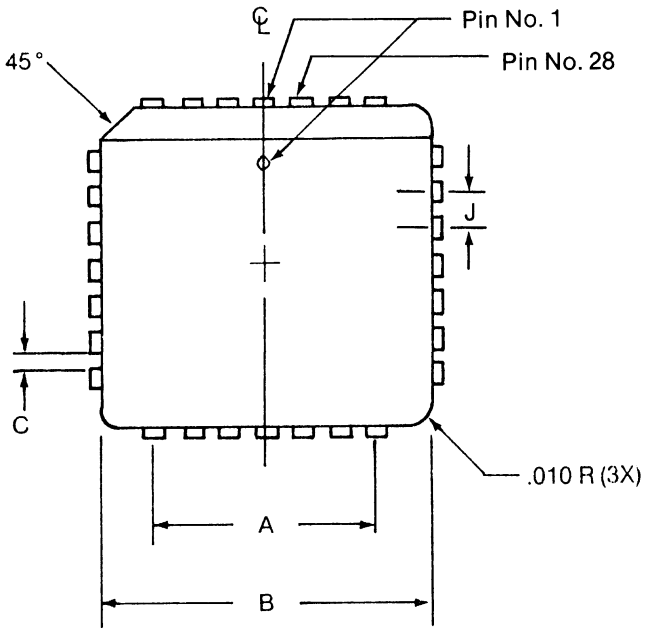
DIM.	INCHES	
	MIN.	MAX.
A	1.240	1.280
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

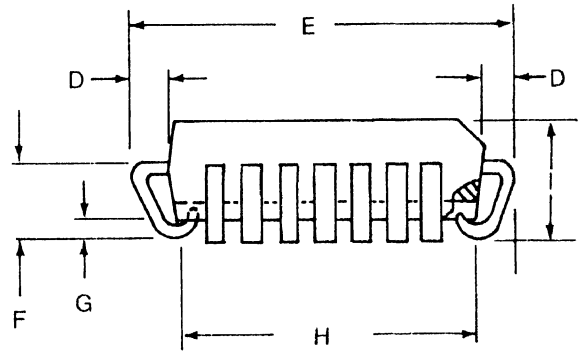


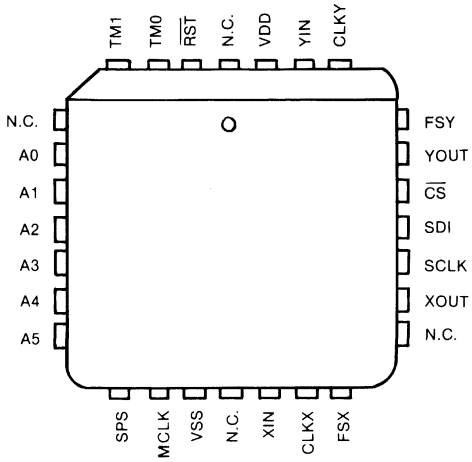




DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
J	.048	.052







VOICE/DATA ENCRYPTION

3

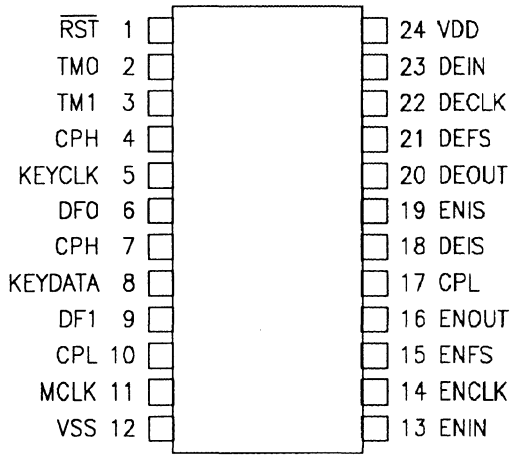
DALLAS SEMICONDUCTOR

DS2160
DES PROCESSOR

FEATURES

- Performs voice/data encryption and decryption according to the Data Encryption Standard (DES)
- Full duplex operation; one encrypt channel, one decrypt channel
- Each channel can process up to 64K bits per second
- Connects directly to combo-codec devices
- Simple key entry
- Uses Cipher Feedback Mode (CFB) of the DES standard
- Can encrypt/decrypt either 8 bits, 7 bits, 6 bits, or 4 bits
- Single +5V supply; low-power CMOS technology
- Available in 24-pin DIP and 28-pin PLCC

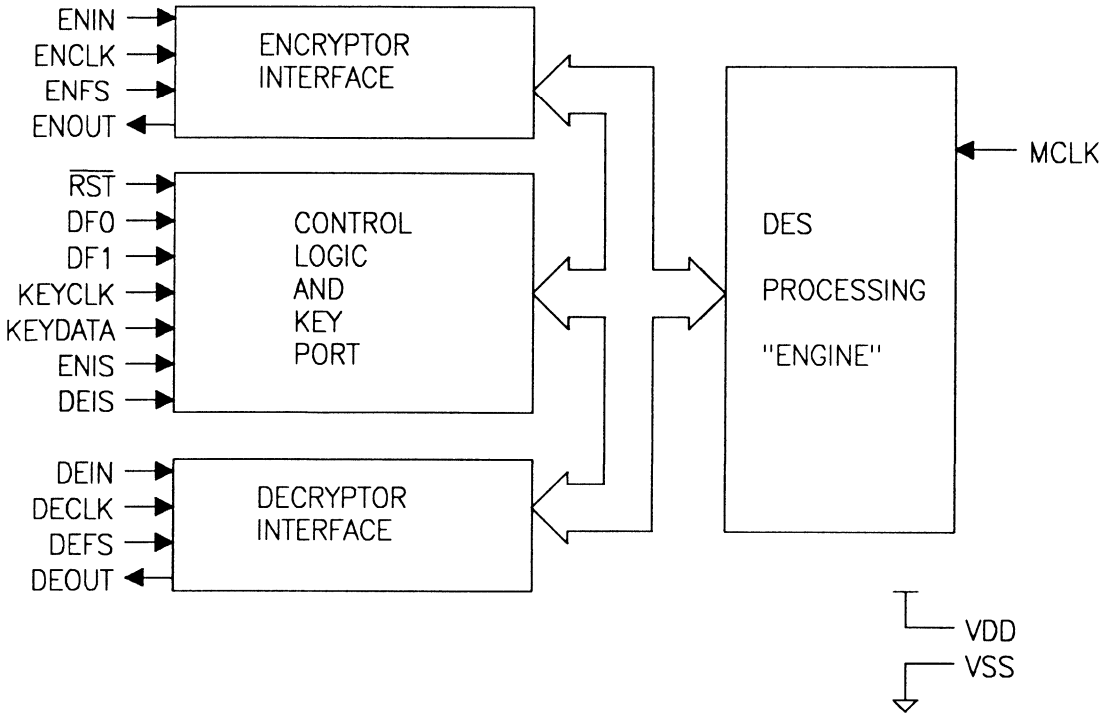
PIN CONNECTIONS



DESCRIPTION

The DS2160 is a dedicated Digital Signal Processing (DSP) CMOS chip optimized for the National Bureau of Standard's Data Encryption Standard (DES) algorithm. The DS2160 has two channels: one for encryption and one for decryption. The chip performs encipher/decipher operations on 64-bit words at a rate of up to 64K bits per second per channel. To provide security as specified in DES, a 64-bit key is necessary. The key is entered into the DS2160 through a simple serial port and cannot be accessed externally. The DES algorithm is used in both governmental and commercial applications where sensitive information is passed though unsecured media.

DS2160 BLOCK DIAGRAM Figure 1



3

PIN	SYMBOL	TYPE	DESCRIPTION
1	**RST**	I	**Reset.** A high-low transition resets the algorithm. The device should be reset on power-up.
2 3	**TMO** **TM1**	I	**Test Modes 0 and 1.** Tie to VSS for normal operation.
4	**CPH**	I	**Configure Pin High.** Tie to VDD for normal operation.
5	**KEYCLK**	I	**Key Clock.** Used in conjunction with the KEYDATA pin to enter the 64-bit DES key.
6	**DF0**	I	**Data Format 0.** Used in conjunction with the DF1 pin to select whether the device will encrypt/decrypt 8 bits, 7 bits, 6 bits, or 4 bits. See Table 2.
7	**CPH**	I	**Configure Pin High.** Tie to VDD for normal operation.
8	**KEYDATA**	I	**Key Data.** Used in conjunction with the KEYCLK pin to enter the 64-bit DES key.
9	**DF1**	I	**Data Format 1.** Used in conjunction with the DF0 pin to select whether the device will encrypt/decrypt 8 bits, 7 bits, 6 bits, or 4 bits. See Table 2.
10	**CPL**	I	**Configure Pin Low.** Tie to VSS for normal operation.
11	**MCLK**	I	**Master Clock.** 12MHz clock for the DES processing engine; may be asynchronous to ENCLK and DECLK.
12	**VSS**	-	**Signal Ground.** 0.0 volts.
13	**ENIN**	I	**Encrypt Channel Data Input.** Input PCM word is sampled on the first eight falling edges of ENCLK after the ENFS signal.
14	**ENCLK**	I	**Encrypt Channel Clock.** Data I/O clock for the encryption channel; must be tied to DECLK.
15	**ENFS**	I	**Encrypt Channel Frame Sync.** Frame sync for the encryption channel; must be tied to DEFS. A two ENCLK wide pulse here indicates a 64-bit word boundary.
16	**ENOUT**	O	**Encrypt Channel Data Output.** Updated on the first eight rising edges of ENCLK after the ENFS signal.
17	**CPL**	I	**Configure Pin Low.** Tie to VSS for normal operation.
18	**DEIS**	I	**Decrypt Channel Idle Select.** High state will idle the decryption channel causing the DEOUT pin to 3-state.

19	**ENIS**	i	**Encrypt Channel Idle Select.** High state will idle the encryption channel causing the ENOUT pin to 3-state.
20	**DEOUT**	0	**Decrypt Channel Data Output.** Updated on the first eight rising edges of DECLK after the DEFS signal.
21	**DEFS**	i	**Decrypt Channel Frame Sync.** Frame sync for the decryption channel; must be tied to ENFS. A two DECLK wide pulse here indicates a 64-bit word boundary.
22	**DECLK**	i	**Decrypt Channel Clock.** Data I/O clock fo the decryption channel; must be tied to ENCLK.
23	**DEIN**	i	**Decrypt Channel Data Input.** Input PCM word is sampled on the first eight edges of DECLK after the DEFS signal.
24	**VDD**	-	**Positive Supply.** 5.0 volts.

3

RESET AND CONTROL BITS

The RST pin must be held low for at least 1 millisecond on system power-up after the master clock (MCLK) is stable to insure proper initialization of the device. The control bits on the DS2160 (ENIS, DEIS, DF0, and DF1) can be changed without a reset being issued. If both ENIS and DEIS pins are tied high, then the DS2160 will enter a power-down state that consumes much less current. When either ENIS or DEIS is taken low, the DS2160 will exit the power-down condition in less than 200 milliseconds.

DATA FORMAT

The DS2160 has four separate data formats. The chip can be configured via the DF0 and DF1 pins to encrypt/decrypt either 4 bits, 6 bits, 7 bits, or 8 bits of the PCM word. (See Table 2). For example, if DF0 is strapped low and the DF1 pin is strapped high, then the DES processor will be in the 7-bit mode. In this mode, the encrypt channel of the processor will only encrypt the seven most significant bits of the PCM word that it receives, or in other words, the first seven bits of each 8-bit PCM word that it receives. The remaining bit, which is the least significant bit, will pass through the processor untouched. In the 7-bit mode, the decrypt channel knows that only the seven most significant bits are encrypted and it will decode the incoming encrypted PCM word accordingly. As with the encrypt channel, the LSB of the encrypted PCM word will pass though the decrypt channel unaffected.

DS2160 DATA FORMATS Table 2

Data Format	DF0 (pin 6)	DF1 (pin 9)
8-Bit	0	0
7-Bit	0	1
6-Bit	1	0
4-Bit	1	1

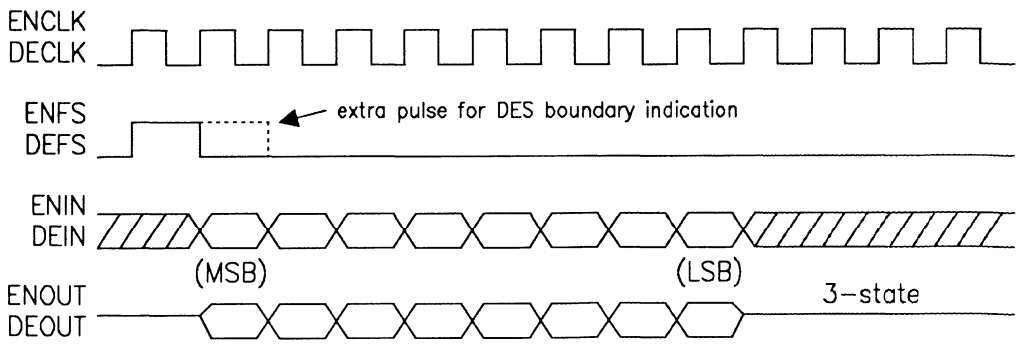
When bits are to pass through the DS2160 unaffected, the processor handles the transfer as follows:

1. The one, two, or four bits in each PCM word that are not to be touched are extracted.
2. Their bit positions are replaced by logical ones.
3. The encrypt/decrypt algorithm is performed.
4. The extracted bits are replaced into their original positions.

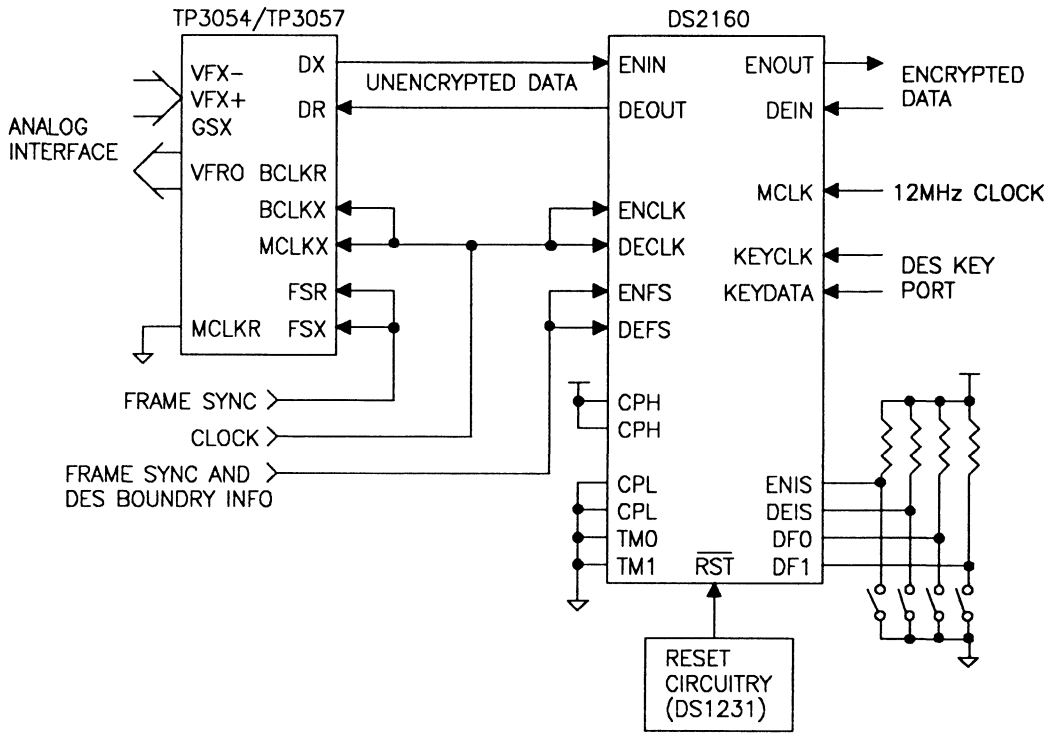
PCM INTERFACE

The DS2160 operates directly with a standard PCM type interface. (See Figure 2.) The processor samples the PCM data to be processed (encrypted or decrypted) on the first eight falling edges of ENCLK/DECLK after the ENFS/DEFS signal. All other data on ENIN and DEIN is ignored. The output of the encrypting or decrypting is placed on the ENOUT and DEOUT pins, respectively, on the first eight rising edges of ENCLK/DECLK after the ENFS/DEFS signal. The ENOUT and DEOUT pins are 3-stated except for the 8-bit period when they are outputting data. The I/O clocks ENCLK and DECLK on the DS2160 can operate at speeds from 256KHz to 4.096 MHz. The DS2160 interprets a two-bit wide frame sync pulse to indicate a DES word boundary. More on this issue is covered in the DES word synchronization section.

DS2160 PCM INTERFACE Figure 2



DS2160 CONNECTION TO COMBO CODEC Figure 3



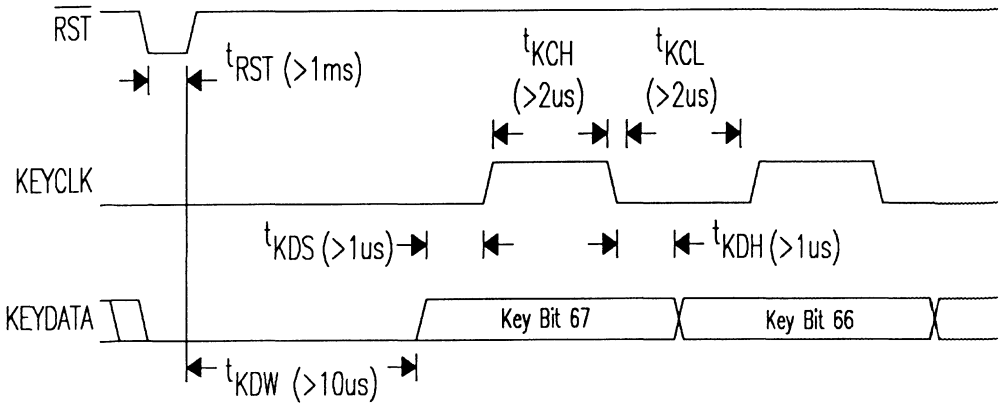
NOTE:
TP3054 and TP3057 are National Semiconductor Combo Codecs.

KEY MANAGEMENT

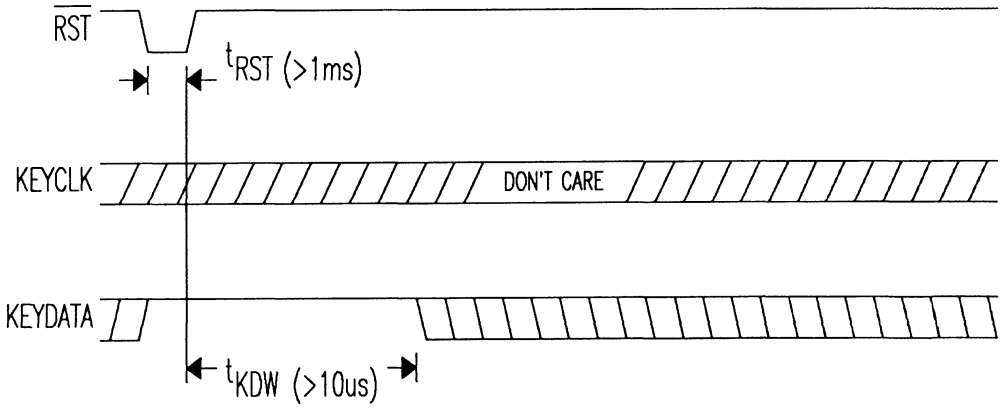
The 64-bit key (56 bits plus eight parity bits) is entered into the DS2160 through a simple two-pin serial port. Figure 4 details the operation of the DES key port. To enter a key into the DS2160, the KEYDATA pin must be held low during and after a Reset. Once the RST pin is returned high, then the key can begin to be entered after a wait time of at least 10 us. (NOTE: the DS2160 will wait indefinitely after a reset for a key to be entered.) After the wait period, data is clocked in using the KEYCLK pin. The key data has a minimum setup and hold time of 1 us and the key clock must be held high and low for at least 2 us. The DS2160 expects that 68 bits of data will be clocked in: the 64-bit key plus a leading 4 bit header that must be all zeros. The header is clocked in first, followed by the key. If a reset is to be issued, and the user wishes not to disturb to the key currently in the DS2160, then the KEYDATA pin must be held high during and after the reset. (See Figure 5.)

In order to maintain the highest level of security possible, the DES key cannot be accessed in any manner once it is clocked into the DS2160. Also, the key is not stored in the DS2160 in its original form.

DS2160 KEY ENTRY SEQUENCE Figure 4



RESET OF DS2160 WITHOUT DISTURBANCE OF THE DES KEY Figure 5

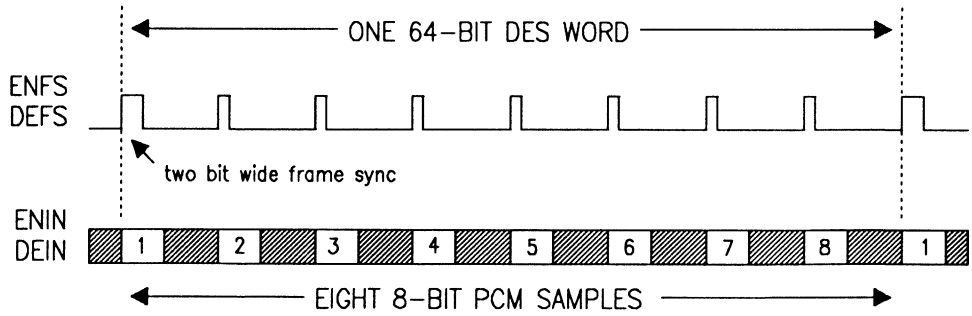


DES 64-BIT WORD BOUNDARY SYNCHRONIZATION

The DES algorithm encrypts/decrypts 64-bit words. In a DES system, it is necessary that the encryptor and decryptor realize where in a contiguous data stream the 64-bit words begin and end so that they can properly encode and decode the data. In the PCM environment in which the DS2160 operates, the data stream is made up of a continuing series of 8-bit samples. The DS2160 will combine eight consecutive PCM samples to create a single DES word.

In the DS2160, the user defines the boundaries of the 64-bit DES words via the ENFS and DEFS pins. The beginning of a 64-bit DES word are indicated by a frame sync pulse that is two bits wide instead of its normal width of one bit. When the DS2160 receives a two-bit wide frame sync pulse at ENFS and DEFS, it realizes that the next eight PCM words that it receives make up the 64-bit DES word. (See Figure 6.)

DS2160 DES WORD FRAMEWORK Figure 6



The DS2160 contains an internal counter that eliminates the need to have double-wide ENFS and DEFS signals every eighth frame. Hence, the wide frame sync pulse can be applied at any multiple of eight from zero to infinity.

DES SYNCHRONIZATION USING T1/CEPT MULTIFRAMES

If the DS2160 is used to encrypt voice or data that is to be transmitted over T1 or CEPT lines, the user can take advantage of an existing multiframe arrangement to provide the necessary synchronizaton of the 64-bit DES words between the encryptor and the decryptor. In T1, multiframes are made up of either 12 or 24 frames depending on whether the framing mode is Superframe (D4) or Extended Superframe (ESF), respectively. In CEPT environments, the multiframe is always made up of 16 frames. If each of these frames per multiframe numbers is multiplied by two, they become candidates for the indication of DES word boundaries needed by the DS2160 because they will be multiples of eight.

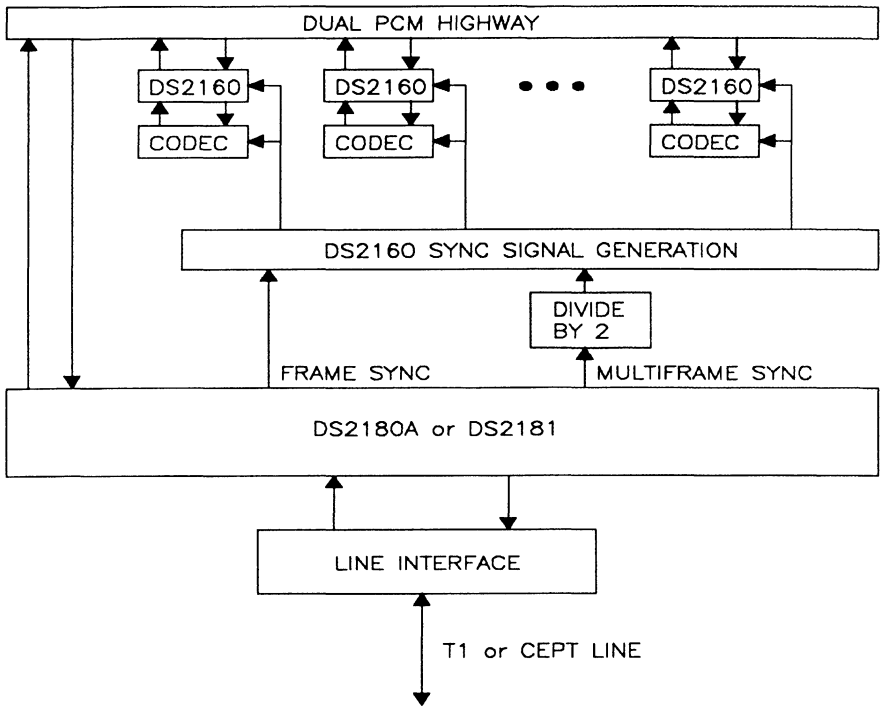
Figure 7 shows an arrangement that could use the existing multiframe scheme for DES synchronization. Either the DS2180A or DS2181 transceiver will synchronize to the T1 or CEPT data stream at both the multiframe and frame level. The frame sync signal is sent to a Time Slot Assignment Circuit (TSAC) where it will be moved in time to allow numerous DS2160s to connect to the same PCM highway. The multiframe signal is divided by two to create a signal that is a multiple of eight. This signal will be used to establish DES word boundaries on the DS2160. The output of the TSAC and the divide by two are combined to create a signal that will provide a one-bit wide frame sync pulse every frame, along with a two-bit wide frame sync pulse at some multiple of eight frames.

CIPHER FEEDBACK MODE

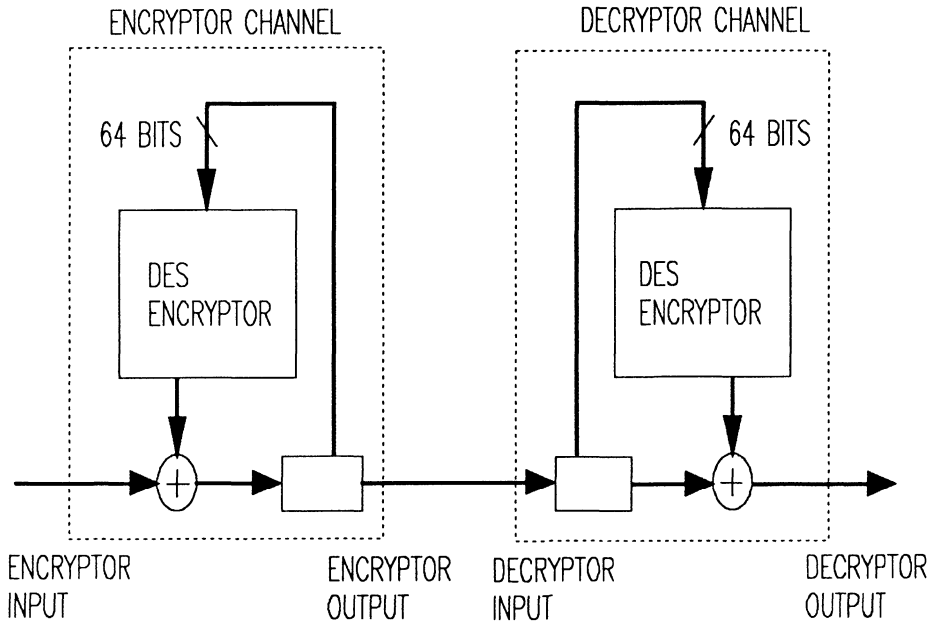
The DS2160 uses the Cipher Feedback Mode (CFB) as described by the Data Encryption Standard to encode and decode data. The CFB mode uses a DES encryptor to both encrypt and decrypt data. (See Figure 8.) Data is encrypted by logically exclusive-ORing the input data with the pseudorandom output of a DES encryptor. This XOR'ed output is the ciphered data and on the DS2160 it is output through the ENOUT pin. The XOR'ed output is also fed back to the DES encryptor where it serves as input to generate another pseudorandom bit code that will be XOR'ed with the next input sample.

To decode the ciphered data, the input 64-bit word is XOR'ed with the pseudorandom output of a DES encryptor. The ciphered input is also fed to the input of the DES encryptor where it serves at input to generate a pseudorandom bit code that will be used to decode the next ciphered input.

USE OF MULTIFRAME TO ESTABLISH DES SYNCHRONIZATION Figure 7



DS2160 CIPHER FEEDBACK MODE Figure 8



More information on CFB and the DES algorithm can be found in the Federal Information Processing Standards Publications or FIPS PUBs for short. The relevant documents are FIPS PUB 46-1, FIPS PUB 74, and FIPS PUB 81.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	VIH	2.0		VCC+0.3	V	
Logic 0	VIL	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{DDA}		30		mA	1, 2
Idle Supply Current	I_{DDPD}		1		mA	1, 2, 3
Input Leakage	I_I	-1.0		+1.0	uA	
Output Leakage	I_O	-1.0		+1.0	uA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES::

1. ENCLK = DECLK = 1.544MHz; MCLK = 12MHz
2. Outputs open; inputs swinging full supply levels
3. ENIS = DEIS = 5V
4. ENOUT and DEOUT are 3-stated

PCM INTERFACE

AC ELECTRICAL CHARACTERISTIC

(0°C to 70°C, V_{CC} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ENCLK, DECLK Period	t_{PED}	244		3906	ns	1
ENCLK, DECLK Pulse Width	t_{WEDL} t_{WEDH}	100			ns	
ENCLK, DECLK Rise Fall Times	t_{RED} t_{FED}		10	20	ns	
Hold Time from ENCLK, DECLK to ENFS, DEFS	t_{HOLD}	0			ns	2
SetUp Time from ENFS, DEFS high to ENCLK, DECLK low	t_{SF}	50			ns	2
Hold Time from ENCLK, DECLK low to ENFS, DEFS low	t_{HF}	100			ns	2
SetUp Time for ENIN, DEIN to ENCLK, DECLK low	t_{SD}	50			ns	2
Hold Time for ENIN, DEIN to ENCLK, DECLK low	t_{HD}	50			ns	2
Delay Time from ENCLK, DECLK to Valid ENOUT, DEOUT	t_{DEDO}	10		150	ns	3
Delay Time from ENCLK, DECLK to ENOUT, DEOUT 3-stated	t_{DEDZ}	20		150	ns	2, 3, 4

NOTES::

1. Maximum width of ENFS and DEFS is one ENCLK or DECLK period (except for frames where edge boundaries for the 64-bit DES words are defined).
2. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.
3. Load = 150pF + 2 LSTTL loads.
4. For LSB of PCM byte.

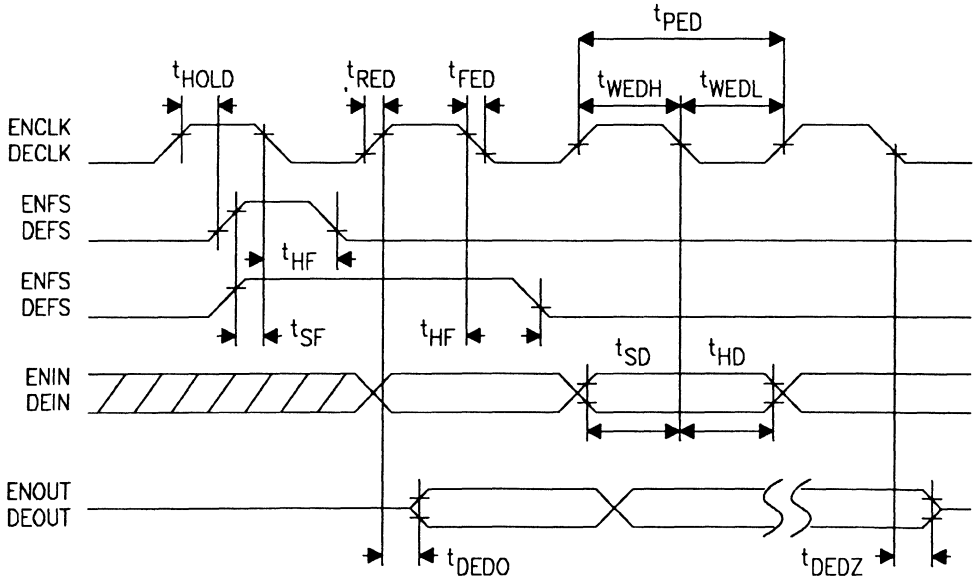
MASTER CLOCK/RESET
AC ELECTRICAL CHARACTERISTIC

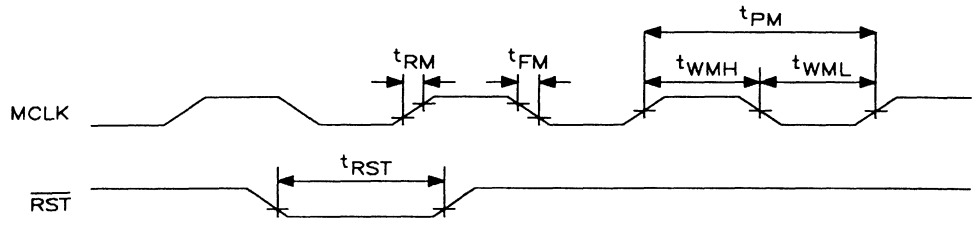
($0^{o}C$ to $70^{o}C$, V_{cc} = 5V+/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		83.3		ns	1
MCLK Pulse Width	t_{WMH} t_{WML}	33		50	ns	
MCLK Rise/ Fall Times	t_{RM} t_{FM}			10	ns	
RST Pulse Width	t_{RST}	1			ms	

NOTE:

1. MCLK = 12MHz +/- 500ppm





ELASTIC STORES

4

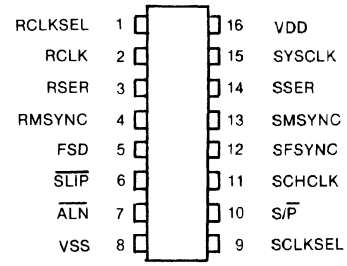
DALLAS SEMICONDUCTOR

DS2175
T1/CEPT ELASTIC STORE

FEATURES

- Rate buffer for T1 and CEPT transmission systems
- Synchronizes loop-timed and system-timed data streams on frame boundaries
- Ideal for T1 (1.544 MHz) to CEPT (2.048 MHz), CEPT to T1 interfaces
- Supports parallel and serial backplanes
- Buffer depth is 2 frames
- Comprehensive on-chip "slip" control logic
  - Slips occur only on frame boundaries
  - Outputs report slip occurrences and direction
  - Align feature allows buffer to be recentered at any time
  - Buffer depth easily monitored
- Compatible with DS2180A DS2181 CEPT Transceivers
- Industrial temperature range of −40° to +85°C available, designated DS2175N

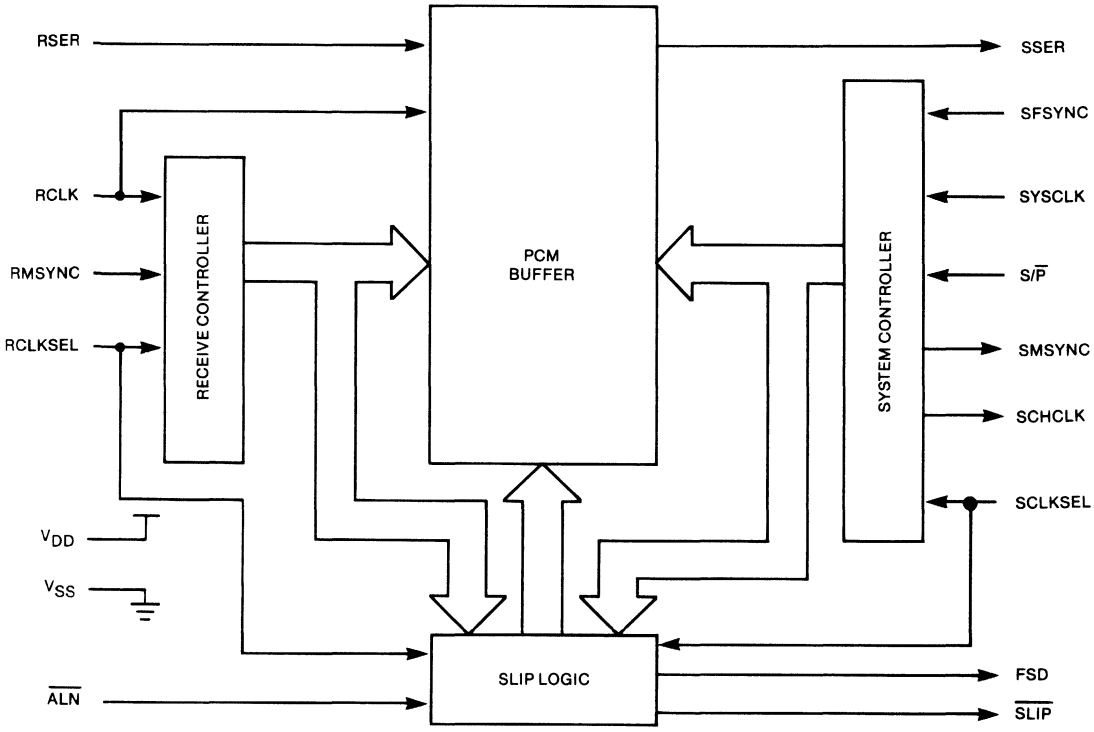
PIN CONNECTIONS



DESCRIPTION

The DS2175 is a low-power CMOS elastic-store memory optimized for use in primary rate telecommunications transmission equipment. The device serves as a synchronizing element between async data streams and is compatible with North American (T1—1.544 MHz) and European (CEPT—2.048 MHz) rate networks. The chip has several flexible operating modes which eliminate support logic and hardware currently required to interconnect parallel or serial TDM backplanes. Application areas include digital trunks, drop and insert equipment, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DS2175 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**RCLKSEL**	I	**Receive Clock Select.** Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
2	**RCLK**	I	**Receive Clock.** 1.544 or 2.048 MHz data clock.
3	**RSER**	I	**Receive Serial Data.** Sampled on falling edge of RCLK.
4	**RMSYNC**	I	**Receive Multiframe Sync.** Rising edge establishes receive side frame and multiframe boundaries.
5	**FSD**	O	**Frame Slip Direction.** State indicates direction of last slip; latched on slip occurrence.
6	**$\overline{\text{SLIP}}$**	O	**Frame Slip.** Active low, open collector output. Held low for 65 SYSCLK cycles when a slip occurs.
7	**$\overline{\text{ALN}}$**	I	**Align.** Recenters buffer on next system side frame boundary when forced low.
8	**VSS**	—	**Signal ground.** 0.0 volts.
9	**SCLKSEL**	I	**System Clock Select.** Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
10	**S/$\overline{\text{P}}$**	I	**Serial/Parallel Select.** Tie to VSS for parallel backplane applications, to VDD for serial.
11	**SCHCLK**	O	**System Channel Clock.** Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
12	**SFSYNC**	I	**System Frame Sync.** Rising edge establishes system side frame boundaries.
13	**SMSYNC**	O	**System Multiframe Sync.** Slip-compensated multiframe output; used with RMSYNC to monitor depth of store real time.
14	**SSER**	O	**System Serial Data.** Updated on rising edge of SYSCLK.
15	**SYSCLK**	I	**System Clock.** 1.544 or 2.048 MHz data clock.
16	**VDD**	—	**Positive Supply.** 5.0 volts.

PCM BUFFER
The DS2175 utilizes a 2-frame buffer to synchronize incoming PCM data to the system backplane clock. Buffer depth is mode-dependent; 2.048 MHz to 2.048 MHz applications utilize 64 bytes of buffer memory, while all other modes are supported by 48 bytes. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. The buffer depth is constantly monitored by on-board contention logic; a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

DATA FORMAT
Data is presented to, and output from, the elastic store in a "framed" format. A rising edge at RMSYNC and SFSYNC establishes frame boundaries for the receive and system sides. North American (T1) frames contain 24 data channels of 8 bits each and an F-bit (193 bits total). European (CEPT) frames contain 32 data channels (256 bits). The frame rate of both systems is 8 KHz. RMSYNC and SFSYNC do not require a pulse at every frame boundary; if desired, they may be pulsed once to establish frame alignment. Internal counters will then maintain the frame alignment and may be reinforced by the next rising edge at RMSYNC and/or SFSYNC.

SLIP CORRECTION CAPABILITY
The 2-frame buffer depth is adequate for T-carrier and CEPT applications where short term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2175 provides an ideal balance between total delay (less than 250 microseconds at its full depth) and slip correction capability.

BUFFER RECENTERING
Many applications require that the buffer be recentered during system power-up and/or initialization. Forcing $\overline{ALN}$ low recenters the buffer on the next rising edge of SFSYNC. A slip will occur during this recentering if the buffer depth is adjusted. If the depth is presently optimum, no adjustment (slip) occurs.

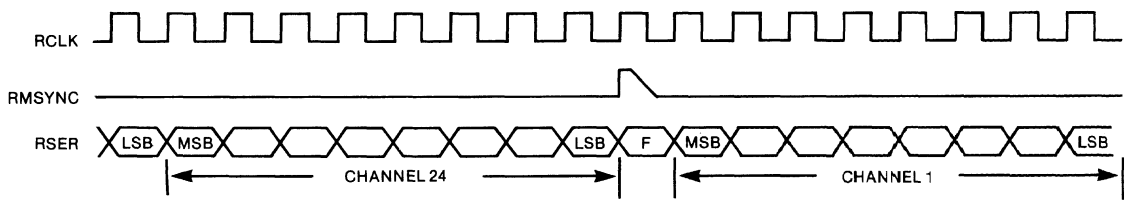
SLIP REPORTING
$\overline{SLIP}$ is held low for 65 SYSCLK cycles when a slip occurs. $\overline{SLIP}$ is an active-low, open-collector output. FSD indicates slip direction. When low (buffer empty) a frame of data was "repeated" at SSER during the previous slip. When high (buffer full), a frame of data was "deleted." FSD is updated at every slip occurrence.

BUFFER DEPTH MONITORING
SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges of RMSYNC and SMSYNC indicates the current buffer depth. Impending slip conditions may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK periods.

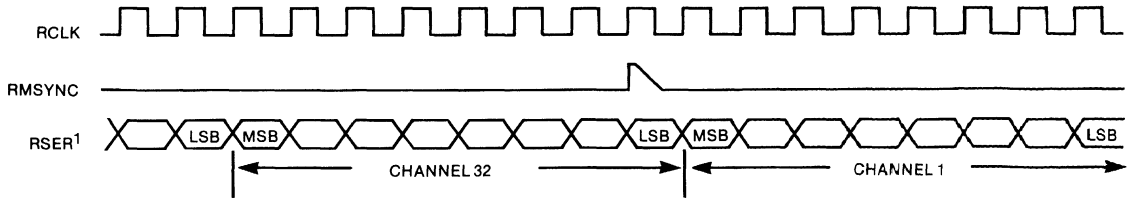
CLOCK SELECT
Receive and system side clock frequencies are independently selectable by inputs RCLKSEL and SCLKSEL. 1.544 MHz is selected when RCLKSEL (SCLKSEL) = 0; 2.048 MHz is selected when RCLKSEL (SCLKSEL) = 1. In 1.544 MHz (receive) to 1.544 MHz (system) applications, the F-bit position is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit position is forced to 1 in 2.048 MHz to 1.544 MHz applications. No F-bit position exists in 2.048 MHz system side applications.

PARALLEL COMPATIBILITY
The DS2175 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC (serial applications, S/$\overline{P}$ = 1). The device utilizes a look-ahead circuit in parallel applications (S/$\overline{P}$ = 0), and presents data 8 clocks early as shown in figures 4 and 5. Converting SSER to a parallel format requires an HC595 shift register.

RECEIVE SIDE TIMING (RCLK = 1.544 MHz) Figure 2

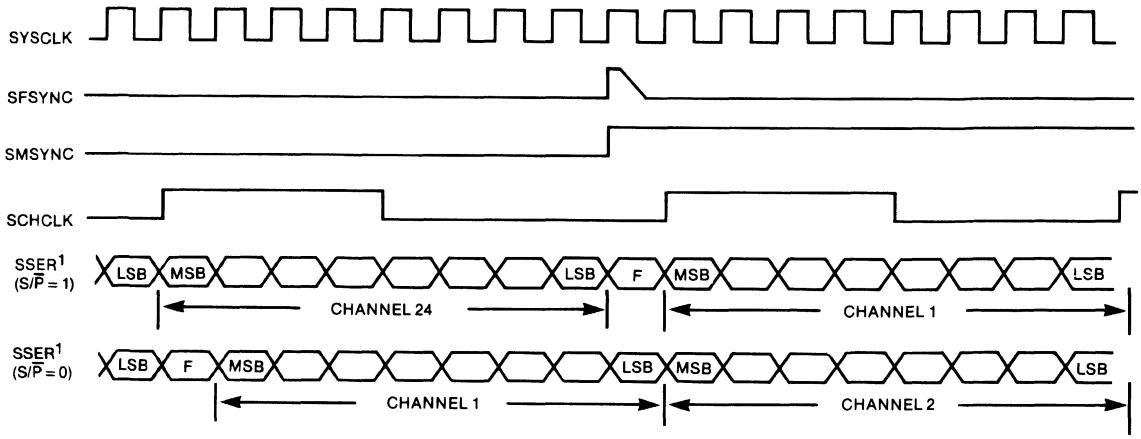


RECEIVE SIDE TIMING (RCLK = 2.048 MHz) Figure 3



NOTES:
1. All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1); Data in channels > 24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

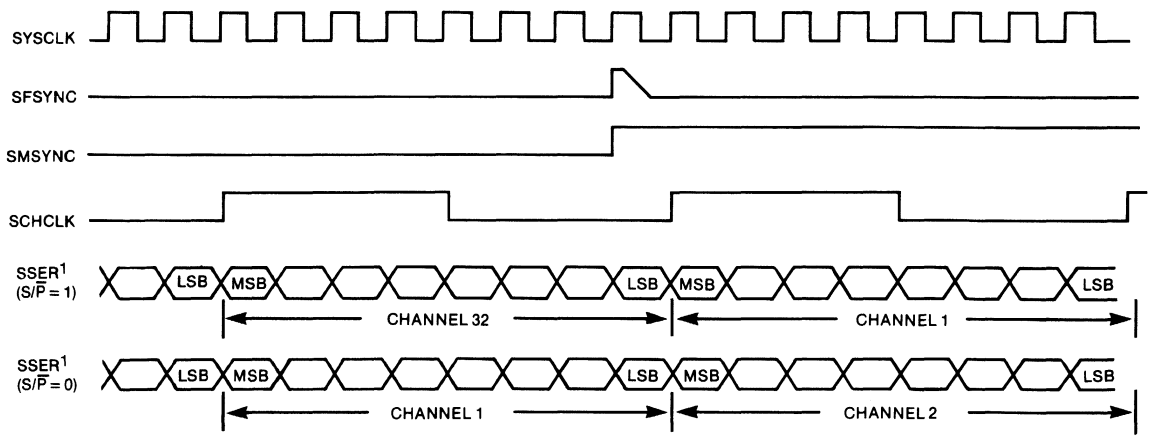
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHz) Figure 4



NOTES:

1. In 1.544 MHz receive side applications (RCLKSEL = 0), the F-bit position contains F-bit data extracted from the data stream at RSER. The F-bit position is forced to "1" in 2.048 MHz receive side applications (RCLKSEL = 1).

SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHz) Figure 5



NOTES:

1. All channel data is passed through the elastic store in 2.048 MHz system side applications (SCLKSEL = 1); Data in channels > 24 is ignored in 1.544 MHz system side applications (SCLKSEL = 0).

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground −1.0V to +7.0V
Operating Temperature 0 °C to 70 °C
Storage Temperature −55 °C to +125 °C
Soldering Temperature 260 °C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}	2.0		$V_{DD}+0.3$	V
Logic 0	V_{IL}	−0.3		+0.8	V
Supply	V_{DD}	4.5		5.5	V

CAPACITANCE ($t_A = 25$ °C)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	7	pF

D.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C $V_{DD} = 5V \pm 10\%$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		6		mA	1,2
Input Leakage	I_{IL}	−1.0		+1.0	uA	
Output Current @2.4V	I_{OH}	−1.0			mA	3
Output Current @0.4V	I_{OL}	+4.0			mA	4

NOTES:

1. SYSCLK = RCLK = 2.048 MHz
2. Outputs open
3. All outputs except $\overline{SLIP}$, which is open collector
4. All outputs

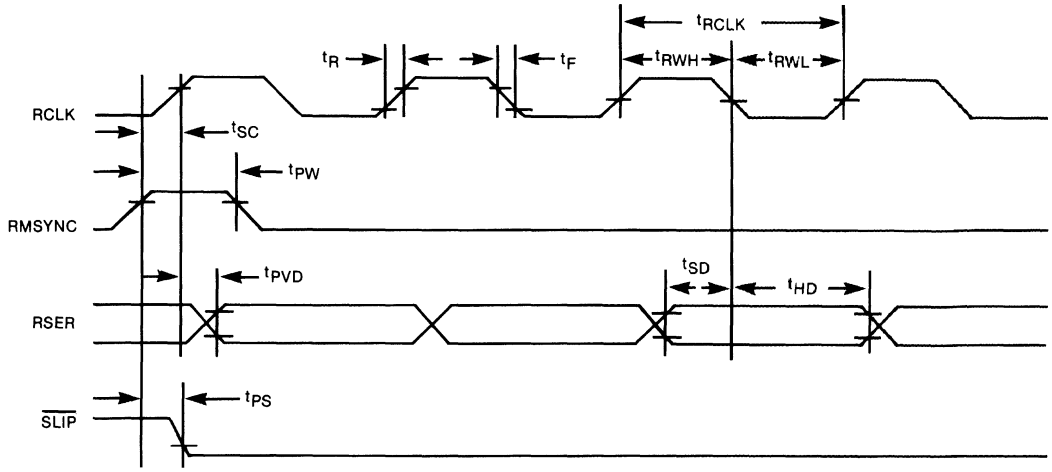
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	200			ns	
RCLK, SYSCLK Rise and Fall Times	t_R, t_F			20	ns	
RCLK Pulse Width	t_{RWH},t_{RWL}	100			ns	
SYSCLK Pulse Width	t_{SWH},t_{SWL}	100			ns	
SYSCLK Period	t_{SYSCLK}	200			ns	
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$		$+t_{RWL}/2$	ns	
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$		$+t_{SWL}/2$	ns	
RMSYNC, SFSYNC, $\overline{ALN}$ Pulse Width	t_{PW}	100			ns	
RSER Set Up to RCLK Falling	t_{SD}	50			ns	
RSER Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay SYSCLK to SSER	t_{PVD}			75	ns	
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to $\overline{SLIP}$ Low, FSD LOW/HIGH	t_{PS}			100	ns	
$\overline{ALN}$ Set Up to SFSYNC Rising	t_{SR}	500			ns	

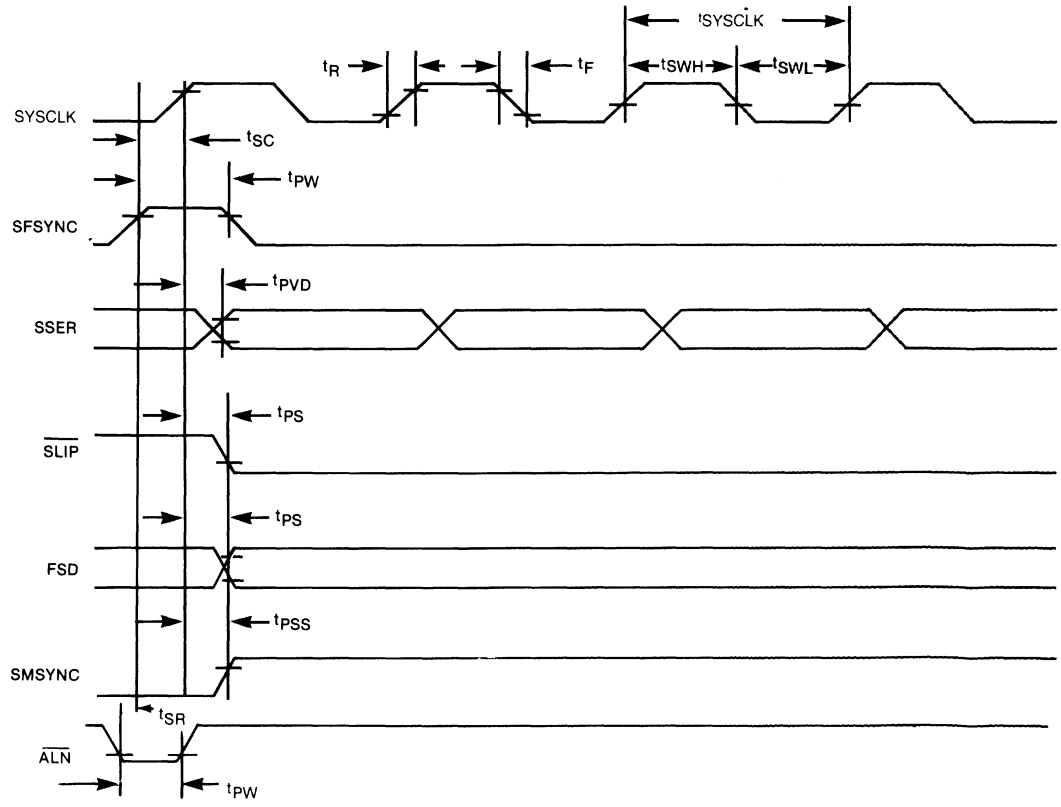
NOTES:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times
2. Output load capacitance = 100 pF

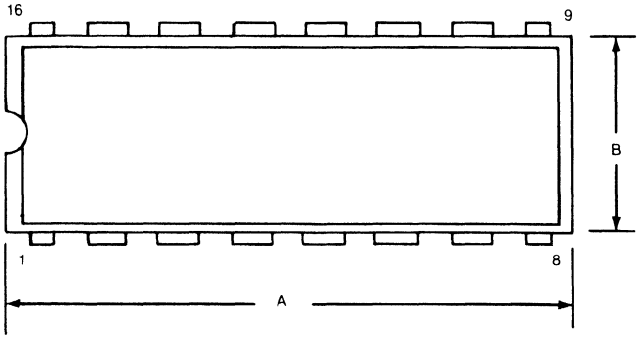
RECEIVE A.C. TIMING DIAGRAM Figure 6



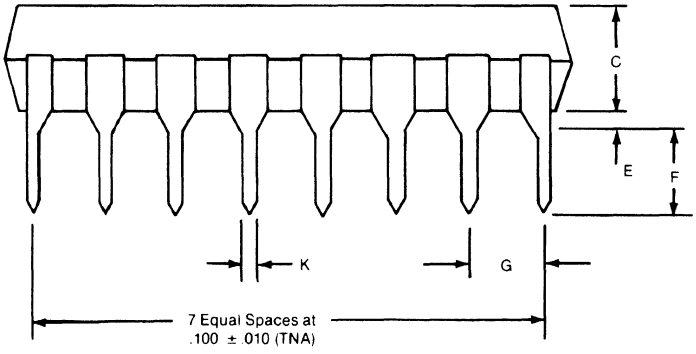
SYSTEM A.C. TIMING DIAGRAM Figure 7

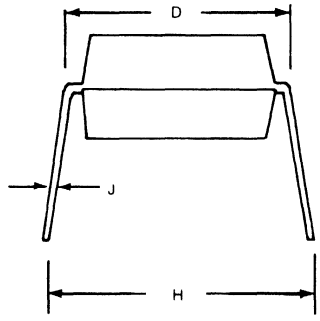


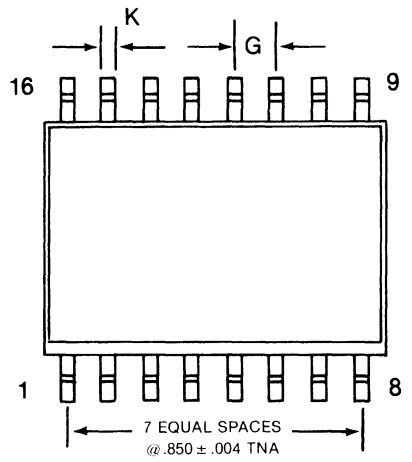
DS2175
T1/CEPT Elastic Store



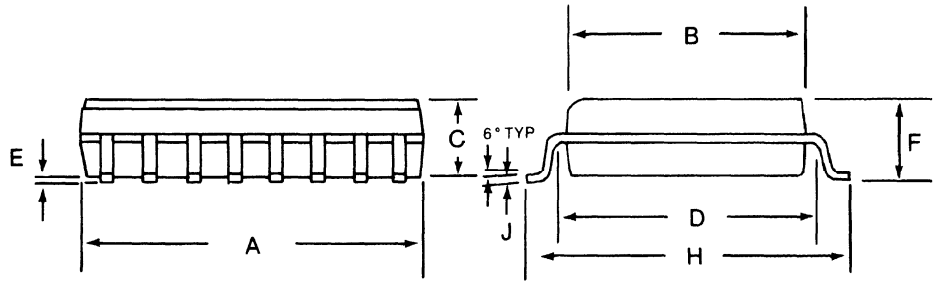
DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.300	.350
J	.008	.012
K	.015	.021







DIM.	INCHES	
	MIN.	MAX.
A	.403	.411
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



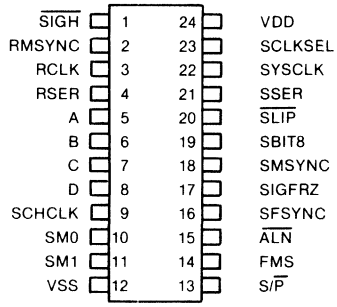
DALLAS SEMICONDUCTOR

DS2176
T1 RECEIVE BUFFER

FEATURES

- Synchronizes loop-timed and system-timed T1 data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signalling
- Inhibits signalling updates during alarm or slip conditions
- Integration feature "debounces" signalling
- Slip-compensated output indicates when signalling updates occur
- Compatible with DS2180A T1 Transceiver
- Surface mount package available, designated DS2176Q
- Industrial temperature range of −40°C to +85°C available, designated **DS2176N**

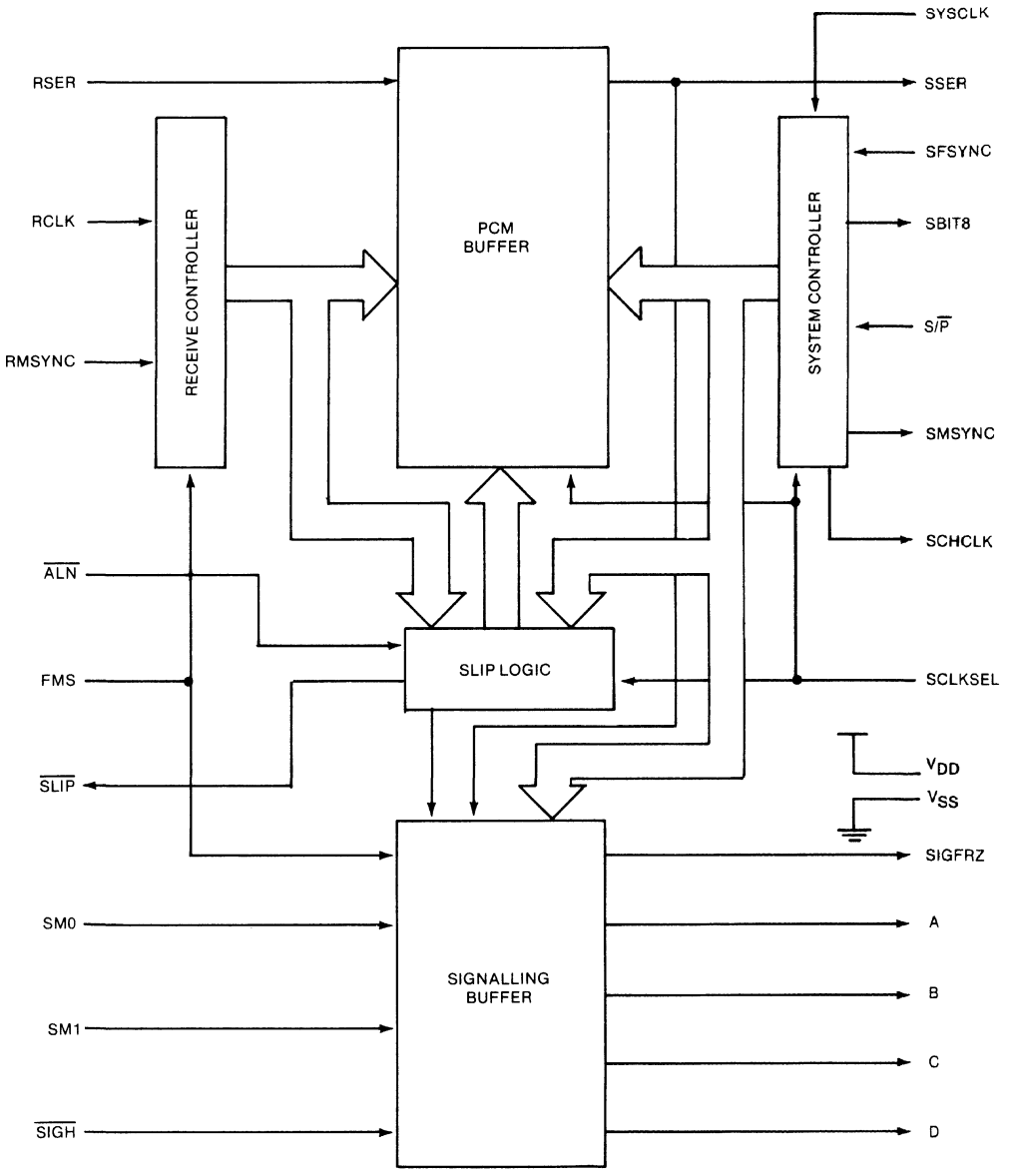
PIN CONNECTIONS



DESCRIPTION

The DS2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signalling; signalling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one "skinny" 24-lead package. Application areas include digital trunks, drop and insert equipment, transcoders, digital cross-connects (DACS), private network equipment and PABX-to-computer interfaces such as DMI and CPI.

DS2176 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

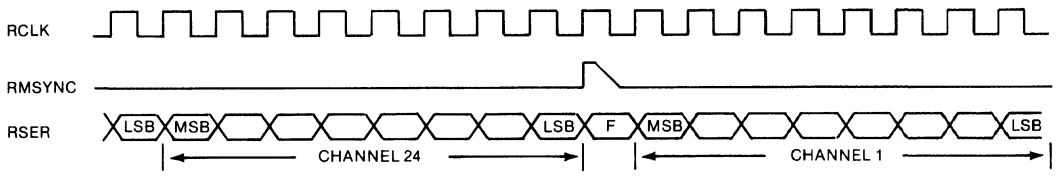
PIN	SYMBOL	TYPE	DESCRIPTION
1	$\overline{\text{SIGH}}$	I	**Signalling Inhibit.** When low, ABCD signalling updates are disabled for a period determined by SM0 and SM1, or until returned high.
2	RMSYNC	I	**Receive Multiframe Sync.** Must be pulsed high at multiframe boundaries to establish frame and multiframe alignment.
3	RCLK	I	**Receive Clock.** Primary 1.544 MHz clock.
4	RSER	I	**Receive Serial Data.** Sampled on falling edge of RCLK.
5 6 7 8	A B C D	O	**Robbed-Bit Signalling Outputs**
9	SCHCLK	O	**System Channel Clock.** Transitions high on channel boundaries; useful for serial to parallel conversion of channel data.
10 11	SM0 SM1	I	**Signalling Modes 0 and 1.** Select signalling supervision technique.
12	VSS	—	**Signal ground.** 0.0 volts.
13	S/$\overline{\text{P}}$	I	**Serial/Parallel Select.** Tie to VSS for parallel backplane applications, to VDD for serial.
14	FMS	I	**Frame Mode Select.** Tie to VSS to select 193S (D4) framing, to VDD for 193E (extended).
15	$\overline{\text{ALN}}$	I	**Align.** Recenters buffer on next system side frame boundary when forced low.
16	SFSYNC	I	**System Frame Sync.** Rising edge establishes start of frame.
17	SIGFRZ	O	**Signalling Freeze.** When high, indicates signalling updates have been disabled internally via a slip or externally by forcing $\overline{\text{SIGH}}$ low.
18	SMSYNC	O	**System Multiframe Sync.** Slip-compensated multiframe output; indicates when signalling updates are made.
19	SBIT8	O	**System Bit 8.** High during the LSB time of each channel. Used to reinsert extracted signalling into outgoing data stream.

20	$\overline{\text{SLIP}}$	O	**Frame Slip.** Active low, open collector output. Held low for 64 SYSCLK cycles when a slip occurs.
21	SSER	O	**System Serial Out.** Updated on rising edge of SYSCLK.
22	SYSCLK	I	**System Clock.** 1.544 or 2.048 MHz data clock.
23	SCLKSEL	I	**System Clock Select.** Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
24	VDD	—	**Positive Supply.** 5.0 volts.

OVERVIEW

The DS2176 performs two primary functions: 1) *synchronization* of received T1 PCM data (looped timed) to host backplane frequencies; 2) *supervision* of robbed-bit signalling data embedded in the data stream. The buffer, while optimized for use with the DS2180A T1 Transceiver, is also compatible with other transceiver devices. The DS2180A data sheet should serve as a valuable reference when designing with the DS2176.

RECEIVE SIDE TIMING Figure 2



DATA SYNCHRONIZATION

PCM BUFFER

The DS2176 utilizes a 2-frame buffer (386 bits) to synchronize incoming PCM data to the system backplane clock. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. A rising edge at RMSYNC establishes receive side frame and multiframe alignment. A rising edge at SFSYNC establishes system side frame alignment. The buffer depth is constantly monitored by on-board contention logic, a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

SLIP CORRECTION CAPABILITY

The 2-frame buffer depth is adequate for most T-carrier applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The DS2176 provides an ideal balance between total delay and slip correction capability.

BUFFER RECENTERING

$\overline{SLIP}$ is held low for 65 SYSCLK cycles when a slip occurs. $\overline{SLIP}$ is an active-low, open-collector output.

BUFFER DEPTH MONITORING

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC real time. SMSYNC is held high for 65 SYSCLK cycles.

CLOCK SELECT

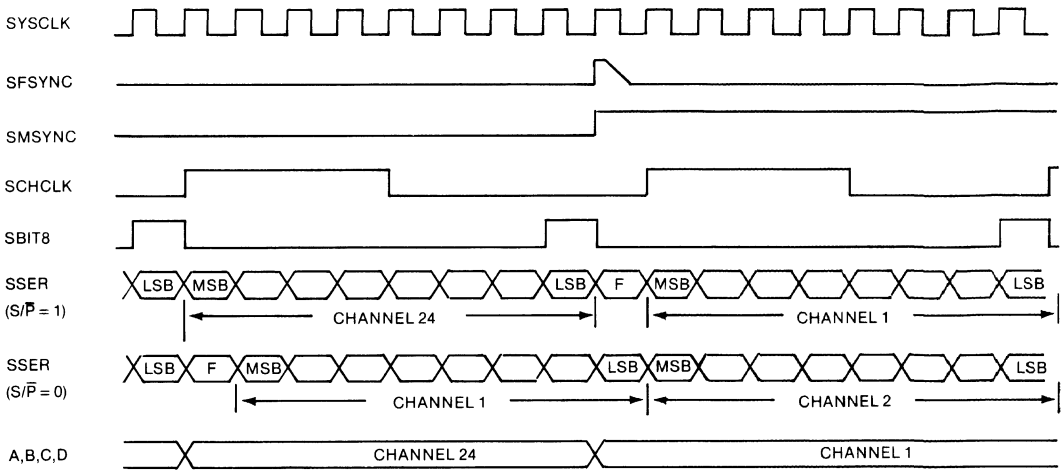
The device is compatible with 2 common backplane frequencies: 1.544 MHz, selected when SCLKSEL = 0; and 2.048 MHz, selected when SCLKSEL = 1. In 1.544 MHz applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit is dropped in 2.048 MHz applications and the MSB of channel 1 appears at SSER one bit period after a rising edge at SFSYNC. SSER is forced to 1 in all channels greater than 24. See figures 3 and 4.

In 2.048 MHz applications (SCLKSEL = 1), the PCM buffer control logic establishes slip criteria different from that used in 1.544 MHz applications to compensate for the faster system-side read frequency.

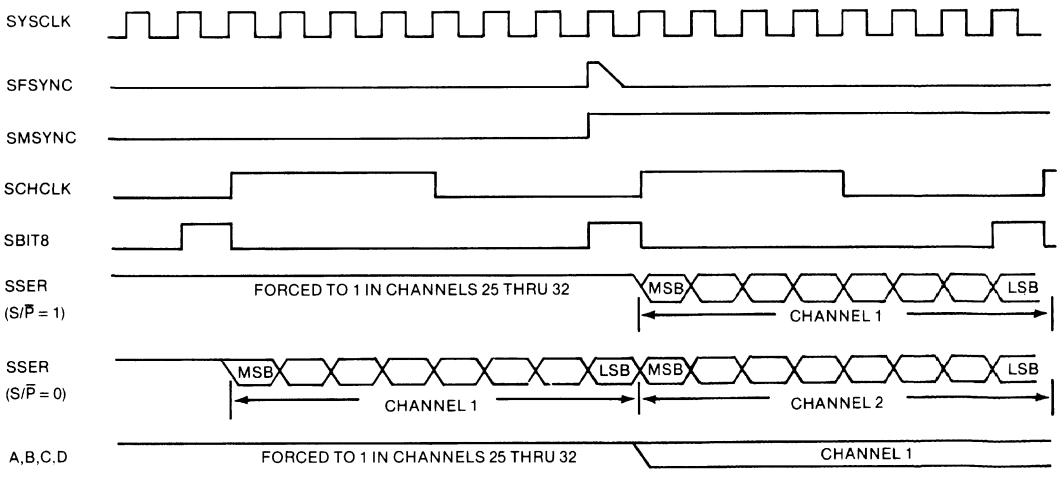
PARALLEL COMPATIBILITY

The DS2176 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC as shown in figures 3 and 4 (serial applications, $S/\overline{P} = 1$). The device utilizes a look-ahead circuit in parallel applications ($S/\overline{P} = 0$). Data is output 8 clocks earlier, allowing the user to parallel convert data externally.

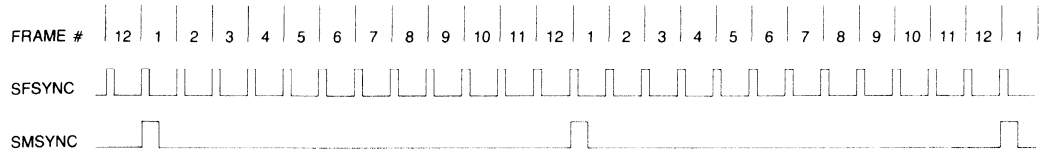
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 1.544 MHZ) Figure 3



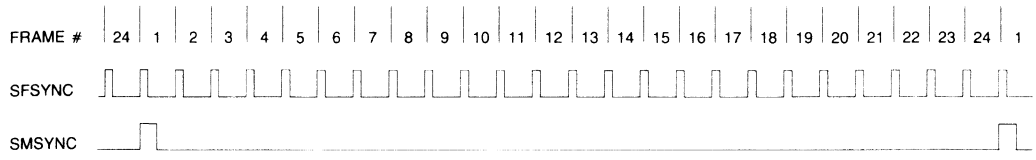
SYSTEM MULTIFRAME BOUNDARY TIMING (SYSCLK = 2.048 MHZ) Figure 4



193S SYSTEM MULTIFRAME TIMING Figure 5



193E SYSTEM MULTIFRAME TIMING Figure 6



SIGNALLING SUPERVISION

EXTRACTION

In digital channel banks, robbed-bit signalling data is inserted into the LSB position of each channel during signalling frames. In 193S framing (FMS = 0) applications, A signalling data is inserted into frame 6 and B signalling data is inserted into frame 12. 193E framing (FMS = 1) includes 2 additional signalling bits: C signalling is inserted into frame 18 and D signalling is inserted into frame 24. This embedded signalling data is synchronized to system side timing (via the PCM buffer) before being extracted and presented at outputs A,B,C and D. Outputs A,B,C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframe. In 193S applications, outputs C and D contain the previous multiframe's A and B data. Signalling updates occur once per multiframe at the rising edge of SMSYNC unless prohibited by a freeze.

FREEZE

The signalling buffer allows the DS2176 to "freeze" (prevent update of) signalling information during alarm or slip conditions. A slip condition or forcing $\overline{\text{SIGH}}$ low freezes signalling; duration of the freeze is dependent on SM0 and SM1. Updates will be unconditionally prohibited when $\overline{\text{SIGH}}$ is held low. During freezing conditions "old" data is recirculated in the output registers and appears at A,B,C and D. SIGFRZ is held high during the freeze condition, and returns low on the next signalling update. Input to output delay of signalling data is equal to 1 multiframe (the depth of the signalling buffer) + the current depth of the PCM buffer (1 frame ± approximately 1 frame).

INTEGRATION

Signalling integration is another feature of the DS2176; when selected, it minimizes the impact of random noise hits on the span and resultant robbed-bit signalling corruption. Integration requires that per-channel signalling data be in the same state for 2 or more multiframes before appearing at A,B,C and D. SM0 and SM1 are used to select the degree of integration or to totally bypass the feature. Integration is limited to 2 multiframes during slip or alarm conditions to minimize update delay.

CLEAR CHANNEL CONSIDERATIONS

The DS2176 does not merge the "processed" signalling information with outgoing PCM data at SSER; this assures integrity of data in clear channel applications. SBIT8 indicates the LSB position of each channel; when combined with off-chip support logic, it allows the user to selectively re-insert robbed-bit signalling data into the outgoing data stream.

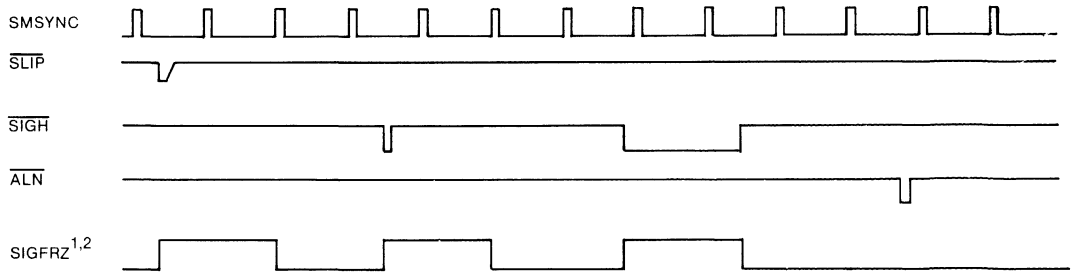
SIGNALLING SUPERVISION MODES Table 2

SM0	SM1	FMS	SELECTED MODE
0	0	0	193S framing, no integration, 1 multiframe freeze.
0	0	1	193E framing, no integration, 1 multiframe freeze.
0	1	0	193S framing, 2 multiframes integration and freeze.
0	1	1	193E framing, 2 multiframes integration and freeze.
1	0	0[1]	193S framing, 5 multiframes integration, 2 multiframes freeze.
1	0	1[1]	193E framing, 3 multiframes integration, 2 multiframes freeze.
1	1	0	Test mode.
1	1	1	Test mode.

NOTES:

1. During slip or alarm conditions, integration is limited to 2 multiframes to minimize signalling delay.

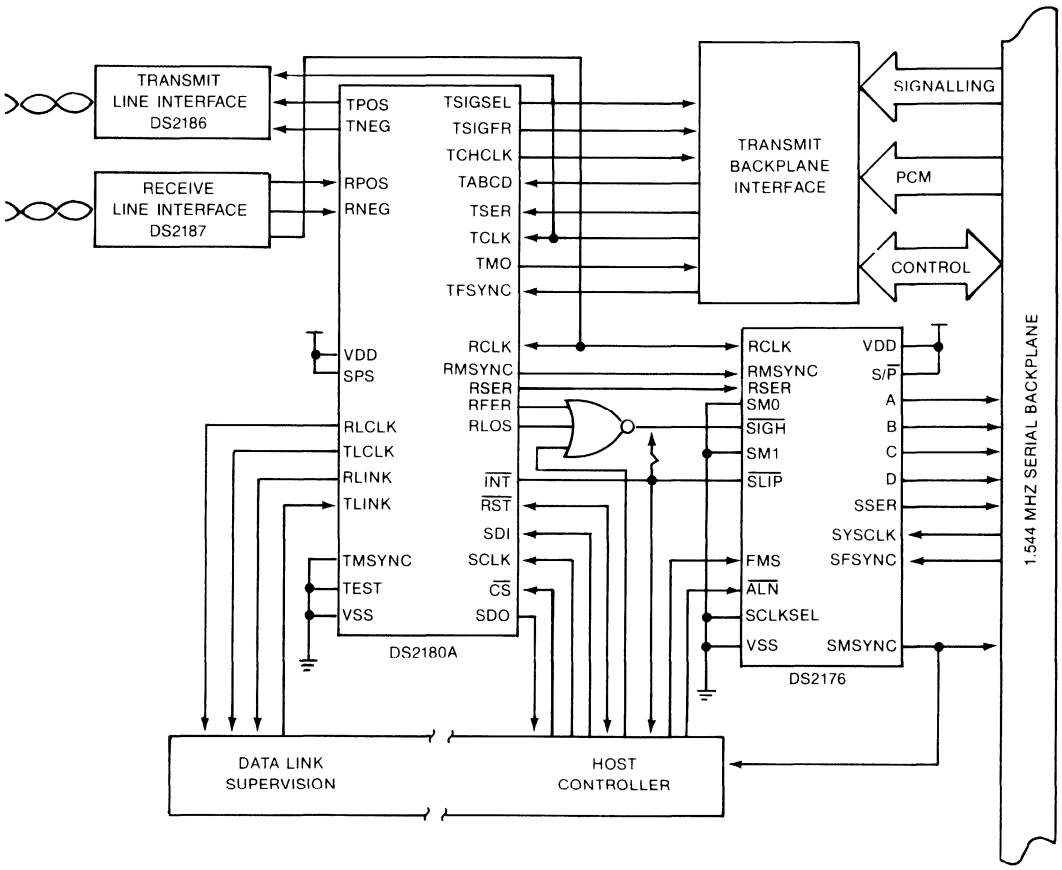
SLIP AND SIGNALLING SUPERVISION LOGIC TIMING Figure 7



NOTES:

1. Integration feature disabled (SM0 = SM1 = 0) in timing set shown.
2. Depending on present buffer depth, forcing $\overline{ALN}$ low may or may not cause a slip condition.

SERIAL 1.544 MHZ BACKPLANE INTERFACE Figure 8



DS2176/DS2180A SYSTEM APPLICATION

Figure 8 shows how the DS2180A T1 Transceiver and DS2176 Receive Buffer interconnect in a typical application.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground −1.0V to + 7.0V
Operating Temperature 0 °C to 70 °C
Storage Temperature −55 °C to +125 °C
Soldering Temperature 260 °C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD} + 0.3	V	
Logic 0	V_{IL}	− 0.3		+ 0.8	V	
Supply	V_{DD}	4.5		5.5	V	

D.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		6	10	mA	1,2
Input Leakage	I_{IL}	− 1.0		+ 1.0	uA	
Output Current @2.4V	I_{OH}	− 1.0			mA	3
Output Current @0.4V	I_{OL}	+ 4.0			mA	4
Output Leakage	I_{LO}	− 1.0		+ 1.0	uA	5

NOTES:

1. TCLK = RCLK = 1.544 MHz
2. Outputs open
3. All outputs except $\overline{SLIP}$, which is open collector
4. All outputs
5. Applies to $\overline{SLIP}$ when tri-stated

CAPACITANCE ($t_A = 25°C$)

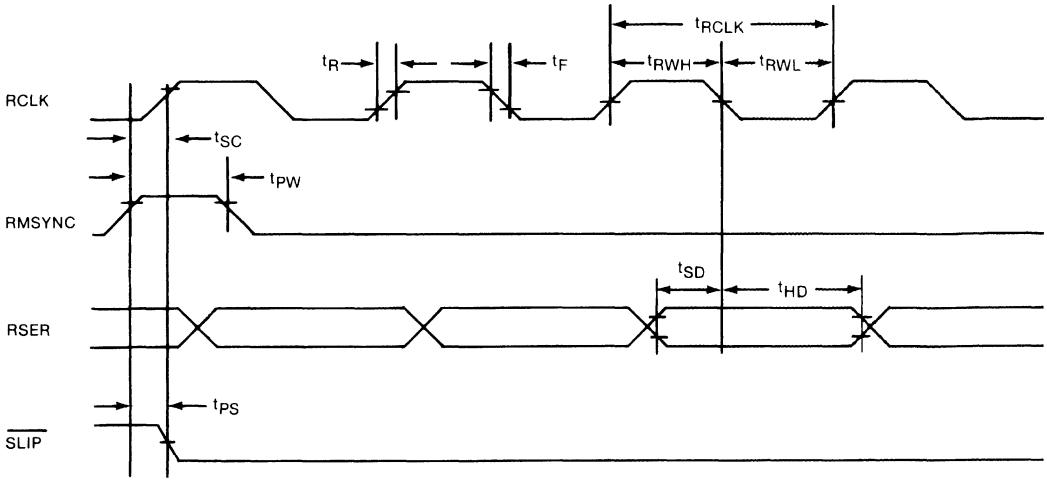
PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C, $V_{DD} = 5V \pm 10\%$)

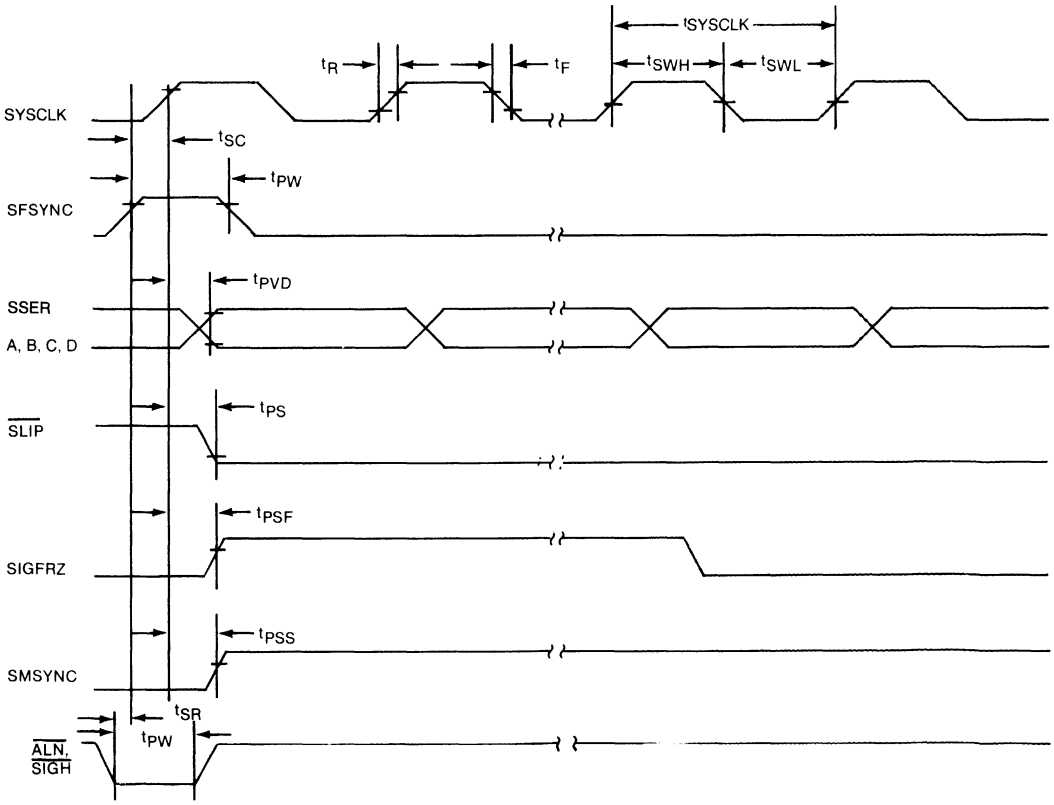
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	250	648		ns	
RCLK, SYSCLK Rise and Fall Times	t_R, t_F			20	ns	
RCLK Pulse Width	t_{RWH}, t_{RWL}	125	324		ns	
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100	244		ns	
SYSCLK Period	t_{SYSCLK}	200	488		ns	
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$		$+t_{RWL}/2$	ns	
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$		$+t_{SWL}/2$	ns	
RMSYNC, SFSYNC, $\overline{SIGH}$ $\overline{ALN}$ Pulse Width	t_{PW}	100			ns	
RSER Setup to RCLK Falling	t_{SD}	50			ns	
RSER Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay SYSCLK to $\overline{SSER}$, A,B,C,D	t_{PVD}			100	ns	
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns	
Propagation Delay SYSCLK or RCLK to $\overline{SLIP}$ Low	t_{PS}			100	ns	
Propagation Delay SYSCLK to SIGFRZ Low/High	t_{PSF}			75	ns	
$\overline{ALN}$, $\overline{SIGH}$ Setup to SFSYNC Rising	t_{SR}	500			ns	

NOTES:
1. Measured at $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, and 10 ns maximum rise and fall times.
2. Output load capacitance = 100 pF.

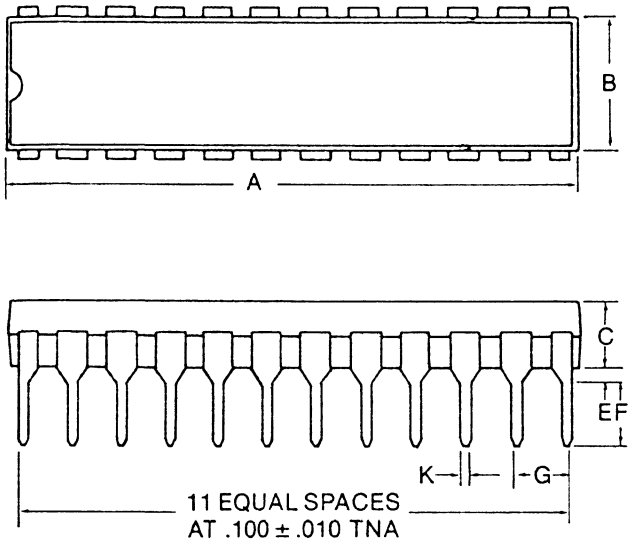
RECEIVE A.C. DIAGRAM Figure 9

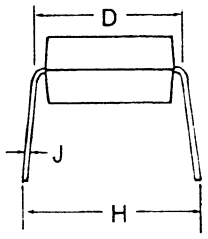


SYSTEM A.C. TIMING DIAGRAM Figure 10



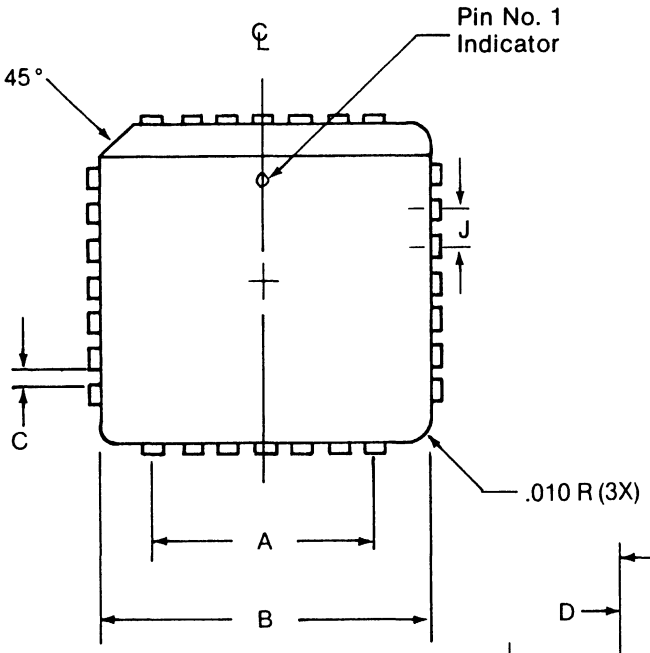
DS2176
T1 Receive Buffer



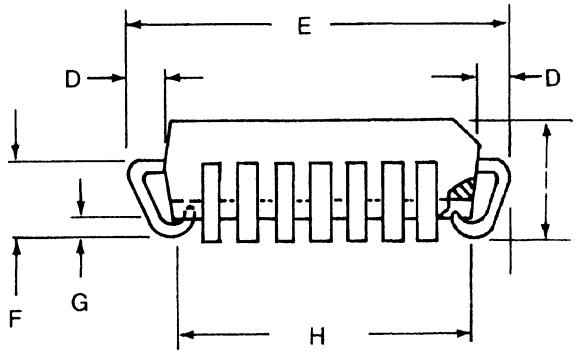


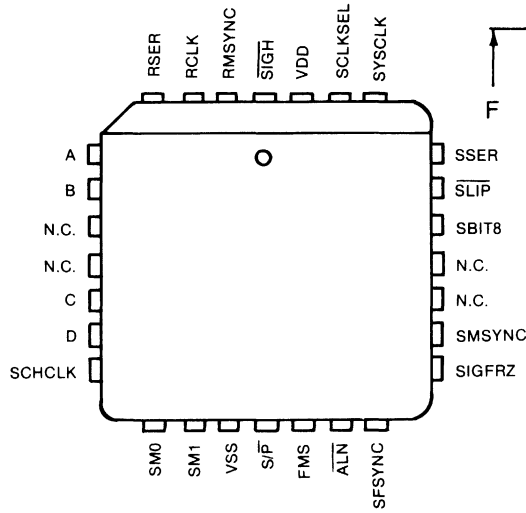
DIM.	INCHES	
	MIN.	MAX.
A	1.150	1.190
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.325	.375
J	.008	.012
K	.015	.021

4



DIM.	INCHES	
	MIN.	MAX.
A	1.240	1.260
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
I	.167	.173
J	.048	.052





TRANSCEIVERS/FRAMERS

5

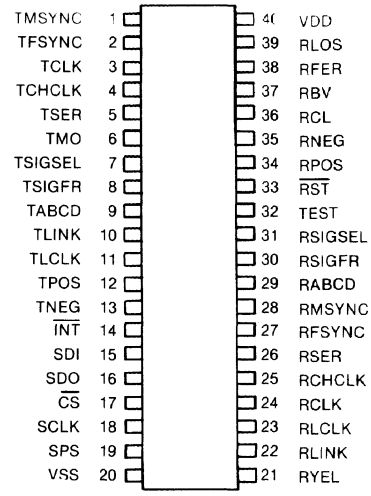
DALLAS SEMICONDUCTOR

DS2180A
T1 TRANSCEIVER

FEATURES

- Single chip DS1 rate transceiver
- Supports common framing standards
  - 12 frames/superframe "193S"
  - 24 frames/superframe "193E"
- Three zero suppression modes
  - B7 stuffing
  - B8ZS
  - Transparent
- Simple serial interface used for configuration, control and status monitoring in "processor" mode
- "Hardware" mode requires no host processor; intended for stand-alone applications
- Selectable 0, 2, 4, 16 state robbed bit signaling modes
- Allows mix of "clear" and "non-clear" DS0 channels on same DS1 link
- Alarm generation and detection
- Receive error detection and counting for transmission performance monitoring
- 5V supply, low power CMOS technology
- Surface mount package available, designated DS2180AQ
- Industrial temperature range of −40 °C to +85 °C available, designated DS2180AN or DS2180AQN

PIN CONNECTIONS



DESCRIPTION

The DS2180A is a monolithic CMOS device designed to implement primary rate (1.544 MHz) T-carrier transmission systems. The 193S framing mode is intended to support existing Ft/Fs applications (12 frames/superframe). The 193E framing mode supports the extended superframe format (24 frames/superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

Several functional blocks exist in the transceiver. The transmit framer/formatter generates appropriate framing bits, inserts robbed bit signaling, supervises zero suppression, generates alarms, and provides output clocks useful for data conditioning and decoding.

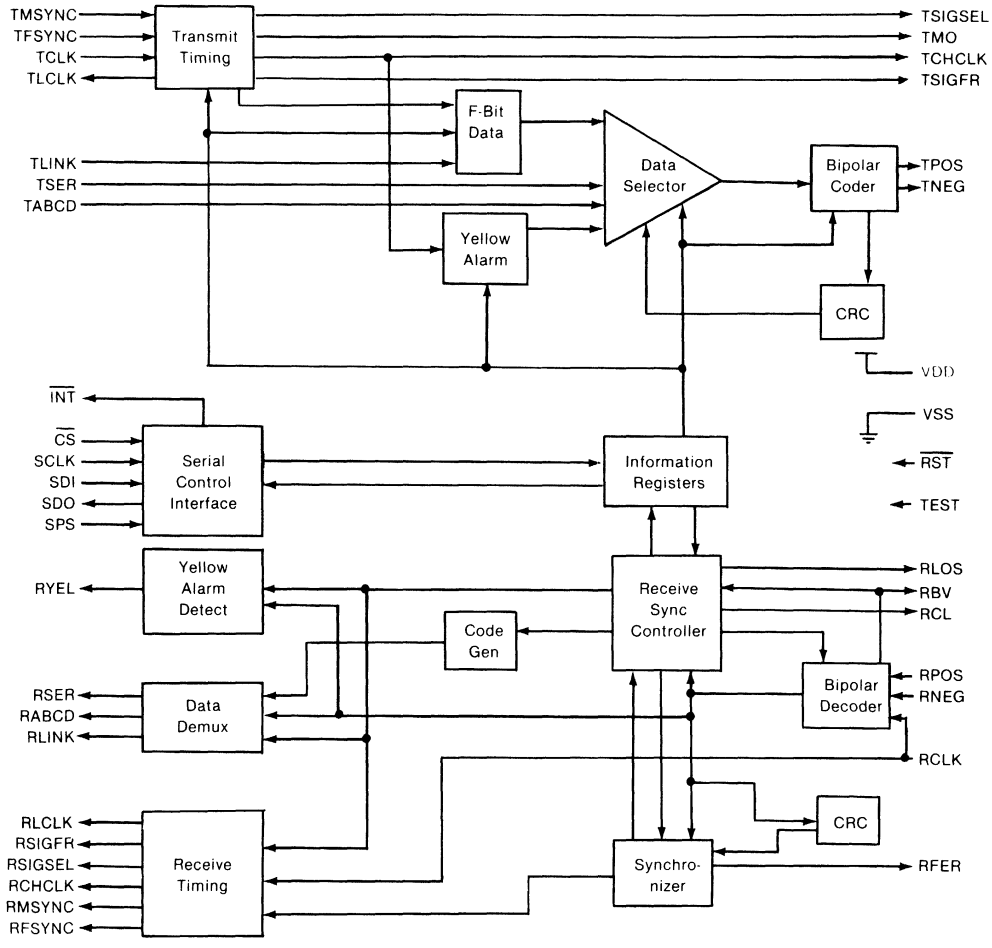
The receive synchronizer establishes frame and multiframe boundaries by identifying frame signaling bits, extracts signaling data, reports alarms and transmission errors, and provides output clocks useful for data conditioning and decoding.

The control block is shared between transmit and receive sides. This block determines the frame, zero suppression, alarm and signaling formats. User access to the control block is by one of two modes.

In the processor mode pins 14 through 18 are a microprocessor/microcontroller compatible serial port which can be used for device configuration, control and status monitoring.

In the hardware mode no offboard processor is required. Pins 14 through 18 are reconfigured into "hardwired" select pins. Features such as selective "clear" DS0 channels, insertion of idle code and alteration of sync algorithm are unavailable in the hardware mode.

DS2180A BLOCK DIAGRAM Figure 1



TRANSMIT PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**TMSYNC**	I	**Transmit Multiframe Sync.** May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows internal multiframe counter to free run.
2	**TFSYNC**	I	**Transmit Frame Sync.** Rising edge identifies frame boundary; may be pulsed every frame to reinforce internal frame counter, or tied low (allowing TMSYNC to establish frame and multiframe alignment).
3	**TCLK**	I	**Transmit Clock.** 1.544 MHz primary clock.
4	**TCHCLK**	O	**Transmit Channel Clock.** 192 KHz clock which identifies time slot (channel) boundaries. Useful for parallel to serial conversion of channel data.
5	**TSER**	I	**Transmit Serial Data.** NRZ data input, sampled on falling edge of TCLK.
6	**TMO**	O	**Transmit Multiframe Out.** Output of internal multiframe counter, indicates multiframe boundaries. 50% duty cycle.
7	**TSIGSEL**	O	**Transmit Signaling Select.** .667 KHz clock which identifies signaling frames A and C in 193E framing. 1.33 KHz clock in 193S.
8	**TSIGFR**	O	**Transmit Signaling Frame.** High during signaling frames, low otherwise.
9	**TABCD**	I	**Transmit ABCD Signaling.** When enabled via TCR.4, sampled during channel LSB time in signaling frames on falling edge of TCLK.
10	**TLINK**	I	**Transmit Link Data.** Sampled during the F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-Bit insertion).
11	**TLCLK**	O	**Transmit Link Clock.** 4 KHz demand clock for TLINK input.
12 13	**TPOS** **TNEG**	O	**Transmit Bipolar Data Outputs.** Updated on rising edge of TCLK.

PORT PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
14	$\overline{\text{INT}}$[1]	O	**Receive Alarm Interrupt.** Flags host controller during alarm conditions. Active low, open drain output.
15	SDI[1]	I	**Serial Data In.** Data for on-board registers. Sampled on rising edge of SCLK.
16	SDO[1]	O	**Serial Data Out.** Control and status information from on-board registers. Updated on falling edge of SCLK, tri-stated during serial port write or when $\overline{\text{CS}}$ is high.
17	$\overline{\text{CS}}$[1]	I	**Chip Select.** Must be low to write or read the serial port.
18	SCLK[1]	I	**Serial Data Clock.** Used to write or read the serial port registers.
19	SPS	I	**Serial Port Select.** Tie to VDD to select serial port. Tie to VSS to select hardware mode.
NOTES: 1. Multifunction pins, see hardware mode description.			

5

POWER AND TEST PIN DESCRIPTION Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
20	VSS	-	**Signal Ground.** 0.0 volts.
32	TEST	I	**Test Mode.** Tie to VSS for normal operation.
40	VDD	-	**Positive Supply.** 5.0 volts.

RECEIVE PIN DESCRIPTION Table 4

PIN	SYMBOL	TYPE	DESCRIPTION
21	**RYEL**	O	**Receive Yellow Alarm.** Transitions high when yellow alarm detected, goes low when alarm clears.
22	**RLINK**	O	**Receive Link Data.** Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	**RLCLK**	O	**Receive Link Clock.** 4 KHz demand clock for RLINK.
24	**RCLK**	I	**Receive Clock.** 1.544 MHz primary clock.
25	**RCHCLK**	O	**Receive Channel Clock.** 192 KHz clock, identifies time slot (channel) boundaries.
26	**RSER**	O	**Receive Serial Data.** Received NRZ serial data, updated on rising edges of RCLK.
27	**RFSYNC**	O	**Receive Frame Sync.** Extracted 8 KHz clock, one RCLK wide, indicates F-Bit position in each frame.
28	**RMSYNC**	O	**Receive Multiframe Sync.** Extracted multiframe sync; edge indicates start of multiframe, 50% duty cycle.
29	**RABCD**	O	**Receive ABCD Signaling.** Extracted signaling data output, valid for each channel time in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
30	**RSIGFR**	O	**Receive Signaling Frame.** High during signaling frames, low during resync and non-signaling frames.
31	**RSIGSEL**	O	**Receive Signaling Select.** In 193E framing a .667 KHz clock which identifies signaling frames A and C. A 1.33 KHz clock in 193S.
33	**$\overline{\text{RST}}$**	I	**Reset.** A high-low transition clears all internal registers and resets receive side counters. A high-low-high transition will initiate a receive resync.
34 35	**RPOS** **RNEG**	I	**Receive Bipolar Data Inputs.** Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
36	**RCL**	O	**Receive Carrier Loss.** High if 32 consecutive "0's" appear at RPOS and RNEG, goes low after next "1."
37	**RBV**	O	**Receive Bipolar Violation.** High during accused bit time at RSER if bipolar violation detected, low otherwise.

38	**RFER**	O	**Receive Frame Error.** High during F-Bit time when F_T or F_S errors occur (193S), or when FPS or CRC errors occur (193E). Low during resync.
39	**RLOS**	O	**Receive Loss of Sync.** Indicates sync status; high when internal resync is in progress, low otherwise.

REGISTER SUMMARY Table 5

REGISTER	ADDRESS	T/R[1]	DESCRIPTION/FUNCTION
RSR	0000	R[2]	**Receive Status Register.** Reports all receive alarm conditions.
RIMR	0001	R	**Receive Interrupt Mask Register.** Allows masking of individual alarm generated interrupts.
BVCR	0010	R	**Bipolar Violation Count Register.** 8 bit presettable counter which records individual bipolar violations.
ECR	0011	R	**Error Count Register.** 2 independent 4-bit counters which record OOF occurrences, and individual frame bit or CRC errors.
CCR[3]	0100	T/R	**Common Control Register.** Selects device operating characteristics common to receive and transmit sides.
RCR[3]	0101	R	**Receive Control Register.** Programs device operating characteristics unique to the receive side.
TCR[3]	0110	T	**Transmit Control Register.** Selects additional transmit side modes.
TIR1 **TIR2** **TIR3**	0111 1000 1001	T T T	**Transmit Idle Registers.** Designate which outgoing channels are to be substituted with idle code.
TTR1 **TTR2** **TTR3**	1010 1011 1100	T T T	**Transmit Transparent Registers.** Designate which outgoing channels are to be treated transparently. (No robbed bit signaling or bit 7 zero insertion.)
RMR1 **RMR2** **RMR3**	1101 1110 1111	R R R	**Receive Mark Registers.** Designate which incoming channels are to be replaced with idle or digital milliwatt codes (under control of RCR).

NOTES: 1. Transmit or receive side register.
2. RSR is a read only register, all other registers are read/write.
3. Reserved bit locations in the control registers should be programmed to 0, to maintain compatibility with future transceiver products.

SERIAL PORT INTERFACE

Pins 14 through 18 of the DS2180A serve as a microprocessor/microcontroller compatible serial port. Sixteen on-board registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads and/or writes by the host.

ADDRESS/COMMAND

Reading or writing the control, configuration or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. The following 4 bit nibble identifies register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. *Data is written to and read from the transceiver LSB first.*

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the rising edge of SCLK and *must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes.* Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO is tristated when $\overline{CS}$ is high.

DATA I/O

Following the 8 SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edges of the next 8 SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next 8 SCLK cycles. The SDO pin is tristated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE

The burst mode allows all on-board registers to be consecutively read or written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power-up or system reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. Burst is terminated by low-high transition on $\overline{CS}$.

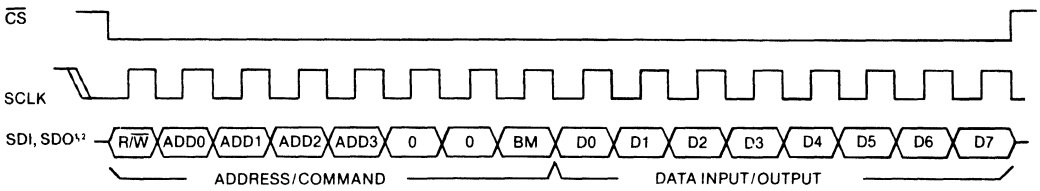
ACB: ADDRESS COMMAND BYTE Figure 2

(MSB) (LSB)

BM	—	—	ADD3	ADD2	ADD1	ADD0	R/$\overline{W}$

SYMBOL	POSITION	NAME AND DESCRIPTION
BM	ACB.7	**Burst Mode.** If set (and ACB.1 through ACB.4 = 0) burst read or write is enabled
—	ACB.6	Reserved, must be 0 for proper operation
—	ACB.5	Reserved, must be 0 for proper operation
ADD3	ACB.4	MSB of register address
ADD0	ACB.1	LSB of Register address
R/$\overline{W}$	ACB.0	**Read/Write Select.** 0 = write addressed register 1 = read addressed register

SERIAL PORT READ/WRITE Figure 3



NOTES: 1. SDI sampled on rising edge of SCLK
2. SDO updated on falling edge of SCLK

COMMON CONTROL REGISTER Figure 4

(MSB) (LSB)

—	FRSR2	EYELMD	FM	SYELMD	B8ZS	B7	LPBK

SYMBOL	POSITION	NAME AND DESCRIPTION
—	CCR.7	Reserved, must be 0 for proper operation
FRSR2	CCR.6	**Function of Rec Status Register 2.** 0 = Detected B8ZS code words reported at RSR.2 1 = COFA (Change-of-Frame Alignment) reported at RSR.2 when last resync resulted in change of frame or multiframe alignment.
EYELMD	CCR.5	**193E Yellow Mode Select.** 0 = Yellow alarm is a repeating pattern set of 00 hex and FF hex 1 = Yellow alarm is a "0" in the bit 2 position of all channels
FM	CCR.4	**Frame Mode Select.** 0 = D4 (193S, 12 frames/superframe) 1 = Extended (193E, 24 frames/superframe)
SYELMD	CCR.3	**193S Yellow Mode Select.** Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a "1" in the S-bit position of frame 12; if cleared, yellow alarm is a "0" in bit 2 of all channels. Does not affect 193E yellow alarm operation.
B8ZS	CCR.2	**Bipolar eight zero substitution.** 0 = No B8ZS 1 = B8ZS Enabled
B7	CCR.1	**Bit seven zero suppression.** If CCR.1 = 1, channels with an all zero content will be transmitted with bit 7 forced to "1." If CCR.1 = 0, no bit 7 stuffing occurs.
LPBK	CCR.0	**Loopback.** When set, the device internally loops output transmit data into the incoming receive data buffers and TCLK is internally substituted for RCLK.

LOOPBACK (Refer to Figure 4)

Enabling loopback will typically induce an out-of-frame "OOF" condition. If appropriate bits are set in the receive control register, the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit unframed all "1's." All operating modes (B8ZS, alarm, signaling, etc.) except for blue alarm transmission are available in loopback.

BIT SEVEN STUFFING

Existing systems meet "ones" density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is "globally" enabled by asserting bit CCR.1, and may be disabled on an individual channel basis by setting appropriate bits in TTR1-TTR3.

B8ZS

The DS2180A supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system "ones" density requirements without disturbing data integrity as required in emerging clear channel applications. B8ZS coding replaces 8 consecutive outgoing zeros with a B8ZS code word. Any received B8ZS code word is replaced with all zeros.

TCR: TRANSMIT CONTROL REGISTER Figure 5

(MSB) (LSB)

ODF	TFPT	TCP	RBSE	TIS	193SI	TBL	TYEL

SYMBOL	POSITION	NAME AND DESCRIPTION
ODF	TCR.7	**Output Data Format.** 0 = Bipolar data at TPOS and TNEG 1 = NRZ data at TPOS; TNEG = 0
TFPT	TCR.6	**Transmit Framing Pass-through.** 0 = FT/FPS sourced internally 1 = FT/FPS sampled at TSER during F-bit time
TCP	TCR.5	**Transmit CRC Pass-through.**0 = Transmit CRC code internally generated. 1 = TSER sampled at CRC F-bit time for external CRC insertion.
RBSE	TCR.4	**Robbed Bit Signaling Enable.**1 = signaling inserted in all channels during signaling frames. 0 = no signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DS0 channels.)
TIS	TCR.3	**Transmit Idle Code Select.** Determines idle code format to be inserted into channels marked by the TIR registers. 0 = insert 7F (Hex) into marked channels. 1 = insert FF (Hex) into marked channels.
193SI	TCR.2	**193S S-bit Insertion.** Determines source of transmitted S-bit. 0 = internal S-bit generator 1 = external (sampled at TLINK input)
TBL	TCR.1	**Transmit Blue Alarm.** 0 = disabled 1 = enabled
TYEL	TCR.0	**Transmit Yellow Alarm.** 0 = disabled 1 = enabled

TRANSMIT BLUE ALARM (Refer to Figure 5)
The blue alarm (also known as the AIS, Alarm Indication Signal) is an unframed, all 1's sequence enabled by asserting TCR.1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR.1. Use of the TIR registers allows a framed, all 1's alarm transmission if required by the network.

TRANSMIT YELLOW ALARM
In 193E framing a yellow alarm is a repeating pattern set of FF (Hex) and 00 (Hex) on the 4 KHz facility data link (FDL). In 193S framing, the yellow alarm format is dependent on the state of bit CCR.3. In all modes, yellow alarm is enabled by asserting TCR.0 and disabled by clearing TCR.0.

TRANSMIT SIGNALING
When enabled (via TCR.4) channel signaling is inserted in frames 6 and 12, (193S) or 6, 12 and 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allow external multiplexing of separate serial links for A, B or A, B, C, D signaling sources.

TTR1-TTR3: TRANSMIT TRANSPARENCY REGISTERS Figure 6

(MSB) (LSB)

CH8	**CH7**	**CH6**	**CH5**	**CH4**	**CH3**	**CH2**	**CH1**	TTR1
CH16	**CH15**	**CH14**	**CH13**	**CH12**	**CH11**	**CH10**	**CH9**	TTR2
CH24	**CH23**	**CH22**	**CH21**	**CH20**	**CH19**	**CH18**	**CH17**	TTR3

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	**Transmit Transparent Registers.** Each of these bit positions represents a DS0 channel in the outgoing frame. When set the corresponding channel is transparent.
CH1	TTR1.0	

TIR1-TIR3: TRANSMIT IDLE REGISTERS Figure 7

(MSB) (LSB)

CH8	**CH7**	**CH6**	**CH5**	**CH4**	**CH3**	**CH2**	**CH1**	TIR1
CH16	**CH15**	**CH14**	**CH13**	**CH12**	**CH11**	**CH10**	**CH9**	TIR2
CH24	**CH23**	**CH22**	**CH21**	**CH20**	**CH19**	**CH18**	**CH17**	TIR3

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	**Transmit Idle Registers.** Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel will output an idle code format determined by TCR.3.
CH1	TIR1.0	

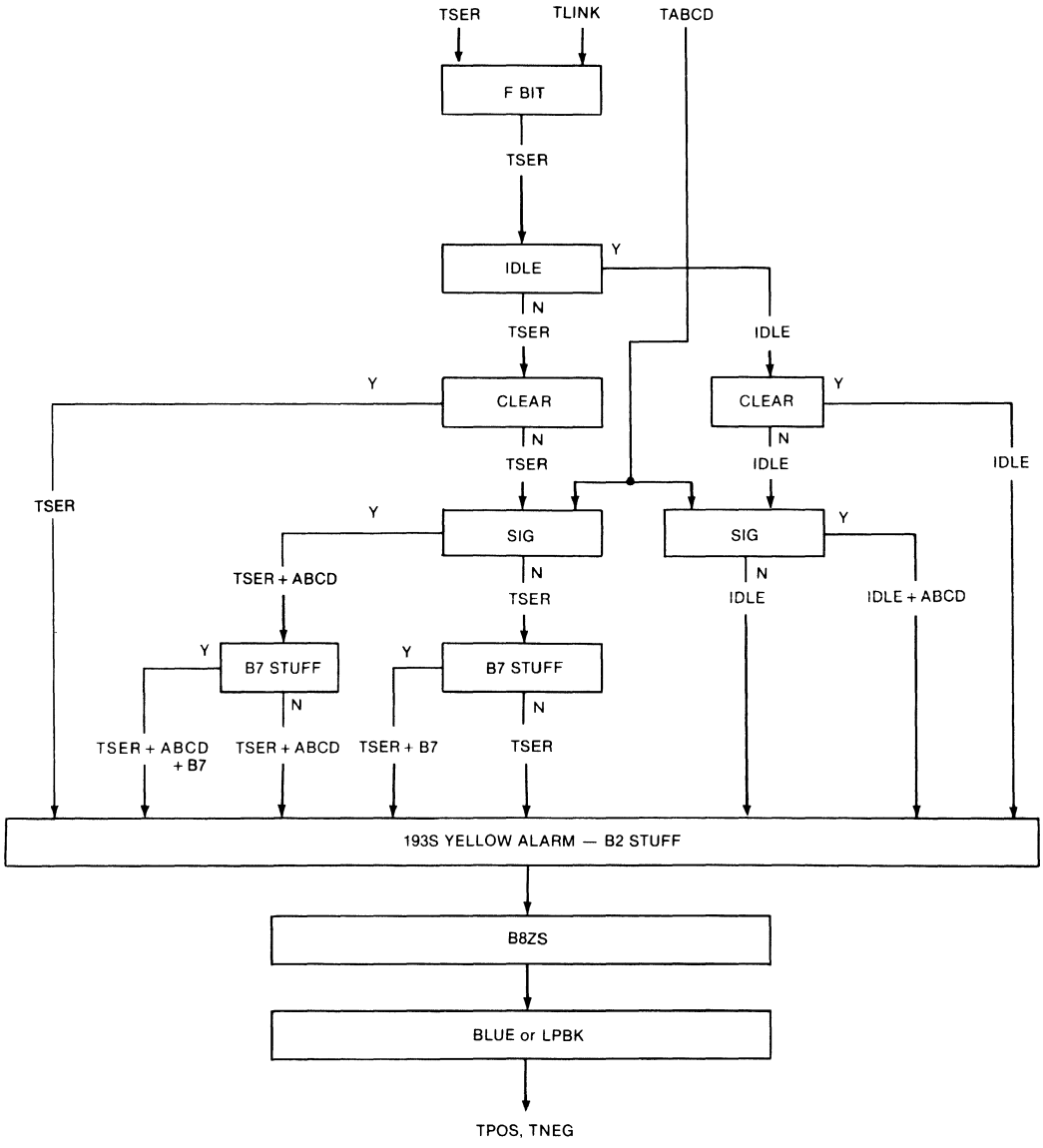
TRANSMIT CHANNEL TRANSPARENCY

Individual DS0 channels in the T1 frame may be programmed clear (no inserted robbed bit signaling and no bit 7 zero suppression) by setting the appropriate bits in the transmit transparency registers. Channel transparency is required in mixed voice/data or data-only environments such as ISDN, where data integrity must be maintained.

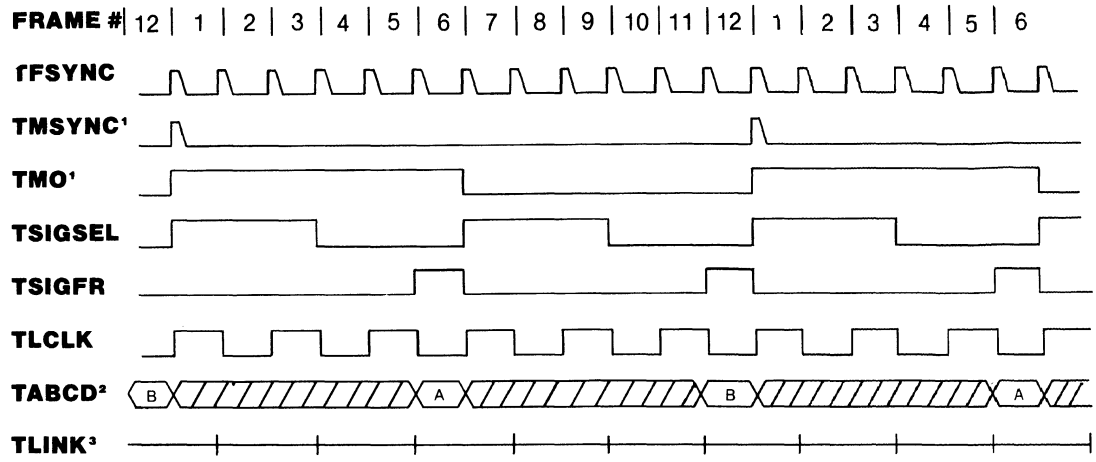
TRANSMIT IDLE CODE INSERTION

Individual outgoing channels in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR.3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates external hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream.

TRANSMIT INSERTION HIERARCHY Figure 8

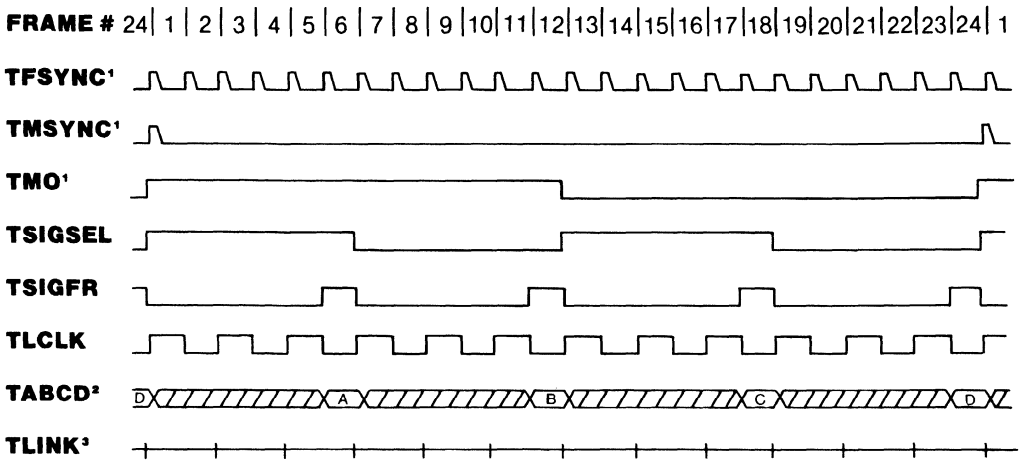


193S TRANSMIT MULTIFRAME TIMING Figure 9



NOTES:
1. Transmit frame and multiframe timing may be established in one of four ways:
   a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c) TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
   d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.
2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. When external S-bit insertion is enabled, TLINK will be sampled during the F-bit time of even frames and inserted into the outgoing data stream.

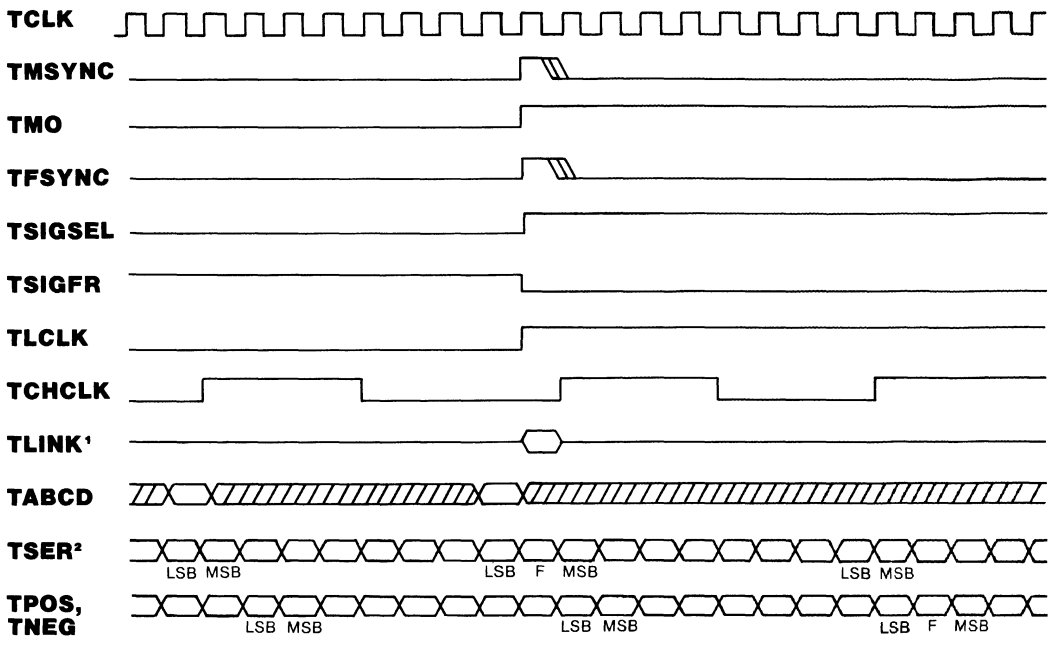
193E TRANSMIT MULTIFRAME TIMING Figure 10



NOTES: 1. Transmit frame and multiframe timing may be established in one of four ways:
   a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries, allowing internal counters to determine frame timing.
   b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.
   c) TMSYNC and TFSYNC may be continuously pulsed to establish and reinforce frame and superframe timing.
   d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.

2. Channels in which robbed bit signaling is enabled will sample TABCD during the LSB bit time in frames indicated.
3. TLINK is sampled during the F-bit time of odd frames and inserted into the outgoing data stream (FDL data).

TRANSMIT MULTIFRAME BOUNDARY TIMING Figure 11



NOTES: 1. TLINK timing shown is for 193E framing; in 193E framing, TLINK is sampled as indicated for insertion into F-bit position of odd frames. When S-bit insertion is enabled in 193S, TLINK is sampled during even frames.

2. If TCR.5 = 1; TSER is sampled during the F-bit time of CRC frames for insertion into the outgoing data stream (193E Framing only).

RECEIVE CONTROL REGISTER Figure 12

(MSB) (LSB)

ARC	OOF	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
ARC	RCR.7	**Auto Resync Criteria.** 0 = Resync on OOF or RCL event. 1 = Resync on OOF only.
OOF	RCR.6	**Out-of-frame (OOF) Condition Detection.** 0 = 2 of 4 framing bits in error 1 = 2 of 5 framing bits in error
RCI	RCR.5	**Receive Code Insert.** When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.
RCS	RCR.4	**Receive Code Select.** 0 = idle code (7F Hex) 1 = digital milliwatt
SYNCC	RCR.3	**Sync Criteria.** Determines the type of algorithm utilized by the receive synchronizer and differs for each frame mode. **193S Framing (CCR.4 = 0).** 0 = synchronize to frame boundaries using F_T pattern, then search for multiframe by using F_S. 1 = cross couple F_T and F_S patterns in sync algorithm. **193E Framing (CCR.4 = 1).** 0 = normal sync (utilizes FPS only) 1 = validate new alignment with CRC before declaring sync.
SYNCT	RCR.2	**Sync Time.** If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.
SYNCE	RCR.1	**Sync Enable.** If clear, the transceiver will automatically begin a resync if 2 of the previous 4 or 5 framing bits were in error, or if carrier loss is detected. If set, no auto resync occurs.
RESYNC	RCR.0	**Resync.** When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

RECEIVE CODE INSERTION

Incoming receive channels can be replaced with idle (7F Hex) or digital milliwatt (u-LAW format) codes. The receive mark registers indicate which channels are inserted. When set, bit RCR.5 serves as a "global" enable for marked channels, and bit RCR.4 selects inserted code format: 0 = idle code, 1 = digital milliwatt.

RECEIVE SYNCHRONIZER

Bits RCR.0 through RCR.3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate qualify testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

RECEIVE SIGNALING

Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data.

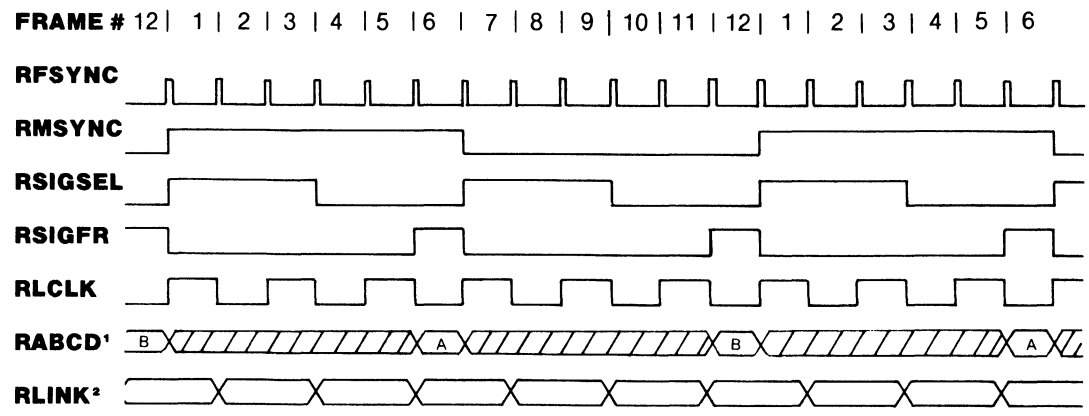
RMR1-RMR3: RECEIVE MARK REGISTERS Figure 13

(MSB) (LSB)

CH8	**CH7**	**CH6**	**CH5**	**CH4**	**CH3**	**CH2**	**CH1**	RMR1
CH16	**CH15**	**CH14**	**CH13**	**CH12**	**CH11**	**CH10**	**CH9**	RMR2
CH24	**CH23**	**CH22**	**CH21**	**CH20**	**CH19**	**CH18**	**CH17**	RMR3

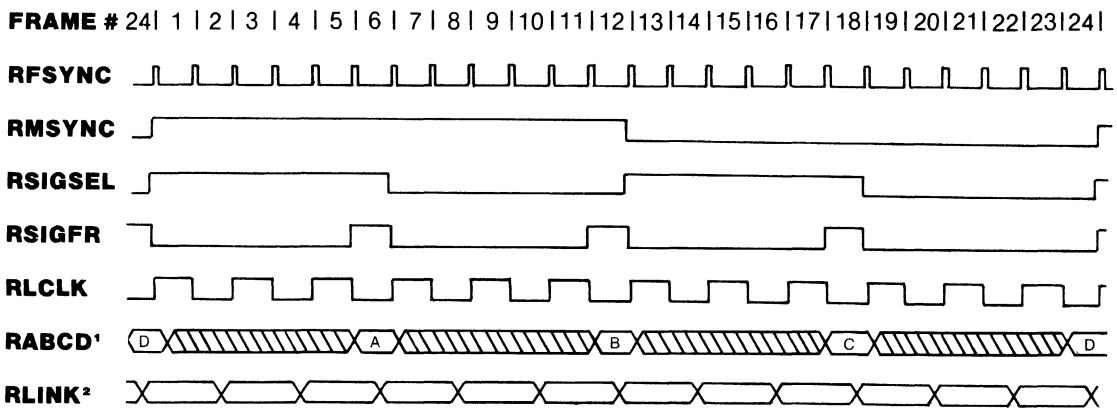
SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RMR3.7	**Receive Mark Registers.** Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set the corresponding channel will output codes determined by RCR.4 and RCR.5.
CH1	RMR1.0	

193S RECEIVE MULTIFRAME TIMING Figure 14



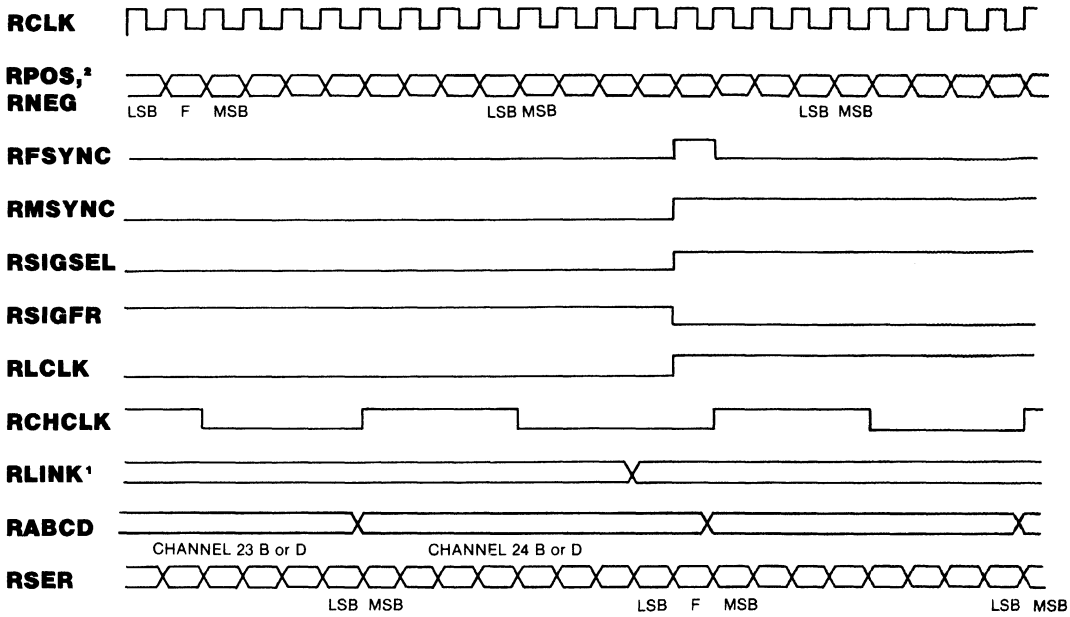
NOTES: 1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

193E RECEIVE MULTIFRAME TIMING Figure 15



NOTES: 1. Signaling data is updated during signaling frames on channel boundaries. RABCD outputs the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL-bit) is updated one bit time prior to odd frames and held for two frames.

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 16



NOTES: 1. RLINK timing is shown for 193E; in 193S RLINK is updated on even frame boundaries and is held across multiframe edges.
2. Total delay from RPOS and RNEG to RSER output is 13 RCLK periods.

RSR: RECEIVE STATUS REGISTER Figure 17

(MSB) (LSB)

BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
BVCS	RSR.7	**Bipolar Violation Count Saturation.** Set when the 8-bit counter at BVCR saturates.
ECS	RSR.6	**Error Count Saturation.** Set when either of the 4-bit counters at ECR saturates.
RYEL	RSR.5	**Receive Yellow Alarm.** Set when yellow alarm detected. (Detected yellow alarm format determined by CCR.4 and CCR.3.)
RCL	RSR.4	**Receive Carrier Loss.** Set when 32 consecutive "0's" appear at RPOS and RNEG.
FERR	RSR.3	**Frame Bit Error.** Set when F_T (193S) or FPS (193E) bit error occurs.
B8ZSD	RSR.2	**Bipolar Eight Zero Substitution Detect.** Set when B8ZS code word detected.
RBL	RSR.1	**Receive Blue Alarm.** Set when 2 consecutive frames have less than 3 zeros (total) in the data stream (F-bit positions not tested).
RLOS	RSR.0	**Receive Loss of Sync.** Set when resync is in process; if RCR.1 = 0, RLOS transitions high on an OOF event or carrier loss, indicating auto resync.

5

RECEIVE ALARM REPORTING

Incoming serial data is monitored by the transceiver for alarm occurrences. Alarm conditions are reported in two ways: via transitions on the alarm output pins and registered interrupt, in which the host controller reads the RSR in response to an alarm driven interrupt. Interrupts may be direct, in which the transceiver demands service for a real time alarm, or count-overflow triggered, in which an on-board alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register (RIMR).

ALARM SERVICING

The host controller must service the transceiver in order to clear an interrupt condition. Clearing appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupts (those driven from real-time alarms) will be cleared when the RSR is directly read, unless the alarm condition still exists. Count-overflow interrupts (BVCS, FCS) are not cleared by a direct read of the RSR. They will be cleared only when the user presets the appropriate count register to a value other than all "1s." A burst read of the RSR will not clear an interrupt condition.

RIMR: RECEIVE INTERRUPT MASK REGISTER Figure 18

(MSB) (LSB)

BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
BVCS	RIMR.7	**Bipolar Violation Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
ECS	RIMR.6	**Error Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
RYEL	RIMR.5	**Receive Yellow Alarm Mask.** 1 = interrupt enabled 0 = interrupt masked
RCL	RIMR.4	**Receive Carrier Loss Mask.** 1 = interrupt enabled 0 = interrupt masked
FERR	RIMR.3	**Frame Bit Error Mask.** 1 = interrupt enabled 0 = interrupt masked
B8ZSD	RIMR.2	**B8ZS Detect Mask.** 1 = interrupt enabled 0 = interrupt masked
RBL	RIMR.1	**Receive Blue Alarm Mask.** 1 = interrupt enabled 0 = interrupt masked
RLOS	RIMR.0	**Receive Loss of Sync Mask.** 1 = interrupt enabled 0 = interrupt masked

ALARM COUNTERS

The three on-board alarm event counters allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presettable by the user, establishing an event count interrupt threshold. As each counter saturates, the next error event occurrence will set a bit in the RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

OOF EVENTS AND ERRORED SUPERFRAMES

Out of frame is declared when at least two of four (or five) consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S, the FPS bits are tested in 193E. OOF events are recorded by the 4-bit OOF counter in the error count register. In the 193E framing mode, the OOF event is logically "OR'ed" with an on-chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4-bit ESF error counter in the error count register. In the 193S framing mode, the 4-bit ESF error counter records individual F_T and F_S errors when RCR.3 = 1, or F_T errors only when RCR.3 = 0.

BVCR: BIPOLAR VIOLATION COUNT REGISTER Figure 19

(MSB) (LSB)

BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

SYMBOL	POSITION	NAME AND DESCRIPTION
BVD7	BVCR.7	MSB of bipolar violation count
BVD0	BVCR.0	LSB of bipolar violation count

This 8 bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation once saturated (RIMR.7 = 1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "up" to saturation from the preset value, and may be read at any time. Counter increments occur at all times and are not disabled by resync.

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ECR: ERROR COUNT REGISTER Figure 20

(MSB) (LSB)

OOFD3	OOFD2	OOFD1	OOFD0	ESFD3	ESFD2	ESFD1	ESFD0
← OOF COUNT →				← ESF ERROR COUNT →			

SYMBOL	POSITION	NAME AND DESCRIPTION
OOFD3	ECR.7	MSB of OOF event count
OOFD0	ECR.4	LSB of OOF event count
ESFD3	ECR.3	MSB of extended superframe error count
ESFD0	ECR.0	LSB of extended superframe error count

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF error event after saturation (RIMR.6 = 1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counters will count "up" to saturation from the preset value, and may be read at any time. These counters share the same register address, and must be written to or read from simultaneously.

The OOF counter records out-of-frame events in both 193S and 193E. The ESF error counter records errored superframes in 193E. In 193S the ESF counter records individual F_T and F_S errors when RCR.3 = 1; F_T errors only when RCR.3 = 0. ECR counter increments are disabled when resync is in progress (RLOS high).

ALARM OUTPUTS

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on-board alarm logic.

RLOS OUTPUT

The receive loss of sync output indicates the status of the receiver synchronizer circuitry: when high, an off-line resynchronization is in progress and a high-low transition indicates resync is complete. The RLOS bit (RSR.0) is a "latched" version of the RLOS output. If the auto-resync mode is selected (RCR.1 = 0) RLOS is a real time indication of a carrier loss or OOF event occurrence.

RYEL OUTPUT

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR.5) is a "latched" version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 (Hex) and FF (Hex) received at RLINK. In 193S framing the yellow alarm format is dependent on CCR.3: if CCR.3 = 0, the RYEL output transitions high if bit 2 of 256 or more consecutive channels is 0; if CCR.3 = 1, yellow alarm is declared when the S-bit received in frame 12 is 1.

RBV OUTPUT

The bipolar violation output transitions high when accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

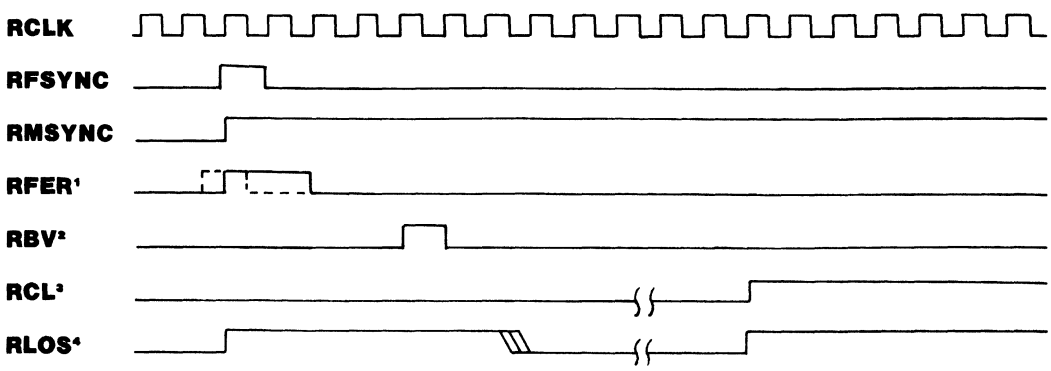
RFER OUTPUT

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S framing F_T and F_S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low-high-low transition (one bit period wide) one half RCLK period before a low-high transition on RMSYNC.

RESET

A high-low transition on $\overline{RST}$ clears all registers and forces immediate receive resync when $\overline{RST}$ returns high. This reset has no effect on transmit frame, multiframe, or channel counters. $\overline{RST}$ must be held low on system power-up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

ALARM OUTPUT TIMING Figure 21



NOTES:

1. RFER transitions high during F-bit time if received framing pattern bit is in error. (Frame 12 F-bits in 193S are ignored if CCR.3 = 1.) Also, in 193E, RFER transitions ½ bit time before the rising edge of RMSYNC to indicate a CRC error for the previous multiframe.
2. RBV indicates received bipolar violation and transitions high when accused bit emerges from RSER. If B8ZS is enabled, RBV will not report the zero replacement code.
3. RCL transitions high (during 32nd bit time) when 32 consecutive bits received are "0"; RCL transitions low when the next "1" is received.
4. RLOS transitions high during the F-bit time that caused an OOF event (any 2 of 4 consecutive F_T or FPS bits are in error) if auto-resync mode is selected (RCR.1 = 0). Resync will also occur when loss of carrier is detected (RCL = 1). When RCR.1 = 1, RLOS remains low until resync occurs, regardless of OOF or carrier loss flags. In this situation, resync is initiated only when RCR.0 transitions low-to-high or the $\overline{RST}$ pin transitions high-low-high.

HARDWARE MODE

For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying SPS to VSS disables the serial port, clears all internal registers except CCR and TCR and redefines pins 14 through 18 as mode control inputs. The hardware mode allows device retrofit into existing applications where mode control and alarm conditioning hardware is often designed with discrete logic.

HARDWARE COMMON CONTROL

In the hardware mode bits TCR.2, CCR.4, TCR.0, CCR.1 and CCR.2 map to pins 14 through 18. The loopback feature (bit CCR.0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched as when both pins are taken high, preserving the current zero suppression mode). Robbed bit signalling (bit TCR.4) is enabled for all channels. The user may tie TSER to TABCD externally to disable signaling if so desired. Bit CCR.3 is forced to 0, which selects bit 2 yellow alarm in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR, are cleared in the hardware mode. The $\overline{RST}$ input may be used to force immediate receiver resync, and has no effect on transmit.

HARDWARE MODE Table 6

PIN NUMBER	REGISTER BIT LOCATION	NAME AND DESCRIPTION
14	**TCR-D2**	**193S - S-bit insertion[3].** 1 = external; 0 = internal
15	**CCR-D4**	**Framing Mode Select.** 1 = 193E; 0 = 193S
16	**TCR-D0**	**Transmit Yellow Alarm[2,3].** 1 = enabled; 0 = disabled
17	**CCR-D1**	**Zero Suppression[1].** 1 = bit 7 stuffing 0 = transparent
18	**CCR-D2**	**B8ZS[1].** 1 = enabled; 0 = disabled

NOTES:
1. Tying pins 17 and 18 high enables loopback in the hardware mode.
2. Bit 2 (193S) and data link (193E) yellow alarms are supported.
3. S-bit yellow alarm (193S) is not internally supported; however, the user may elect to insert external S-bits for alarm purposes.

T1 Overview

FRAMING STANDARDS

The DS2180A is compatible with the existing Bell System D4 framing standard described in ATT PUB 43801 and the new extended superframe format (ESF) as described in ATT C.B. #142. In this document, D4 framing is referred to as 193S, and ESF (also known as Fe) is referred to as 193E. Programmable features of the DS2180A allow support of other framing standards which are derivatives of 193E and 193S. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position. In 193S, 12 frames make up a superframe; in 193E, 24. A frame consists of 24 channels (time-slots) of 8-bit data preceded by an F-bit. Channel data is transmitted and received MSB first.

F-BITS

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F_T-bits) which provides frame alignment information, and the signaling framing pattern (known as F_S-bits) which provides multiframe alignment information. In 193E framing, the F-bit position is shared by the framing pattern sequence (FPS), which provides frame and multiframe alignment information, a 4 KHz data link (facility data link) known as FDL, and CRC (cyclic redundancy check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK) and the CRC bits are an indicator of link quality and may be monitored by the user to establish error performance.

SIGNALING

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted. In 193E, A and B data is inserted into frames 6 and 12, and C and D data is inserted into frames 18 and 24. This allows a maximum of 4 signaling states to be transmitted per superframe in 193S and 16 states in 193E.

ALARMS

The DS2180A supports all alarm pattern generation and detection required in typical Bell System applications. These alarm modes are explained in ATT PUB 43801, ATT C.B. #142 and elsewhere in this document.

193E FRAMING FORMAT Table 7

FRAME NUMBER	F-BIT USE			BIT USE IN EACH CHANNEL		SIGNALING-BIT USE		
	FPS[1]	FDL[2]	CRC[3]	DATA	SIGNALING[4,5]	2 STATE	4 STATE	16 STATE
1	—	M	—	BITS 1-8				
2	—	—	C1	BITS 1-8				
3	—	M	—	BITS 1-8				
4	0	—	—	BITS 1-8				
5	—	M	—	BITS 1-8				
6	—	—	C2	BITS 1-7	**BIT 8**	A	A	A
7	—	M	—	BITS 1-8				
8	0	—	—	BITS 1-8				
9	—	M	—	BITS 1-8				
10	—	—	C3	BITS 1-8				
11	—	M	—	BITS 1-8				
12	1	—	—	BITS 1-7	**BIT 8**	A	B	B
13	—	M	—	BITS 1-8				
14	—	—	C4	BITS 1-8				
15	—	M	—	BITS 1-8				
16	0	—	—	BITS 1-8				
17	—	M	—	BITS 1-8				
18	—	—	C5	BITS 1-7	**BIT 8**	A	A	C
19	—	M	—	BITS 1-8				
20	1	—	—	BITS 1-8				
21	—	M	—	BITS 1-8				
22	—	—	C6	BITS 1-8				
23	—	M	—	BITS 1-8				
24	1	—	—	BITS 1-7	**BIT 8**	A	B	D

NOTES:

1. FPS - Framing Pattern Sequence.
2. FDL - 4 KHz Facility Data Link; M = message bits.
3. CRC - Cyclic Redundancy Check Bits. The CRC code will be internally generated by the device when TCR.5 = 0. When TCR.5 = 1, externally supplied CRC data will be sampled at TSER during the F-bit time of frames 2, 6, 10, 14, 18, 22.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.
5. Depending on application, the user can support 2-state, 4-state or 16-state signaling by the appropriate decodes of TMO, TSIGFR, TSIGSEL (Transmit Side) and RMSYNC, RSIGFR AND RSIGSEL (Receive Side).

193S FRAMING FORMAT Table 8

FRAME NUMBER	F-BIT USE		BIT USE IN EACH CHANNEL		SIGNALING-BIT USE
	F_T[1]	F_S[2]	DATA	SIGNALING[4]	
1	1	—	BITS 1-8		
2	—	0	BITS 1-8		
3	0	—	BITS 1-8		
4	—	0	BITS 1-8		
5	1	—	BITS 1-8		
6	—	1	BITS 1-7	**BIT 8**	A
7	0	—	BITS 1-8		
8	—	1	BITS 1-8		
9	1	—	BITS 1-8		
10	—	1	BITS 1-8		
11	0	—	BITS 1-8		
12	—	0[3]	BITS 1-7	**BIT 8**	B

NOTES:
1. F_T (terminal framing) bits provide frame alignment information.
2. F_S (signaling frame) bits provide multiframe alignment information.
3. The S-bit in frame 12 may be used for yellow alarm transmission and detection in some applications.
4. The user may program any individual channels clear, in which case Bit 8 will be used for data, not signaling.

LINE CODING

T1 line data is transmitted in a bipolar alternative mark inversion line format; ones are transmitted as alternating negative and positive pulses and zeros are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a one's density constraint to keep clock extraction circuitry functioning, which is usually met by forcing bit 7 of any channel consisting of all 0's to 1. The use of Bipolar Eight Zero Substitution (B8ZS) satisfies all the one's density requirement, while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in ATT C.B. #144. When the B8ZS feature is enabled, any outgoing stream of eight consecutive zeros is replaced with a B8ZS code word. If the last "one" transmitted was positive, the inserted code is 000 + – 0 – + ; if negative, the code word inserted is 000 – + 0 + –. Bipolar violations occur in the fourth and seventh bit positions, which are ignored by the DS2180A error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all 0's if B8ZS is enabled. Also, the receive status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability, and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR.2.

Transmit Side Overview

The transmit side of the DS2180A is made up of 6 major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC. The timing and clock generation circuit develops all on-board and output clocks to the system from inputs TCLK, TFSYNC and TMSYNC. The yellow alarm circuitry generates mode dependent yellow alarms. The CRC block generates checksum results utilized in 193E framing. F-bit data provides mode dependent framing patterns and allows insertion of link or S-bit data externally. All of these blocks feed into the data selector, where under control of the CCR, TCR, TIRs and TTRs, the contents of the outgoing data stream are established by bit selection and insertion. The bipolar coder formats the output of the data selector to make it compatible with bipolar transmission techniques and inserts zero suppression codes. The bipolar coder also supports the on-board loopback feature. Input to output delay of the transmitter is 10 TCLK cycles.

Receive Side Overview

SYNCHRONIZER
The heart of the receiver is the synchronizer/sync monitor. This circuit serves two purposes: 1) monitoring the incoming data stream for loss of frame or multiframe alignment, and 2) searching for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment; all output timing signals remain at the old alignment with the exception of RSIGFR, which is forced low during resync. When one and only one candidate is qualified, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS will transition low, indicating valid sync and the resumption of the normal sync monitoring mode. Several bits in the RCR allow tailoring of the resync algorithm by the user. These bits are described below.

SYNC TIME (RCR.2)
Bit RCR.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR.2 = 1, the algorithm will validate 24 bits; if RCR.2 = 0, 10 bits are validated. 24-bit testing results in superior false framing protection, while 10-bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

RESYNC (RCR.0)
A zero-to-one transition of RCR.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

SYNC ENABLE (RCR.1)
When RCR.1 is cleared, the receiver will initiate automatic resync if any of the following events occur: 1) an OOF event ("out-of-frame"), or 2) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or FPS bits are in error. When RCR.1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR.0 to 1, or externally via a low-high transition on $\overline{RST}$. Note that using $\overline{RST}$ to initiate resync resets the receive output timing while $\overline{RST}$ is low; use of RCR.1 does not affect output timing until the new alignment is located.

SYNC CRITERIA (RCR.3)

193E

Bit RCR.3 determines which sync algorithm is utilized when resync is in progress (RLOS = 1). In 193E framing, when RCR.3 = 0, the synchronizer will lock only to the FPS pattern and will move to the new frame and multiframe alignment after the framing candidate is qualified. RLOS will go low one frame after the move to the new alignment. When RCR.3 = 1, the new alignment is further tested by a CRC code match. RLOS will transition low after a CRC match occurs. If no CRC match occurs in three attempts (three multiframes), the algorithm will reset and a new search for the framing pattern begins. It takes 9 ms for the synchronizer to check the first CRC code after the new alignment has been loaded. Each additional CRC test takes 3 msec. Regardless of the state of RCR.3, if more than one candidate exists after about 24 milliseconds, the synchronizer will begin eliminating emulators by testing their CRC codes on-line in order to find the true framing candidate.

193S

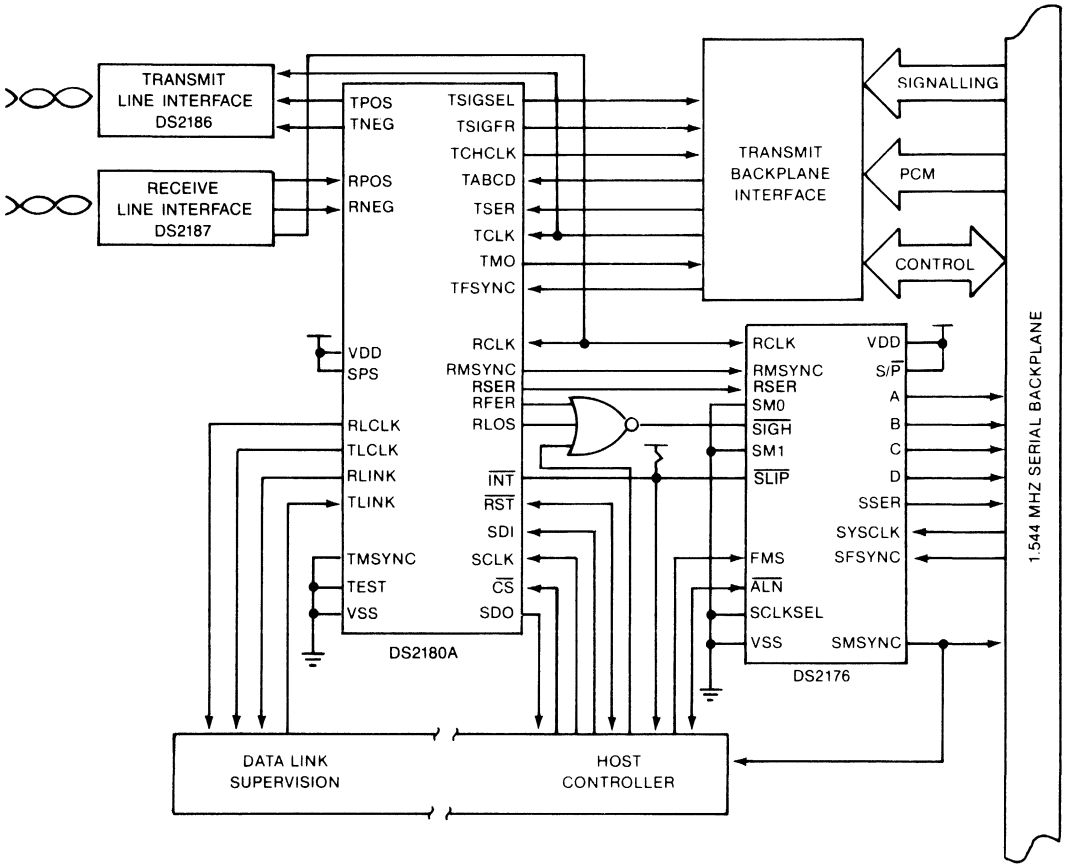
In 193S framing, when RCR.3 = 1, the synchronizer will cross check the F_T pattern with the F_S pattern to help eliminate false framing candidates such as digital milliwatts. The F_S patterns are compared to the repeating pattern . . . 00111000111000 . . . (00111X0 if CCR.3—YELMD—is equal to a 1).In this mode, F_T and F_S patterns must be correctly identified by the synchronizer before sync is declared. Clearing RCR.3 causes the synchronizer to search for F_T patterns (101010 . . .) without cross-coupling the F_S pattern. Frame sync will be established using the F_T information, while multiframe sync will be established only if valid F_S information is present. If no valid F_S pattern is identified, the synchronizer will move to the F_T alignment, RLOS will go low, and a false multiframe position may be indicated by RMSYNC. RFER will indicate when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode will be used in applications where non-standard S-bit patterns exist. In such applications multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

AVERAGE REFRAME TIME[1] Table 9

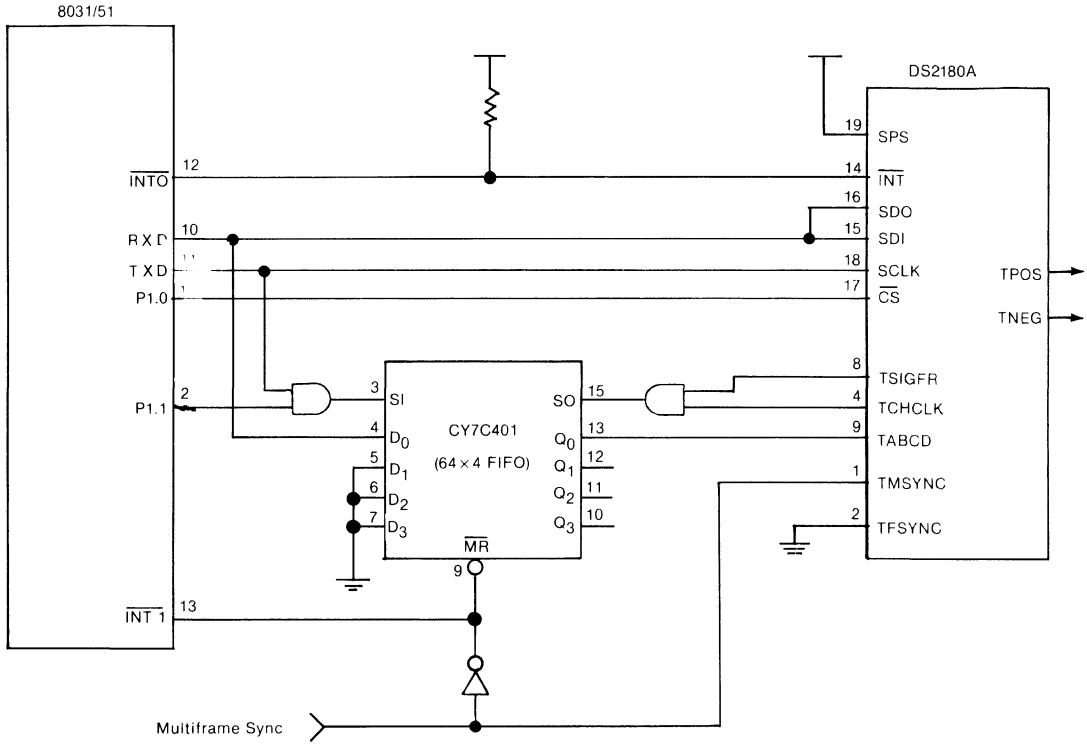
FRAME MODE	RCR.2 = 0			RCR.2 = 1			UNITS
	MIN	AVG	MAX	MIN	AVG	MAX	
193S	3.0	3.75	4.5	6.5	7.25	8.0	msec
193E	6.0	7.5	9.0	13.0	14.5	16.0	

NOTES: 1. Average Reframe Time is defined here as the average time it takes from the start of resync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.

BACKPLANE INTERFACE USING DS2180A AND DS2176 Figure 22



PROCESSOR-BASED TRANSMIT SIGNALLING INSERTION Figure 23



PROCESSOR-BASED SIGNALING

Many robbed-bit signaling applications utilize a microprocessor to insert transmit signaling data into the outgoing data stream. The circuit shown in figure 23 "decouples" the processor timing from that of the DS2180A by use of a small FIFO memory. The processor writes to the FIFO (6 bytes are written: 3 for A data, 3 for B data) only when signaling updates are required. The FIFO automatically retransmits old data when no updates occur. The system is interrupt-driven from the transmit multiframe sync input; the processor must update the FIFO prior to Frame 6 (625 *us*) after interrupt) to prevent data corruption. The application circuit shown supports 193S framing additional hardware is required for 193E applications.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	—	−1.0V to +7V
OPERATING TEMPERATURE	—	0°C to 70°C
STORAGE TEMPERATURE	—	−55°C to 125°C
SOLDERING TEMPERATURE	—	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0 °C to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Logic 1	V_{IH}	2.0		V_{DD} + .3	V
Logic 0	V_{IL}	− 0.3		+ 0.8	V
Supply	V_{DD}	4.5	5.0	5.5	V

5

CAPACITANCE (t_A = 25 °C)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	7	pF

D.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{DD}		3	10	mA	1,2
Input Leakage	I_{IL}			1	µA	
Output Leakage	I_{LO}			1	µA	3
Output Current @ 2.4V	I_{OH}	− 1			mA	4
Output Current @ .4V	I_{OL}	+ 4			mA	5

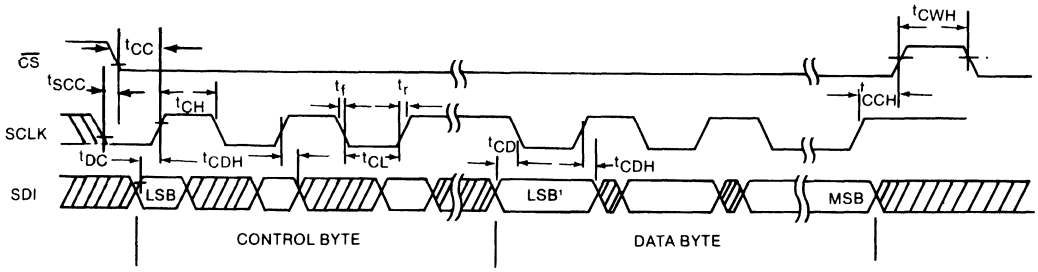
NOTES: 1. TCLK = RCLK = 1.544 MHz
2. Outputs open
3. Applies to SDO when tristated
4. All outputs except $\overline{INT}$, which is open collector
5. All outputs

A.C. ELECTRICAL CHARACTERISTICS[1] — SERIAL PORT (0 °C to 70 ° V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
SDI to SCLK Set up	t_{DC}	50			ns
SCLK to SDI Hold	t_{CDH}	50			ns
SDI to SCLK Falling Edge	t_{CD}	50			ns
SCLK Low Time	t_{CL}	250			ns
SCLK High Time	t_{CH}	250			ns
SCLK Rise & Fall Time	t_R, t_F			500	ns
$\overline{CS}$ to SCLK Set Up	t_{CC}	50			ns
SCLK to $\overline{CS}$ Hold	t_{CCH}	50			ns
$\overline{CS}$ Inactive Time	t_{CWH}	250			ns
SCLK to SDO Valid[2]	t_{CDV}			200	ns
$\overline{CS}$ to SDO High Z	t_{CDZ}			75	ns
SCLK Setup to $\overline{CS}$ Falling	t_{SCC}	50			ns

NOTES:
1.Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.
2.Output load capacitance = 100 pF.

SERIAL PORT WRITE A.C. TIMING DIAGRAM

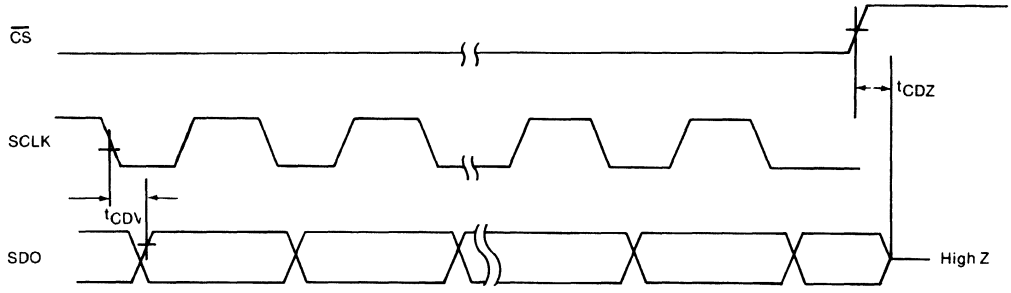


NOTES: 1. Data byte bits must be valid across low clock periods to prevent transients in operating modes.

2. Shaded regions indicate don't-care states of input data.

5

SERIAL PORT READ[1] A.C. TIMING



NOTES: 1. Serial port write must precede a port read to provide address information.

A.C. ELECTRICAL CHARACTERISTICS[1] — TRANSMIT (0 °C to 70°, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
TCLK Period	t_P	250	648		ns
TCLK Pulse Width	t_{WL}, t_{WH}	125	324		ns
TCLK, RCLK Rise & Fall Times	t_F, t_R		20		ns
TSER, TABCD, TLINK Set Up to TCLK Falling	t_{STD}	50			ns
TSER, TABCD, TLINK Hold from TCLK Falling	t_{HTD}	50			ns
TFSYNC, TMSYNC Set Up to TCLK Rising	t_{STS}	−125		125	ns
Propagation Delay TFSYNC to TMO, TSIGSEL, TSIGFR, TLCLK	t_{PTS}			75	ns
Propagation Delay TCLK to TCHCLK	t_{PTCH}			75	ns
TFSYNC, TMSYNC Pulse Width	t_{TSP}	100			ns

NOTES:

1.Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.
2.Output load capacitance = 100 pF.

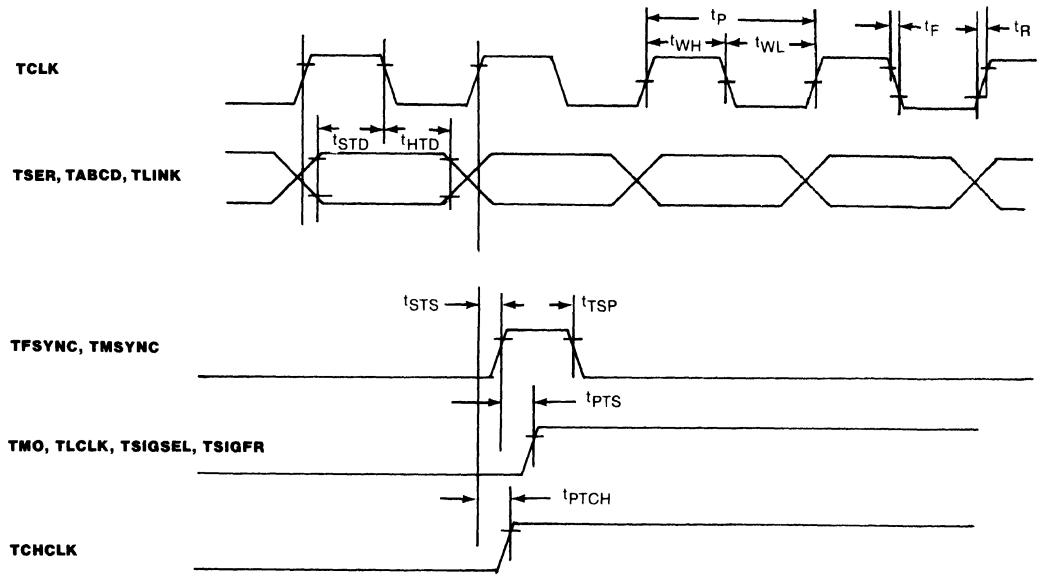
A.C. ELECTRICAL CHARACTERISTICS[1] — RECEIVE (0 °C to 70 °, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Propagation Delay RCLK to RMSYNC, RFSYNC, RSIGSEL, RSIGFR, RLCLK, RCHCLK	t_{PRS}			75	ns
Propagation Delay RCLK to RSER, RABCD, RLINK	t_{PRD}			75	ns
Transition Time All Outputs	t_{TTR}			20	ns
RCLK Period	t_P	250	648		ns
RCLK Pulse Width	t_{WL}, t_{WH}	125	324		ns
RCLK Rise & Fall Times	t_R, t_F		20		ns
RPOS, RNEG Set Up to RCLK Falling	t_{SRD}	50			ns
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50			ns
Propagation Delay RCLK to RYEL, RCL, RFER, RLOS, RBV	t_{PRA}			75	ns
Minimum $\overline{RST}$ Pulse Width on System Power Up or Restart	t_{RST}	1			μs

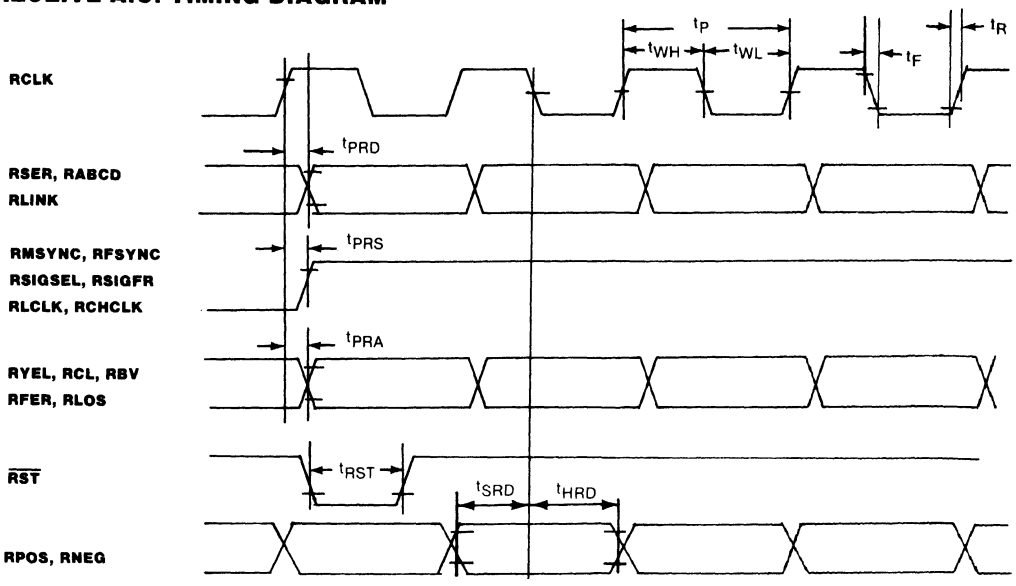
NOTES:

1.Measured at V_{IH} = 2.0V, V_{IL} = .8V, and 10 ns maximum rise and fall time.
2.Output load capacitance = 100 pF.

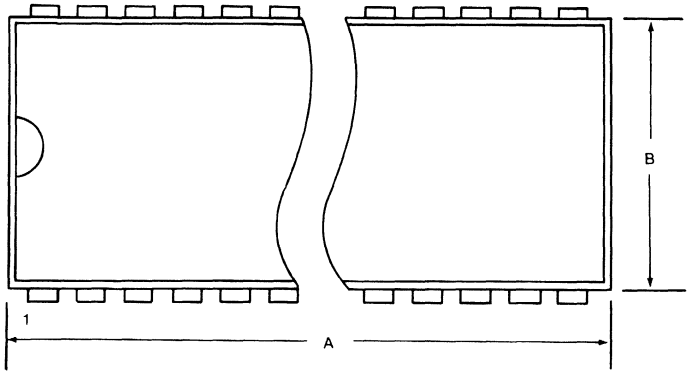
TRANSMIT A.C. TIMING DIAGRAM



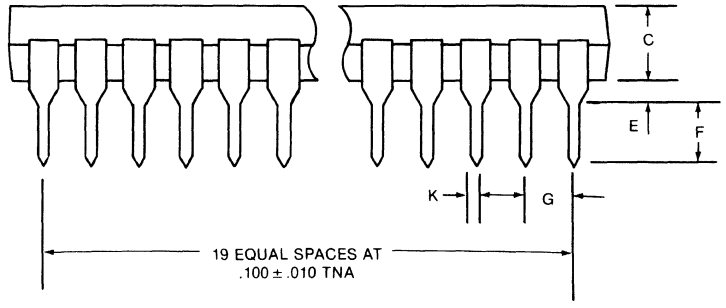
RECEIVE A.C. TIMING DIAGRAM

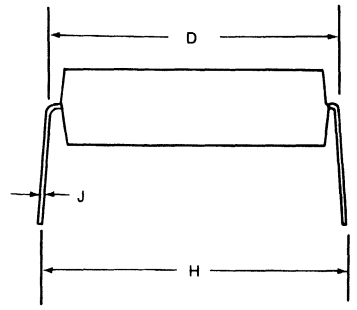


DS2180A
Serial T1 Transceiver

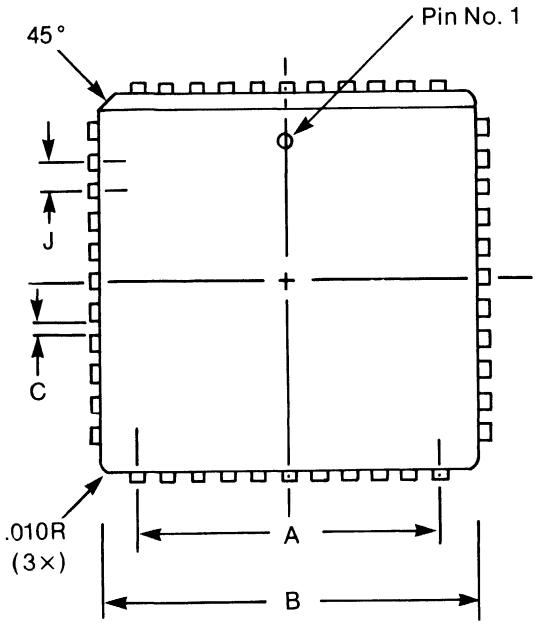


DIM.	INCHES	
	MIN.	MAX.
A	2.040	2.080
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

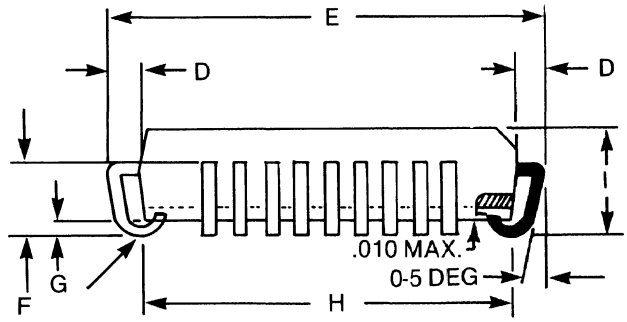


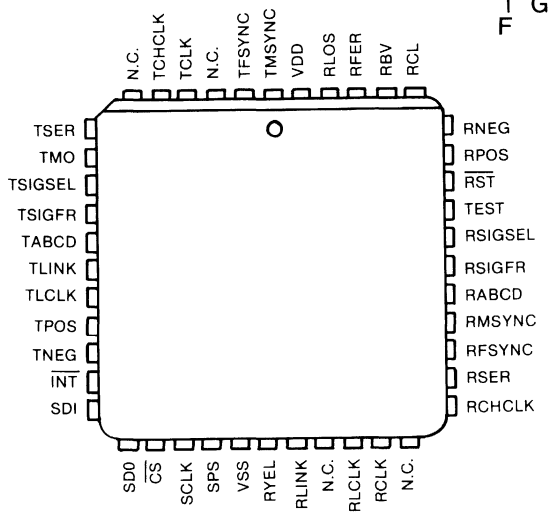


DS2180AQ



DIM.	INCHES	
	MIN.	MAX.
A	.490	.510
B	.590	.630
C	.020	.024
D	.018	.022
E	.688	.692
F	.118	.122
G	.020	.030
H	.590	.630
I	.167	.173
J	.048	.051





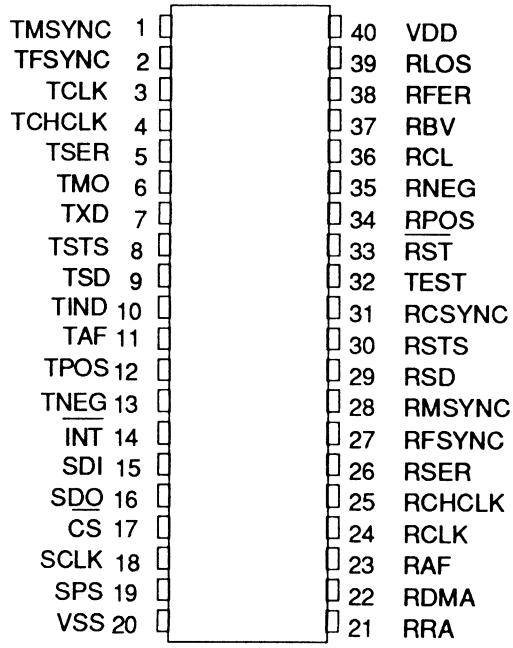
DALLAS SEMICONDUCTOR

DS2181
CEPT PRIMARY RATE TRANSCEIVER

FEATURES

- Single chip primary rate transceiver meets CCITT standards G.704 and G.732
- Supports new CRC4-based framing standards and CAS and CCS signalling standards
- Simple serial interface used for device configuration and control in processor mode
- Hardware mode requires no host processor; intended for stand-alone applications
- Comprehensive, on-chip alarm generation, alarm detection, and error logging logic
- Shares footprint with DS2180A T1 Transceiver
- Companion to DS2175 Transmit/Receive Elastic Store
- 5V supply; low-power CMOS technology

PIN CONNECTIONS



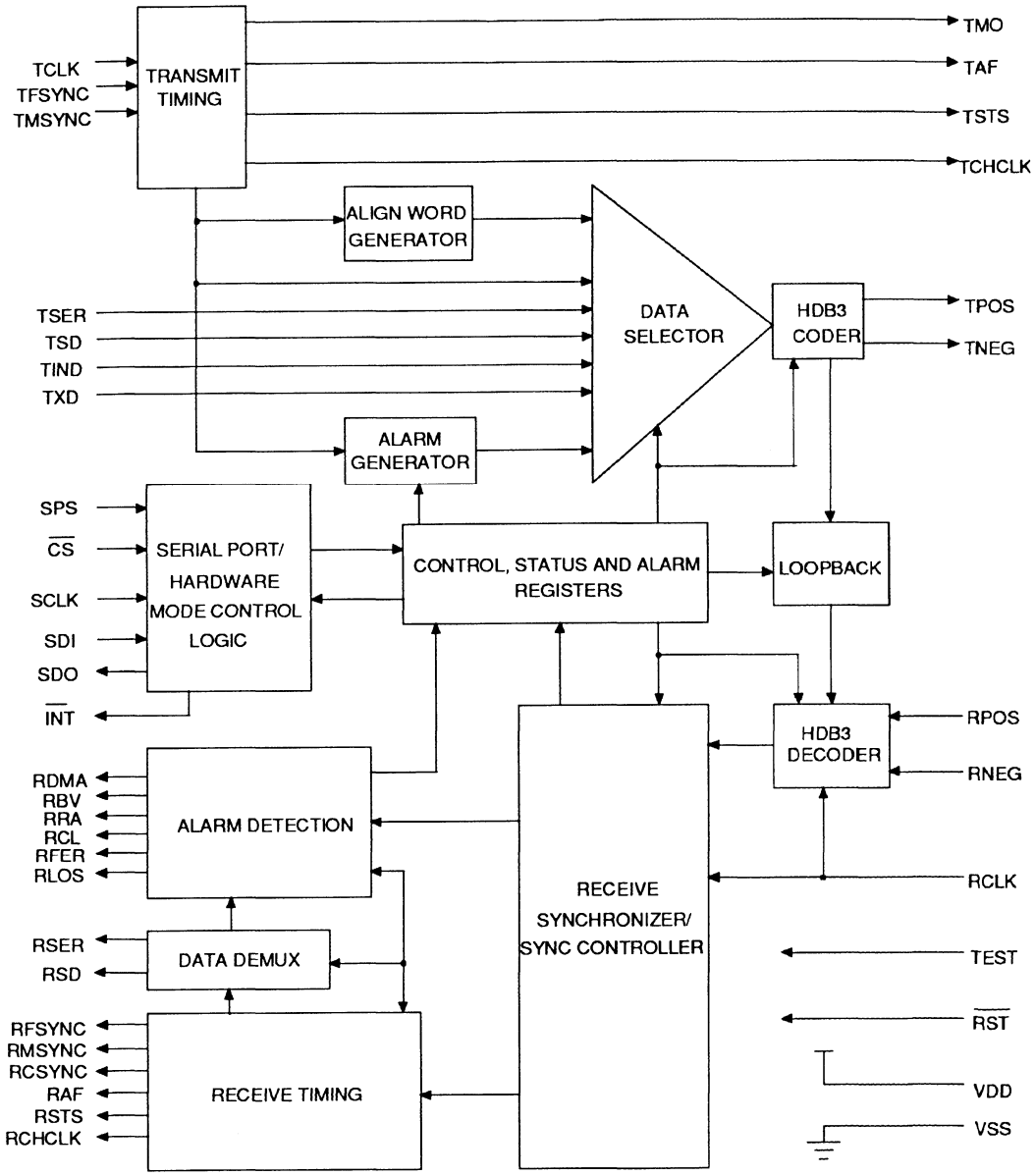
DESCRIPTION

The DS2181 is designed for use in CEPT networks and supports all logical requirements of CCITT Red Book Recommendations G.704 and G.732. The transmit side generates framing patterns and CRC4 codes, formats outgoing channel and signalling data, and produces network alarm codes when enabled. The receive side decodes the incoming data and establishes frame, CAS multiframe, and CRC4 multiframe alignments. Once synchronized, the device extracts channel, signalling, and alarm data.

A serial port allows access to 14 on-chip control and status registers in the processor mode. In this mode, a host processor controls such features such as error logging, per-channel code manipulation, and alteration of the receive synchronizer algorithm.

The hardware mode is intended for preliminary system prototyping and/or retrofitting into existing systems. This mode requires no host processor and disables special features available in the processor mode.

DS2181 BLOCK DIAGRAM Figure 1



TRANSMIT PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**TMSYNC**	I	**Transmit Multiframe Sync.** Low-high transition establishes start of CAS and/or CRC4 multiframe. Can be tied low, allowing internal multiframe counter to run free.
2	**TFSYNC**	I	**Transmit Frame Sync.** Low-high transition every frame period establishes frame boundaries. Can be tied low, allowing TMSYNC to establish frame boundaries.
3	**TCLK**	I	**Transmit Clock.** 2.048 MHz primary clock.
4	**TCHCLK**	O	**Transmit Channel Clock.** 256 KHz clock which identifies timeslot boundaries. Useful for parallel-to-serial conversion of channel data.
5	**TSER**	I	**Transmit Serial Data.** NRZ data input, sampled on falling edges of TCLK.
6	**TMO**	O	**Transmit Multiframe Out.** Output of multiframe counter; high during frame 0, low otherwise.
7	**TXD**	I	**Transmit Extra Data.** Sampled on falling edge of TCLK during bit times 5, 7, and 8 of timeslot 16 in frame 0 when CAS signalling is enabled.
8	**TSTS**	O	**Transmit Signalling Timeslot.** High during timeslot 16 of every frame, low otherwise.
9	**TSD**	I	**Transmit Signalling Data.** CAS signalling data input; sampled on falling edges of TCLK for insertion into outgoing timeslot 16 when enabled.
10	**TIND**	I	**Transmit International and National Data.** Sampled on falling edge of TCLK during bit 1 time of timeslot 0 every frame (international) and/or during bit times 4 through 8 of timeslot 0 during non-align frames (national) when enabled.
11	**TAF**	O	**Transmit Alignment Frame.** High during frames containing the frame alignment signal, low otherwise.
12 13	**TPOS** **TNEG**	O	**Transmit Bipolar Data Outputs.** Updated on rising edge of TCLK.

5

RECEIVE PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DECRIPTION
21	**RRA**	O	**Receive Remote Alarm.** Transitions high when alarm detected; returns low when alarm cleared.
22	**RDMA**	O	**Receive Distant Multiframe Alarm.** Transitions high when alarm detected; returns low when alarm cleared.
23	**RAF**	O	**Receive Alignment Frame.** High during frames containing the frame alignment signal, low otherwise.
24	**RCLK**	I	**Receive Clock.** 2.048 MHz primary clock.
25	**RCHCLK**	O	**Receive Channel Clock.** 256 KHz clock, identifies timeslot boundaries; useful for serial-to-parallel conversion of channel data.
26	**RSER**	O	**Receive Serial Data.** Received NRZ data, updated on rising edges of RCLK.
27	**RFSYNC**	O	**Receive Frame Sync.** Trailing edge indicates start of frame.
28	**RMSYNC**	O	**Receive Multiframe Sync.** Low-high transition indicates start of CAS multiframe; held high during frame 0.
29	**RSD**	O	**Receive Signalling Data.** Extracted timeslot 16 data; updated on rising edge of RCLK.
30	**RSTS**	O	**Receive Signalling Timeslot.** High during timeslot 16 of every frame, low otherwise.
31	**RCSYNC**	O	**Receive CRC4 Sync.** Low-high transition indicates start of CRC4 multiframe; held high during CRC4 frames 0 thru 7 and held low during frames 8 through 15.
33	**RST**	I	**Reset.** Must be asserted during device power-up and when changing to/from the hardware mode.
34 35	**RPOS** **RNEG**	I	**Receive Bipolar Data.** Sampled on falling edges of RCLK.
36	**RCL**	O	**Receive Carrier Loss.** Low-high transition indicates loss of carrier.

37	**RBV**	O	**Receive Bipolar Violation.** Pulses high during detected bipolar violations.
38	**RFER**	O	**Receive Frame Error.** Pulses high when frame alignment, CAS multiframe alignment or CRC4 words received in error.
39	**RLOS**	O	**Receive Loss of Sync.** Indicates synchronizer status; high when frame, CAS and/or CRC4 multiframe search underway, low otherwise.

PORT PIN DESCRIPTION Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
14	**INT**	O	**Receive Alarm Interrupt.** Flags host controller during alarm conditions. Active low; open drain output.
15	**SDI**	I	**Serial Data In.** Data for on-chip control registers; sampled on rising edge of SCLK.
16	**SDO**	O	**Serial Data Out.** Control and status data from on-chip registers. Updated on falling edge of SCLK; tri-stated during port write or when CS\ is high.
17	**CS**	I	**Chip Select.** Must be low to write or read the serial port.
18	**SCLK**	I	**Serial Data Clock.** Used to write or read the serial port registers.
19	**SPS**	I	**Serial Port Select.** Tie to VDD to select the serial port. Tie to VSS to select the hardware mode.

POWER AND TEST PIN DESCRIPTION Table 4

PIN	SYMBOL	TYPE	DESCRIPTION
20	**VSS**	-	**Signal Ground.** 0.0 volts.
32	**TEST**	I	**Test Mode.** Tie to VSS for normal operation.
40	**VDD**	-	**Positive Supply.** 5.0 volts.

REGISTER SUMMARY Table 5

REGISTER	ADDRESS	T/R[1]	DESCRIPTION/FUNCTION
RIMR	0000	R	**Receive Interrupt Mask Register.** Allows masking of alarm generated interrupts.
RSR	0001	R[2]	**Receive Status Register.** Reports all receive alarm conditions.
BVCR	0010	R	**Bipolar Violation Count Register.** 8-bit presettable counter which records individual bipolar violations.
CECR	0011	R	**CRC4 Error Count Register.** 8-bit presettable counter which records individual CRC4 errors.
FECR	0100	R	**Frame Error Count Register.** 8-bit presettable counter which logs individual errors in the received frame alignment signal.
RCR	0101	R	**Receive Control Register.** Establishes receive side operating characteristics.
CCR	0110	T/R	**Common Control Register.** Establishes additional operating characteristics for transmit and receive sides.
TCR	0111	T	**Transmit Control Register.** Establishes transmit side operation characteristics.
TIR1 **TIR2** **TIR3** **TIR4**	1000 1001 1010 1011	T	**Transmit Idle Registers.** Designates which outgoing timeslots are to be substituted with idle code.
TINR	1100	T	**Transmit International and National Register.** When enabled via the TCR, contents inserted into the outgoing national and/or international bit positions.
TXR	1101	T	**Transmit Extra Register.** When enabled via the TCR, contents inserted into the outgoing extra bit positions.

NOTES:
1. Transmit or receive side register.
2. RSR is a read-only register; all other registers are read/write.
3. Reserved bit locations must be programmed to zero.

SERIAL PORT INTERFACE

Pins 14 through 18 of the DS2181 serve as a microprocessor/microcontroller-compatible serial port. 14 on-chip registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces.

Port read/write timing is unrelated to the chip transmit and receive timing, allowing asynchronous reads and/or writes by the host. The timing set is identical to that of 8051-type microcontrollers operating in serial port mode 0. For proper operation of the port and the transmit and receive registers, the user should provide TCLK and RCLK as well as SCLK.

ADDRESS/COMMAND

An address/command byte write must precede any read or write of the port registers. The first bit written (LSB) of the address/command byte specifies read or write. The following nibble identifies register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables the burst mode when set; the burst mode allows consecutive reading or writing of all register data. *Data is written to and read from the port LSB first.*

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the CS\ input low. Data is sampled on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of written register contents. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated and SDO tri-stated when CS\ returns to high.

CLOCKS

To access the serial port registers both TCLK and RCLK are required along with the SCLK. The TCLK and RCLK are used to internally access the transmit and receive registers; respectively. The CCR is considered a receive register for this purpose.

DATA I/O

Following the 8 SCLK cycles that input the address/command byte, data at SDI is strobed into the addressed register on the next 8 SCLK cycles (register write) or data is presented at SDO on the next 8 SCLK cycles (register read). SDO is tri-stated during writes and may be tied to SDI in applications where the host processor has bidirectional I/O capability.

BURST MODE

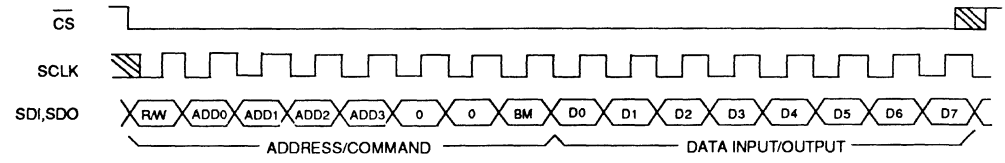
The burst mode allows all on-chip registers to be consecutively read or written by the host processor. This feature minimizes device initialization time on system power-up or reset. Burst mode is initiated when ACB.7 is set and the address nibble is 0000. *All registers must be read or written during the burst mode. If CS\ transitions high before the burst is complete, data validity is not guaranteed.*

ACB: ADDRESS COMMAND BYTE Figure 2

(MSB)							(LSB)
BM	--	--	**ADD3**	**ADD2**	**ADD1**	**ADD0**	**R/W**

SYMBOL	POSITION	NAME AND DESCRIPTION
BM	ACB.7	**Burst Mode.** If set (and ACB.1 through ACB.4 = 0) burst read or write is enabled.
--	ACB.6	Reserved; must be 0 for proper operation.
--	ACB.5	Reserved; must be 0 for proper operation.
ADD3	ACB.4	MSB of register address.
ADD2	ACB.3	
ADD1	ACB.2	
ADD0	ACB.1	LSB of register address.
R/W	ACB.0	**Read/Write select.** 0 = Write addressed register. 1 = Read addressed register.

SERIAL PORT READ/WRITE Figure 3



NOTES:

1. SDI sampled on rising edge of SCLK.
2. SDO updated on falling edge of SCLK.

TCR: TRANSMIT CONTROL REGISTER Figure 4

(MSB) (LSB)

TUA1	TSS	TSM	INBS	NBS	XBS	TSA1	ODM

SYMBOL	POSITION	NAME AND DESCRIPTION
TUA1	TCR.7	**Transmit Unframed All Ones** 0 = Normal operation. 1 = Replace outgoing data at TPOS and TNEG with unframed all ones code.
TSS	TCR.6	**Transmit Signalling Select**[1] 0 = Signalling data embedded in the serial bit stream is sampled at TSER during timeslot 16. 1 = Signalling data is channel associated and sampled at TSD as shown in Table 6.
TSM	TCR.5	**Transmit Signalling Mode**[1] 0 = Channel Associated Signalling (CAS). 1 = Common Channel Signalling (CCS).
INBS	TCR.4	**International Bit Select** 0 = Sample international bit at TIND. 1 = Outgoing international bit = TINR.7.
NBS	TCR.3	**National Bit Select** 0 = Sample national bits at TIND. 1 = Source outgoing national bits from TINR.4 through TINR.0.
XBS	TCR.2	**Extra Bit Select** 0 = Sample extra bits at TXD. 1 = Source extra bits from TXR.0 through TXR.1 and TXR.3.
TSA1	TCR.1	**Transmit Signalling All Ones** 0 = Normal operation. 1 = Force contents of timeslot 16 in all frames to all ones.
ODM	TCR.0	**Output Data Mode** 0 = TPOS and TNEG outputs are 100% duty cycle. 1 = TPOS and TNEG outputs are 50% duty cycle.

5

NOTE:

1. When the common channel signalling mode is enabled (TCR.5 = 1), the TSD input is disabled internally; all timeslot 16 data is sampled at TSER.

CCR: COMMON CONTROL REGISTER Figure 5

(MSB)							(LSB)
--	TAFP	THDE	RHDE	TCE	RCE	--	LLB

SYMBOL	POSITION	NAME AND DESCRIPTION
--	CCR.7	Reserved; must be 0 for proper operation.
TAFP	CCR.6	**Transmit Align Frame Position**[1] When clear, the CAS multiframe begins with a frame containing the frame alignment signal. When set, the CAS multiframe begins with a frame not containing the frame alignment signal.
THDE	CCR.5	**Transmit HDB3 Enable** 0 = Outgoing data at TPOS and TNEG is AMI coded. 1 = Outgoing data at TPOS and TNEG is HDB3 coded.
RHDE	CCR.4	**Receive HDB3 Enable** 0 = Incoming data at RPOS and RNEG is AMI coded. 1 = Incoming data at RPOS and RNEG is HDB3 coded.
TCE	CCR.3	**Transmit CRC4 Enable** When set, outgoing international bit positions in frames 0 through 12 and 14 are replaced by CRC4 multiframe alignment and checksum words.
RCE	CCR.2	**Receive CRC4 Enable** 0 = Disable CRC4 multiframe synchronizer. 1 = Enable CRC4 synchronizer; search for CRC4 multiframe alignment once frame alignment complete.
- -	CCR.1	Reserved; must be 0 for proper operation.
LLB	CCR.0	**Local Loopback** 0 = Normal operation. 1 = Internally loop TPOS, TNEG and TCLK to RPOS, RNEG and RCLK.

NOTES:

1. This bit must be cleared when CRC4 multiframe mode is enabled (CCR.3 = 1); its state does not affect CCS framing (RCR.5 = 1).
2. CCR is considered a receive register and operates from RCLK and SCLK.

RCR: RECEIVE CONTROL REGISTER Figure 6

(MSB) (LSB)

--	--	RSM	CMRC	CMSC	FRC	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
--	RCR.7	Reserved; must be 0 for proper operation.
--	RCR.6	Reserved; must be 0 for proper operation.
RSM	RCR.5	**Received Signalling Mode** 0 = Channel Associated Signalling (CAS). 1 = Common Channel Signalling (CCS).
CMSC	RCR.4	**CAS Multiframe Sync Criteria** 0 = Declare sync when fixed sync criteria met. 1 = Declare sync when fixed criteria are met and two additional consecutive valid multiframe alignment signals are detected.
CMRC	RCR.3	**CAS Multiframe Resync Criteria** 0 = Utilize only fixed resync criteria. 1 = Resync if fixed criteria met and/or if two consecutive timeslot 16 words have values of zero in the first four MSB positions (0000xxxx).
FRC	RCR.2	**Frame Resync Criteria** 0 = Utilize only fixed resync criteria. 1 = Resync if fixed criteria met and/or if bit 2 in timeslot 0 of non-align frames is received in error on three consecutive occasions.
SYNCE	RCR.1	**Sync Enable** If clear, the synchronizer will automatically begin resync if error criteria are met. If high, no auto resync occurs.
RESYNC	RCR.0	**Resync** When toggled low to high, the receive synchronizer will initate immediately. The bit must be cleared, then set again for subsequent resyncs.

CEPT FRAME STRUCTURE

The CEPT frame is made up of 32 8-bit channels (timeslots) numbered from 0 to 31. The frame alignment signal in bit positions 2 through 8 of timeslot 0 of every other frame is independent of the various multiframe modes described below. Outputs TAF and RAF indicate frames which contain the alignment signal. Timeslot 0 of frames not containing the frame alignment signal is used for alarm and national data.

CAS SIGNALLING

CEPT networks support Channel Associated Signalling (CAS) or Common Channel Signalling (CCS). These signalling modes are independently selectable for transmit and receive sides.

CAS (selected when TCR.5 = 0 and/or when RCR.5 = 0) is a bit-oriented signalling technique which utilizes a 16-frame multiframe. The multiframe alignment signal (0-hex), extra and alarm bits occupy timeslot 16 of frame 0. Timeslot 16 of the remaining 15 frames is reserved for channel signalling data. Four signalling bits (A, B, C and D) are transmitted once per multiframe as shown in Figure 7. Input TMSYNC establishes the transmitted CAS multiframe position. Signalling data can be sourced from input TSD (TCR.6 = 1) or multiplexed into TSER (TCR.6 = 0).

CCS SIGNALLING

CCS (selected when TCR.5 = 1 and/or when RCR.1 = 1) utilizes all bit positions of timeslot 16 in every frame for message-oriented signalling data transmission. In CCS mode one can use either timeslot 16 or any one of the other 30 data channels for message-oriented signalling. The CCS mode has no multiframe structure and the insertion of CAS multiframe alignment, distant multiframe alarm and/or extra bits into timeslot 16 is disabled. TSER is the source of timeslot 16 data.

CRC4 CODING

The need for enhanced error monitoring capability and additional protection against emulators of the frame alignment word has led to the development of a cyclic redundancy check (CRC) procedure. When enabled via CCR.2 and/or CCR.3, CRC4 coding replaces the international bit positions in frames 0 through 12 and 14 with a CRC4 multiframe alignment pattern and associated checksum words. The CRC4 multiframe must begin with a frame containing the frame alignment signal (CCR.6 = 0). A rising edge at TMSYNC establishes the CRC4 multiframe alignment (TMSYNC will also establish outgoing CAS multiframe alignment if enabled via TCR.5).

Incoming CRC4 multiframe alignment is indicated by RCSYNC. Detected CRC4 checksum errors are reported at output RFER and logged in the CECR.

RECEIVE SYNCHRONIZER

The fixed characteristics of the receive synchronizer may be modified by use of programmable characteristics resident in the RCR and CCR. Sync criteria must be met before synchronization is declared. Resync criteria establish error occurrences which will cause an auto-resync event when enabled (RCR.1 = 0).

The receive synchronizer searches for the frame alignment pattern first. Once identified, the output timing set associated with the framing pattern (all outputs except RCSYNC) is updated to that new alignment. If enabled, the synchronizer then begins CAS and/or CRC4 multiframe search; outputs RMSYNC and/or RCSYNC are then updated. Output RLOS is held high during the entire resync process, then transitions low after the last output timing update indicating resync is complete.

FIXED FRAME SYNC CRITERIA

Valid frame sync is assumed when the correct frame alignment signal is present in frame N and frame N + 2 and not present in frame N + 1 (bit 2 of timeslot 0 of Frame N + 1 is also checked for 1). CAS and/or CRC4 multiframe alignment search is initiated when the frame search is complete if enabled via RCR.5 and/or CCR.2.

FIXED CAS MULTIFRAME SYNC CRITERIA

CAS multiframe sync is declared when the multiframe alignment pattern is properly detected and timeslot 16 of the previous frame contains code other than zeros. If no valid pattern can be found in 12 to 14 milliseconds, frame search is restarted.

FIXED CRC4 MULTIFRAME SYNC CRITERIA

CRC4 multiframe sync is declared if at least two valid CRC4 multiframe alignment signals are found within 12 to 14 milliseconds after frame alignment is completed. If not found within 12 to 14 milliseconds, frame search is restarted. The search for the multiframe alignment signal is performed in timeslot 0 of frames not containing the frame alignment signal.

FIXED FRAME RESYNC CRITERIA

When enabled via RCR.1, the device will automatically initiate frame search whenever the frame alignment word is received in error three consecutive times.

FIXED CAS MULTIFRAME RESYNC CRITERIA

When enabled via RCR.1, the device will automatically initiate frame search whenever two consecutive CAS multiframe alignment words are received in error.

CAS SIGNALLING SOURCE

CAS applications sample signalling data at TSER when TCR.6 = 0; an on-chip data multiplexer accepts channel-associated data input at TSD when TCR.6 = 1. The data multiplexer must be disabled (TCR.6 = 0) when the CCS mode is enabled (TCR.5 = 1).

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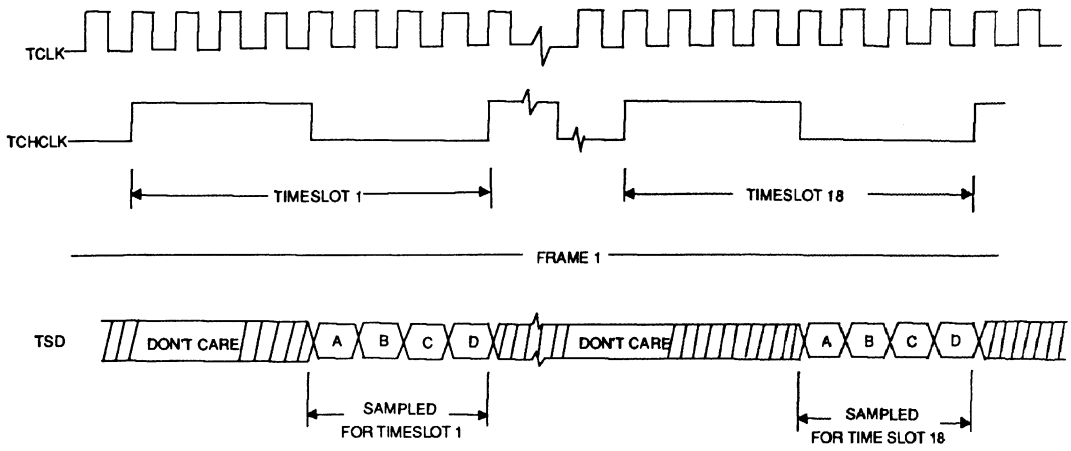
TSD INPUT TIMING (TCR.6 = 1; TCR.5 = 0) Table 6

Frame #	Timeslot signalling data sampled at TSD
0	17
1	1,18
2	2,19
3	3,20
4	4,21
5	5,22
6	6,23
7	7,24
8	8,25
9	9,26
10	0,27
11	11,28
12	12,29
13	13,30
14	14,31
15	15

NOTES:

1. A, B, C and D data is sampled on falling edges of TCLK during bit times 5, 6, 7 and 8 of timeslots indicated.

TSD INPUT TIMING Figure 7



CAS OUTPUT FORMAT IN TIMESLOT 16 Figure 8

Frame 0[1]	Frame 1			Frame 15	
0000 XYXX	ABCD for timeslot 1	ABCD for timeslot 17	- - -	ABCD for timeslot 15	ABCD for timeslot 31

NOTES:

1. Timeslot 16 of frame 0 is reserved for the multiframe alignment word (0000), distant multiframe alarm (Y) and extra bits (X-XX).

TINR: TRANSMIT INTERNATIONAL AND NATIONAL REGISTER Figure 9

(MSB) (LSB)

INB	--	TRA	NB4	NB5	NB6	NB7	NB8

SYMBOL	POSITION	NAME AND DESCRIPTION
INB	TINR.7	**International Bit.** Inserted into the outgoing data stream when TCR.4 = 1.
--	TINR.6	Reserved; must be 0 for proper operation.
TRA	TINR.5	**Transmit Remote Alarm** 0 = Normal operation; bit 3 of timeslot 0 in non-alignment frames clear. 1 = Alarm condition; bit 3 of timeslot 0 in non-align frames set.
NB4	TINR.4	**Transmit National Bits.** Inserted into the outgoing data stream at TPOS and TNEG when TCR.3 = 1
NB5	TINR.3	
NB6	TINR.2	
NB7	TINR.1	
NB8	TINR.0	

TRANSMIT INTERNATIONAL AND NATIONAL DATA

Bit 1 of timeslot 0 in all frames is known as the international bit. When TCR.4 = 1, the transmitted international bit is sourced from TINR.7. When TCR.4 = 0, the transmitted international bit is sampled at TIND during the first bit period of each frame. The international bit positions in all outgoing frames except 13 and 15 are replaced by CRC4 codewords and the CRC4 multiframe alignment signal when CCR.3 = 1.

Bits 4 through 8 of timeslot 0 in non-align frames are reserved for national use. When TCR.3 = 1, the transmitted national bits are sourced from register locations TINR.4 through TINR.0. If TCR.3 = 0, the national bits are sampled at TIND during bit times 4 through 8 of timeslot 0 in non-align frames.

Reserved bit positions in the TINR must be set to 0 when written; those bits can be 0 or 1 when read.

TXR: TRANSMIT EXTRA REGISTER Figure 10

(MSB)							(LSB)
--	--	--	--	**XB1**	**TDMA**	**XB2**	**XB3**

SYMBOL	POSITION	NAME AND DESCRIPTION
--	TXR.7	Reserved; must be 0 for proper operation.
--	TXR.6	Reserved; must be 0 for proper operation.
--	TXR.5	Reserved; must be 0 for proper operation.
--	TXR.4	Reserved; must be 0 for proper operation.
XB1	TXR.3	**Extra Bit 1**
TDMA	TXR.2	**Transmit Distant Multiframe Alarm** 0 = Normal operation; bit 6 of timeslot 16 in frame 0 clear. 1 = Alarm condition; bit 6 of timeslot 16 in frame 0 set.
XB2	TXR.1	**Extra Bit 2**
XB3	TXR.0	**Extra Bit 3**

TRANSMIT EXTRA DATA

In the CAS mode, timeslot 16 of frame 0 contains the multiframe alignment pattern, extra bits and the distant multiframe alarm. When CAS is enabled (TCR.5 = 0), the extra bits are sourced from TXR.0, TXR.1 and TXR.3 (TCR.2 = 1) or the extra bits are sampled externally at TXD during the extra bit time (TCR.2 = 0). The extra bits, alignment pattern and alarm signal are not utilized in the CCS mode (TCR.5 = 1); input TSER overwrites all timeslot 16 bit positions.

Reserved bit positions in the TXR must be set to 0 when written; those bits can be 0 or 1 when read.

TIR1 - TIR4: TRANSMIT IDLE REGISTERS Figure 11

(MSB)							(LSB)	
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0[1]	TIR1
TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8	TIR2
TS23	TS22	TS21	TS20	TS19	TS18	TS17	TS16[1]	TIR3
TS31	TS30	TS29	TS28	TS27	TS26	TS25	TS24	TIR4

SYMBOL POSITION		NAME AND DESCRIPTION
TS31	TIR4.7	**Transmit Idle Registers.** Each of these bit positions represents
TSO	TIR1.0	a timeslot in the outgoing stream at TPOS and TNEG; when set, the contents of that timeslot are forced to idle code (11010101).

NOTE: TS0 and TS16 are not affected by the idle register.

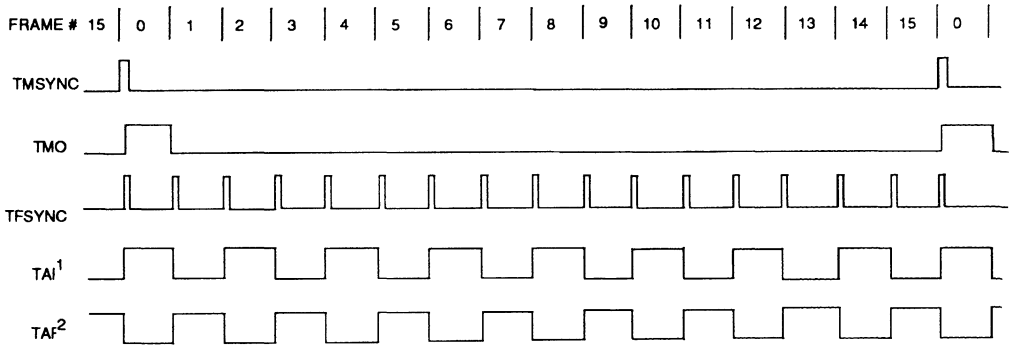
TRANSMIT TIMING

A low-high transition at TMSYNC once per multiframe (every 2 milliseconds) or at a multiple of the multiframe rate establishes outgoing CAS and/or CRC4 multiframe alignment. Output TMO indicates that alignment. A low-high transition at TFSYNC at the frame rate (125 us) or at a multiple of the frame rate establishes the outgoing frame position. Output TAF indicates that alignment.

TMSYNC and/or TFSYNC can be tied low by the user, in which case the arbitrary frame and multiframe alignment established by the device will be indicated at TMO and TAF.

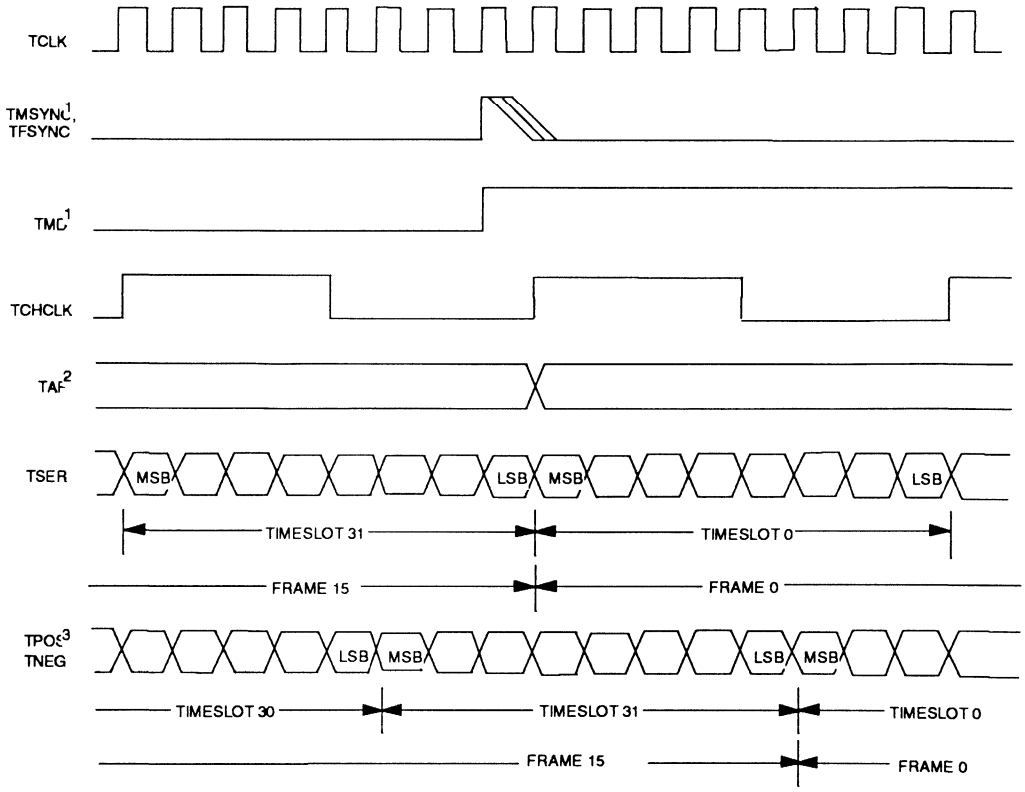
Output TAF also indicates frames containing the frame alignment signal. Those frames can be even or odd numbering frames of the outgoing CAS multiframe (CCR.6).

TRANSMIT MULTIFRAME TIMING Figure 12



NOTES:
1. Alignment frames are even frames of the CAS and/or CRC4 multiframes (CCR.6 = 0).
2. Alignment frames are odd frames of the CAS multiframe (CCR.6 = 1).

TRANSMIT MULTIFRAME BOUNDARY TIMING Figure 13



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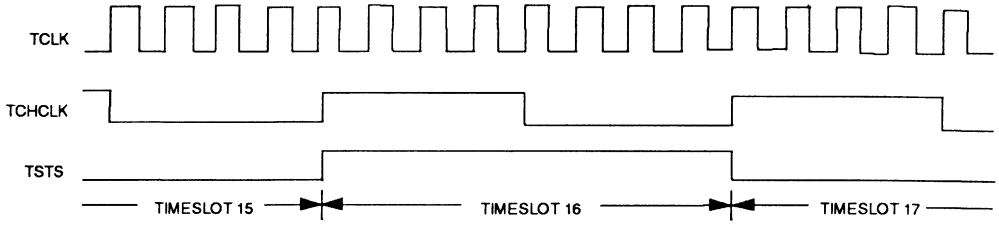
NOTES:

1. Low-high transitions on TMSYNC and/or TFSYNC must occur one TLCK period early with respect to actual frame and multiframe boundaries. TMO follows the rising edge of TMSYNC or TFSYNC.
2. TAF transitions on true frame boundaries.
3. Delay from TSER to TPOS; TNEG is five TCLK periods.

TRANSMIT SIGNALLING TIMESLOT TIMING Figure 14



RECEIVE SIGNALLING

Receive signalling data is available at two outputs: RSER and RSD. RSER outputs the signalling data in timeslot 16 at RSER. The signalling data is also extracted from timeslot 16 and presented at RSD during the timeslots shown in Table 7. This channel-associated signalling simplifies CAS system design.

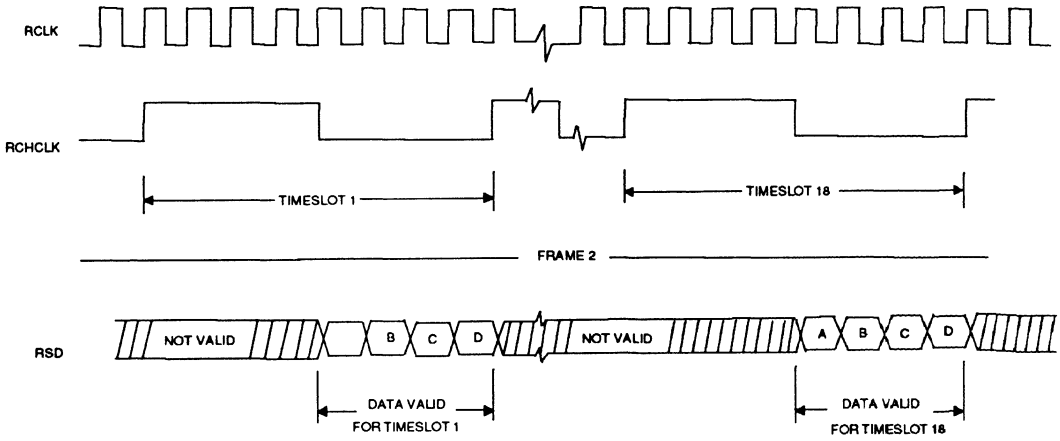
RECEIVE SIGNALLING Table 7

Frame #	RSD[1] valid during timeslot #
0	15,$^{-2}$
1	$^{-2}$,17
2	1,18
3	2,19
4	3,20
5	4,21
6	5,22
7	6,23
8	7,24
9	8,25
10	9,26
11	10,27
12	11,28
13	12,29
14	13,30
15	4,31

NOTES: applicable only to CAS systems

1. RSD is valid for the least significant nibble in each indicated timeslot. Timeslot A data appears in bit 5, B in bit 6, C in bit 7 and D in bit 8.
2. RSD does not output valid data during timeslots 0 and 16.

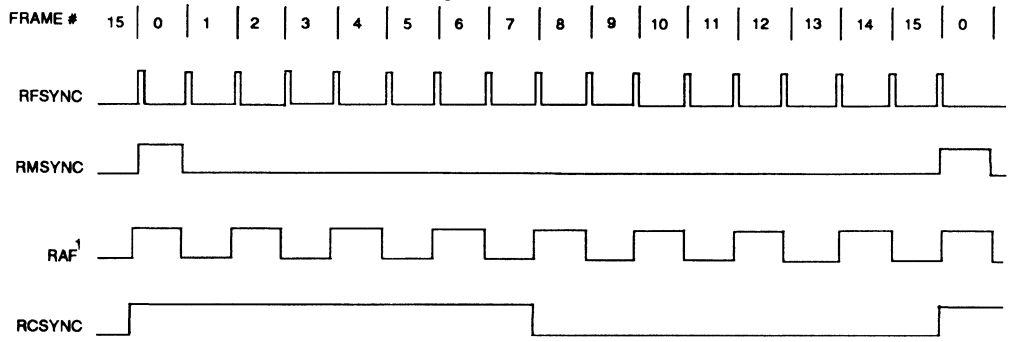
RSD TIMING Figure 15



RECEIVE TIMING

The receive side output timing set is identical to that found on the transmit side. The user can tie receive outputs directly to the transmit inputs for drop and insert applications. The received data of RPOS, RNEG appear at RSER after six RCLK delays, without any change except for the HDB3-to-NRZ conversion when HDB3 is enabled.

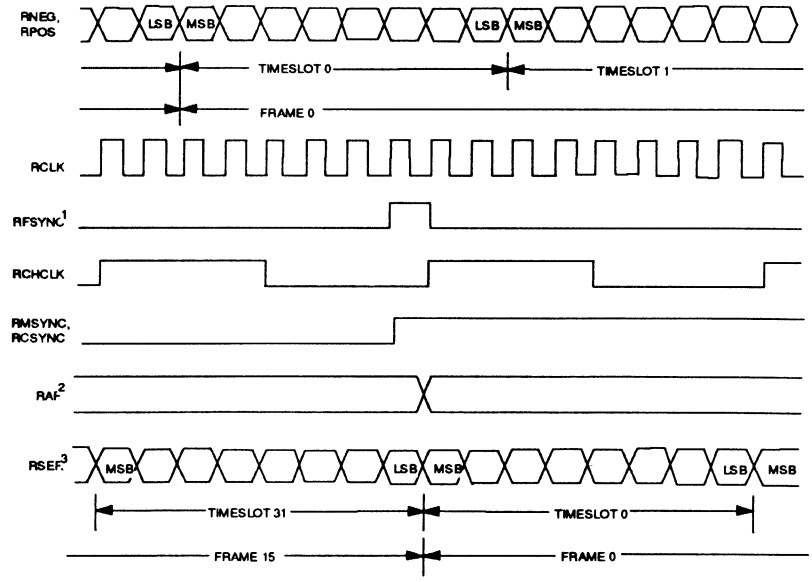
RECEIVE MULTIFRAME TIMING Figure 16



NOTE:

1. The CAS multiframe can start with an align or non-align frame. The CRC4 multiframe always starts with an align frame.

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 17



NOTES:

1. Low-high transitions on RMSYNC and RFSYNC occur one RCLK period early with respect to actual frame and multiframe boundaries.
2. RAF transitions on true frame boundaries.
3. Delay from RPOS, RNEG to RSER is six RCLK periods.

RSR: RECEIVE STATUS REGISTER Figure 18

(MSB) (LSB)

RRA	RDMA	RSA1	RUA1	FSERR	MFSERR	RLOS	ECS

SYMBOL	POSITION	NAME AND DESCRIPTION
RRA	RSR.7	**Receive Remote Alarm.** Set when bit 3 of timeslot 0 in non-align frames set for three consecutive non-align frames.
RDMA	RSR.6	**Receive Distant Multiframe Alarm.** Set when bit 6 of timeslot 16 in frame 0 set for three consecutive multiframes.
RSA1	RSR.5	**Receive Signalling All Ones.** Set when contents of timeslot 16 have been all ones for two consecutive frames.
RUA1	RSR.4	**Receive Unframed All Ones.** Set when < 3 bit positions of the last align and non-align frames received have been 0.
FSERR	RSR.3	**Frame Resync Criteria Met.** Set when the frame error criteria are met; also the frame resync is initiated if RCR.1 = 0.
MFSERR	RSR.2	**CAS Multiframe Resync Criteria Met.** Set when the CAS multiframe error criteria are met; also the frame resync is initiated if RCR.1 = 0.
RLOS	RSR.1	**Receive Loss of Sync.** Set when resync is in progress.
ECS	RSR.0	**Error Count Saturation.** Set when any of the on-chip counters at FECR, CECR or BVCR saturates.

NOTES:

1. When in the CCS mode, the RDMA flag bit and the RDMA pin have no significance. It will be set when bit 6 of timeslot 16 in frame 0 is set for three consecutive multiframes in either CAS or CCS mode.

RIMR: RECEIVE INTERRUPT MASK REGISTER Figure 19

(MSB) (LSB)

RRA	RDMA	RSA1	RUA1	FSERR	MFSERR	RLOS	ECS

SYMBOL	POSITION	NAME AND DESCRIPTION
RRA	RIMR.7	**Receive Remote Alarm** 1 = Interrupt enabled 0 = Interrupt masked
RDMA	RIMR.6	**Receive Distant Multiframe Alarm.** 1 = Interrupt enabled 0 = Interrupt masked
RSA1	RIMR.5	**Receive Signalling All Ones.** 1 = Interrupt enabled 0 = Interrupt masked
RUA1	RIMR.4	**Receive Unframed All Ones.** 1 = Interrupt enabled 0 = Interrupt masked
FSERR	RIMR.3	**Frame Resync Criteria Met.** 1 = Interrupt enabled 0 = Interrupt masked
MFSERR	RIMR.2	**CAS Multiframe Resync Criteria Met.** 1 = Interrupt enabled 0 = Interrupt masked
RLOS	RIMR.1	**Receive Loss of Sync.** 1 = Interrupt enabled 0 = Interrupt masked
ECS	RIMR.0	**Error Count Saturation.** 1 = Interrupt enabled 0 = Interrupt masked

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ALARM REPORTING AND INTERRUPT SERVICING

Alarm and error conditions are reported at outputs and the RSR. Use of the RSR and error count registers simplifies system error monitoring. The RSR can be read in one of two ways: a burst read does not disturb the RSR contents; a direct read will clear all bits set in the RSR unless the alarm condition which set them is still active.

Interrupts are enabled via the RIMR and are generated whenever an alarm or error condition sets an RSR bit. The host controller must service the transceiver in order to clear an interrupt condition. Clearing the appropriate RIMR bit will unconditionally clear an interrupt.

BVCR: BIPOLAR VIOLATION COUNT REGISTER Figure 20

(MSB) (LSB)

BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

SYMBOL	POSITION	NAME AND DESCRIPTION
BVD7	BVCR.7	MSB of bipolar violation count.
BVD0	BVCR.0	LSB of bipolar violation count.

CECR: CRC4 ERROR COUNT REGISTER Figure 21

(MSB) (LSB)

CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC7	BVCR.7	MSB of CRC4 Error Count.
CRC0	BVCR.0	LSB of CRC4 Error Count.

FECR: FRAME ERROR COUNT REGISTER Figure 22

(MSB) (LSB)

FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0

SYMBOL	POSITION	NAME AND DESCRIPTION
FE7	FECR.7	MSB of frame error count.
FE0	FECR.0	LSB of frame error count.

ERROR LOGGING

The BVCR, CECR and FECR contain 8-bit binary up counters which increment on individual bipolar violations, CRC4 code word errors (when CCR.2 = 1), and word errors in the frame alignment signal. Each counter saturates at 255. Once saturated, each following error occurrence will generate an interrupt (RIMR.0 = 1) until the register is reprogrammed to a value other than FF (hex). Presetting the registers allows the user to establish specific error count thresholds; the counter will count up to saturation from the preset value. The BVCR increments at all times (regardless of sync status). CECR and FECR increments are disabled whenever resync is in progress (RLOS high).

ALARM OUTPUTS

Alarm conditions are also reported real time at alarm outputs. These outputs can be used with off-chip logic to complement the on-chip error reporting capability of the DS2181. In the hardware mode, they are the only alarm reporting means available.

RLOS

The RLOS output indicates the status of the receive synchronizer. When high, frame, CAS multiframe and/or CRC4 multiframe synchronization is in progress. A high-low transition indicates resync is complete. The RLOS bit (RSR.1) is a latched version of the RLOS output.

RRA

The remote alarm output transitions high when a remote alarm is detected. A high-low transition indicates the alarm condition has been cleared. The alarm condition is defined as bit 3 of timeslot 0 set for three consecutive non-align frames. The alarm state is cleared when bit 3 has been clear for three consecutive non-align frames. The RRA bit (RSR.7) is a latched version of the RRA output.

RBV

RBV outputs one RCLK pulse when the accused bit emerges at RSER. RBV will return low when RCLK goes low, and RBV pin bipolar violations are logged in the BVCR. The RBV pin provides a pulse for every violation which can be counted externally.

RDMA

RDMA transitions high when bit 6 of timeslot 16 in frame 0 is set for three consecutive occasions and returns low when the bit is clear for three consecutive occasions. The RDMA bit (RSR.6) is a latched version of the RDMA output.

RCL

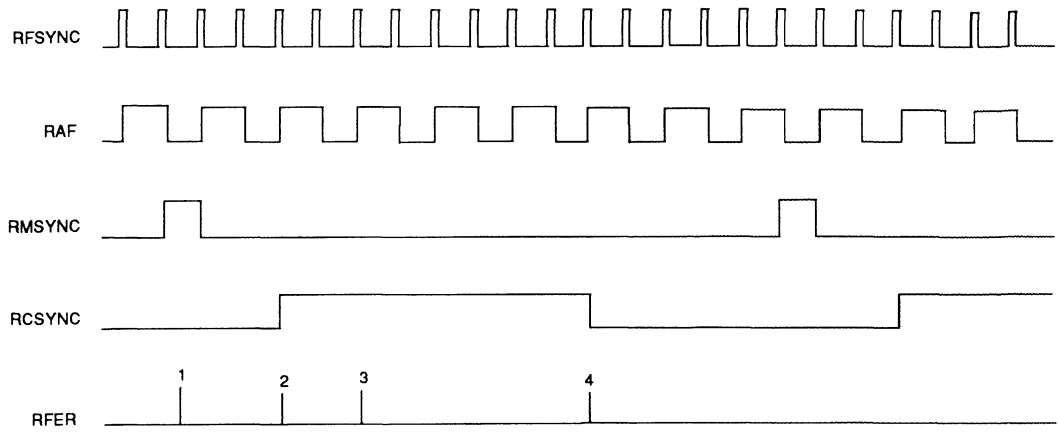
RCL transitions high after 32 consecutive zeros appear at RPOS and RNEG; it goes low at the next one occurrence.

RFER

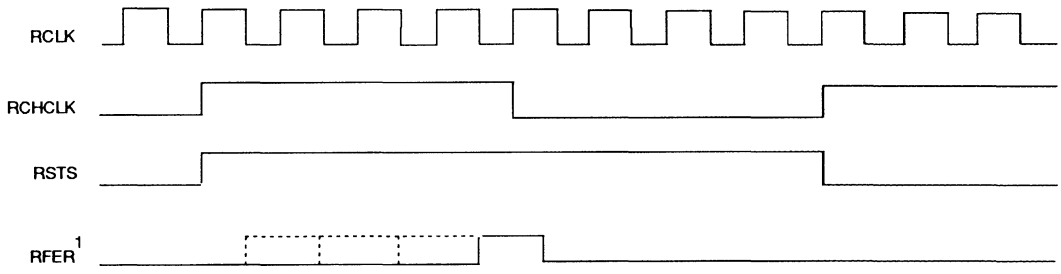
The RFER output transitions high when received frame alignment, CAS multiframe alignment and/or CRC4 code words are in error. The FECR and CECR log error events reported at this output. FECR logs only the frame alignment errors. CECR logs CRC4 code word errors.

To complement the on-chip error logging capabilities of the DS2181, the system designer can use off-chip logic gated by receive side outputs RCHCLK, RAF, RSTS and RCSYNC to demux error states present at RFER.

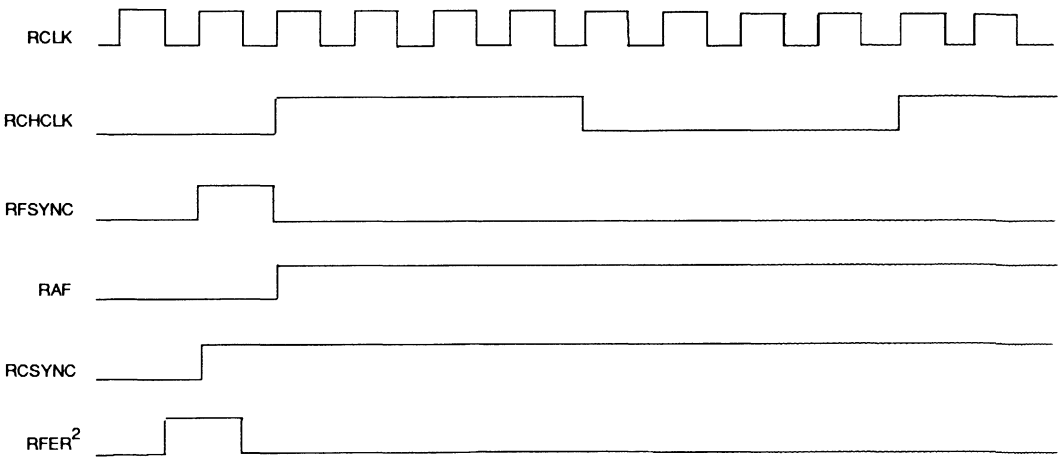
RFER OUTPUT TIMING FOR ALL ERROR CONDITIONS Figure 23



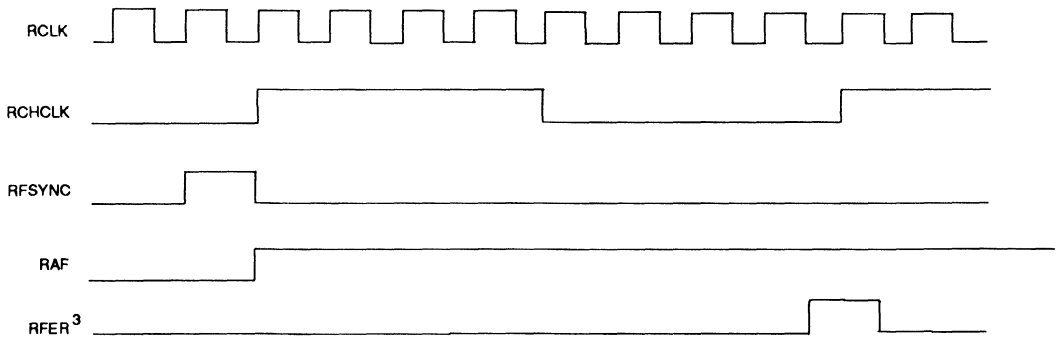
CAS MULTIFRAME ALIGNMENT ERROR Figure 24



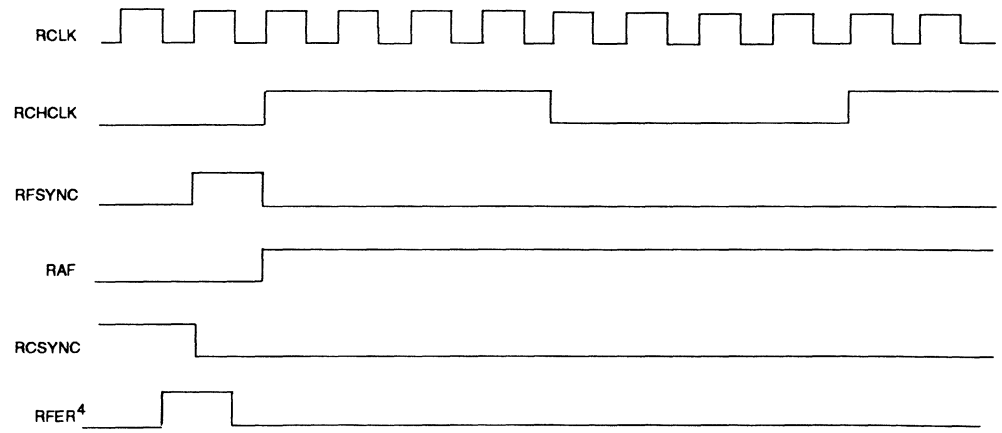
CRC4 SUB-MULTIFRAME 2 ERRORED Figure 25



FRAME ALIGNMENT WORD ERRORED Figure 26



CRC4 SUB-MULTIFRAME 1 ERRORED Figure 27



NOTES FOR FIGURES 23 THROUGH 27:

1. CAS multiframe alignment word received in error; RFER will transition high at first error occurrence and remain high as shown.
2. Previous CRC4 sub-multiframe 2 errored.
3. Frame alignment word errored.
4. Previous CRC4 sub-multiframe 1 errored.

RESET

A high-low transition on RST\ clears all internal registers except the three error counters; a resync is initiated until RST\ returns high. RST\ must be held low on system power-up and when switching to/from the hardware mode. Following reset, the host processor should update all on-chip registers to establish desired operating modes.

HARDWARE MODE

An on-chip hardware control mode simplifies preliminary system prototyping and serves applications which do not require the features of the serial port. Tying SPS low disables the serial port, clears all internal register locations except those shown below, and redefines pins 14 through 18 as mode control inputs. The mode control inputs establish device operational characteristics as shown in Table 8. The hardware mode simplifies device retrofit into existing applications where control interfaces are designed with discrete logic.

HARDWARE MODE CONTROL Table 8

PIN NUMBER	REGISTER LOCATION	NAME AND DESCRIPTION
14	**TINR.5**	**TRA - Transmit Remote Alarm** 0 = Normal operation 1 = Enable alarm
15	**TXR.2**	**TDMA - Transmit Distant Multiframe Alarm** 0 = Normal operation 1 = Enable alarm
16	**CCR.5/ CCR.4**	**Data Format** 0 = Input and output data AMI coded 1 = Input and output data HDB3 coded
17	**CCR.3/ CCR.2**	**Transmit and Receive CRC4 Multiframe** 0 = Disabled 1 = Enabled
18	**TCR.5 RCR.5**	**Transmit and Receive CAS Multiframe** 0 = Enabled 1 = Disabled

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to ground	-1.0V to +7V
Operating temperature	-0° to 70° C
Storage temperature	-55° to +125° C
Soldering temperature	-260° C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0° to 70° C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}	2.0		V_{DD}+.3	V
Logic 0	V_{IL}	-0.3		+0.8	V
Supply	V_{DD}	4.5		5.5	V

DC ELECTRICAL CHARACTERISTICS (0° to 70° C V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		6		mA	1,2
Input Leakage	I_{IL}	-1.0		+1.0	uA	3
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	+4.0			mA	5
Output Leakage	I_{LO}	-1.0		+1.0	uA	6

NOTES:

1. TCLK = RCLK = 2.048 MHz.
2. Outputs open.
3. $0V < V_{IN} < V_{DD}$.
4. All outputs except INT\ which is open collector.
5. All outputs.
6. Applies to SDO when tri-stated.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	7	pF

AC ELECTRICAL CHARACTERISTICS[1,2] SERIAL PORT

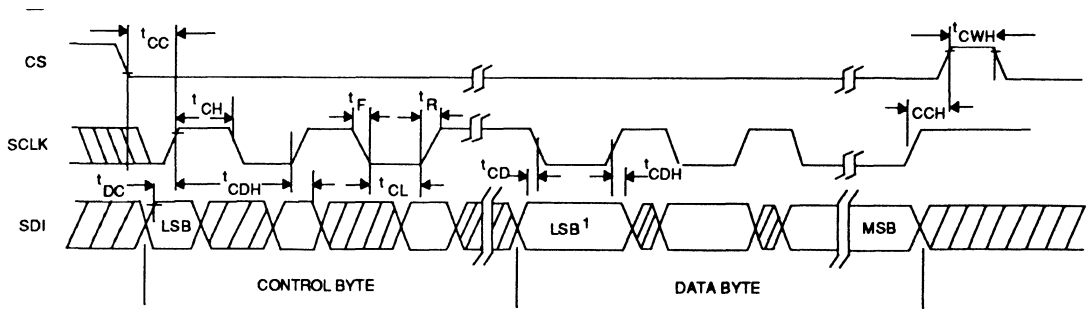
(0° to 70° C, V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SDI to SCLK Setup	t_{DC}	50			ns
SCLK to SDI Hold	t_{CDH}	50			ns
SDI to SCLK Falling Edge	t_{CD}	50			ns
SCLK Low Time	t_{CL}	244			ns
SCLK High Time	t_{CH}	244			ns
SCLK Rise and Fall Times	t_R,t_F			100	ns
CS to SCLK Setup	t_{CC}	50			ns
SCLK to CS Hold	t_{CCH}	50			ns
CS Inactive Time	t_{CWH}	2.5			us
SCLK to SDO Valid	t_{CDV}			200	ns
CS to SDO High Z	t_{CDZ}			75	ns

NOTES:

1. Measured at V_{IH} = 2.0 or V_{IL} = .8 and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pf.

SERIAL PORT WRITE AC TIMING DIAGRAM Figure 28



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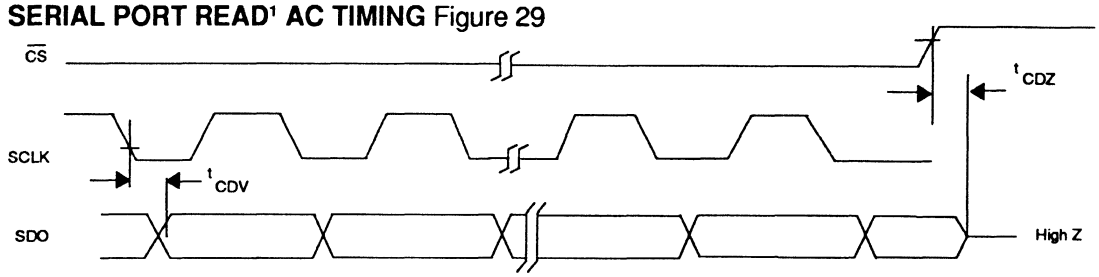
NOTES:

1. Data byte bits must be valid across low clock periods to prevent transients in operating modes.
2. Shaded regions indicate "don't care" states of input data.

SERIAL PORT READ[1] AC TIMING Figure 29



NOTE:

1. Serial port write must precede a port read to provide address information.

AC ELECTRICAL CHARACTERISTICS[1,2] TRANSMIT

(0^0 to 70^0 C, V_{DD} = 5V±5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK Period	t_P		488		ns
TCLK Pulse Width	t_{WL},t_{WH}		244		ns
TCLK Rise and Fall Times	t_R,t_F		20		ns
TSER, TSD, TIND and TXD Setup to TCLK Falling	t_{STD}	50			ns
TSER, TSD, TIND and TXD Hold to TCLK Falling	t_{HTD}	50			ns
TFSYNC, TMSYNC Setup to TCLK Falling	t_{STS}	75			ns
TFSYNC, TMSYNC Hold to TCLK Falling	t_{HTS}	50			ns
Propagation Delay TCLK to TCHCLK, TSTS, TMO, TAF	t_{PTS}			75	ns

NOTES:

1. Measured at V_{IH} = 2.0 or V_{IL} = .8 and 10 ns maximum rise and fall time.
2. Output load capacitance = 100 pf.

AC ELECTRICAL CHARACTERISTICS[1,2] RECEIVE

(0^0 to 70^0 C, V_{DD} = 5V ± 5%)

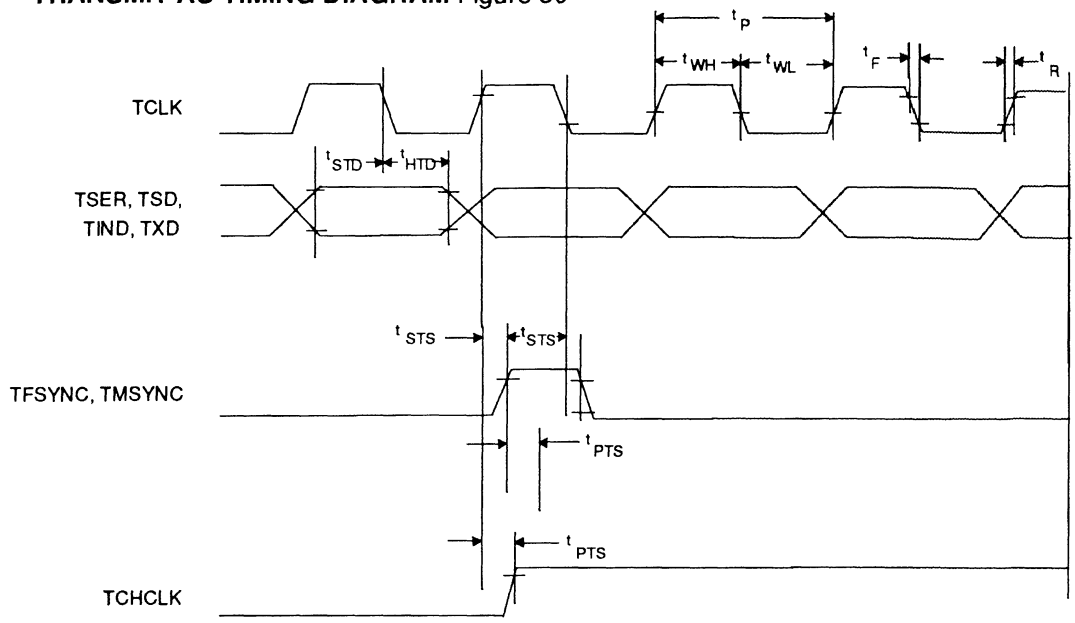
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Propagation Delay RCLK to RMSYNC, RFSYNC, RSTS, RCHCLK, RAF	t_{PRS}			75	ns
Propagation Delay RCLK to RSER, RSD	t_{PRD}			75	ns
Transition Time All Outputs	t_{TTR}			20	ns
RCLK Period	t_P		488		ns
RCLK Pulse Width	t_{WL},t_{WH}		244		ns
RCLK Rise and Fall Times	t_R,t_F		20		ns
RPOS, RNEG Setup to RCLK Falling	t_{SRD}	50			ns
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50			ns
Propagation Delay RCLK to RLOS, RRA, RBV, RFER,RDMA, RCL	t_{PRA}			75	ns
Minimum RST Pulse Width	t_{RST}	1			us

5

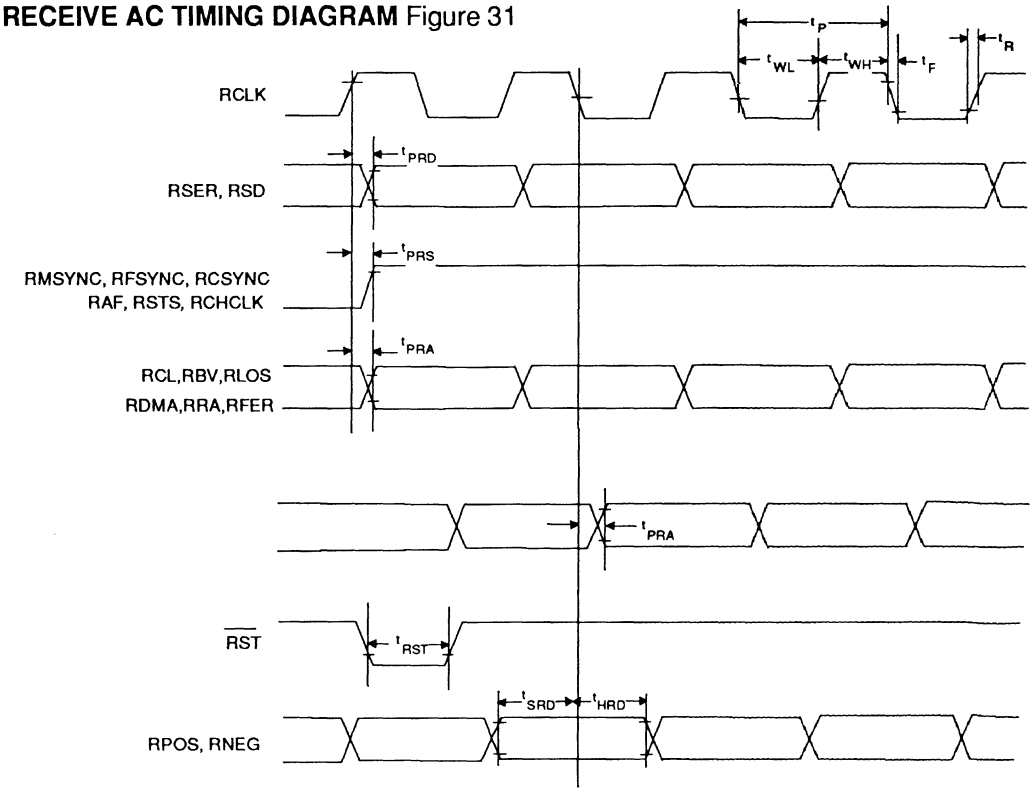
NOTES:

1. Measured at V_{IH} = 2.0 or V_{IL} = .8 and 10 ns. maximum rise and fall time.
2. Output load capacitance = 100 pf.

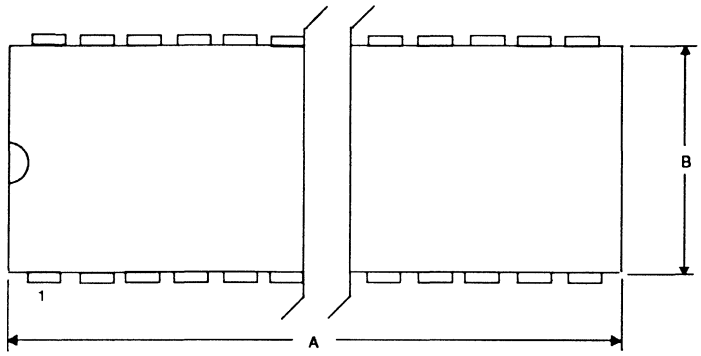
TRANSMIT AC TIMING DIAGRAM Figure 30



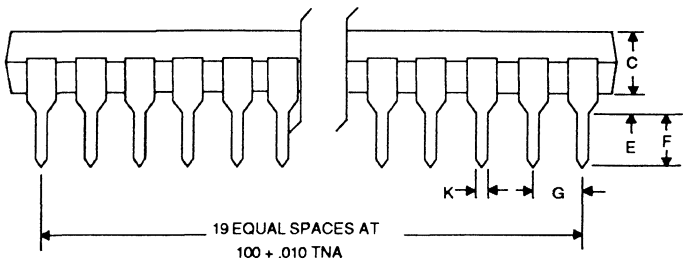
RECEIVE AC TIMING DIAGRAM Figure 31

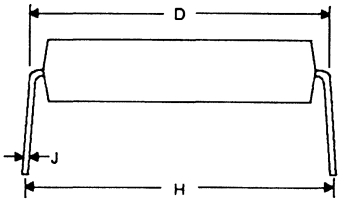


DS2181
CEPT Transceiver

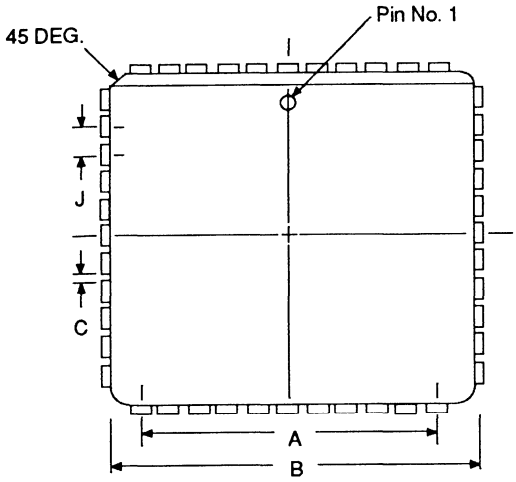


DIM.	INCHES	
	MIN.	MAX.
A	2.040	2.080
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

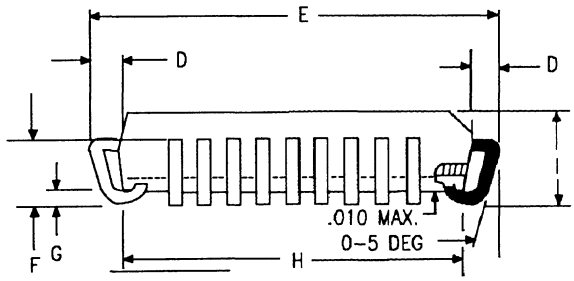


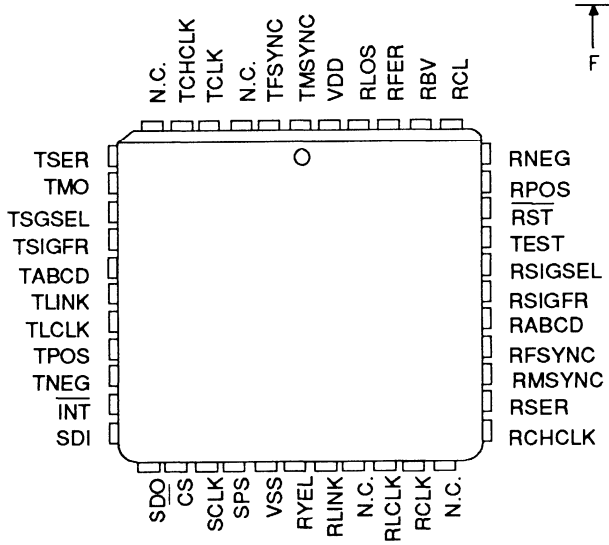


DS2181Q



DIM.	INCHES	
	MIN.	MAX.
A	.490	.510
B	.590	.630
C	.020	.024
D	.018	.022
E	.688	.692
F	.118	.122
G	.020	.030
H	.590	.630
I	.167	.173
J	.048	.051





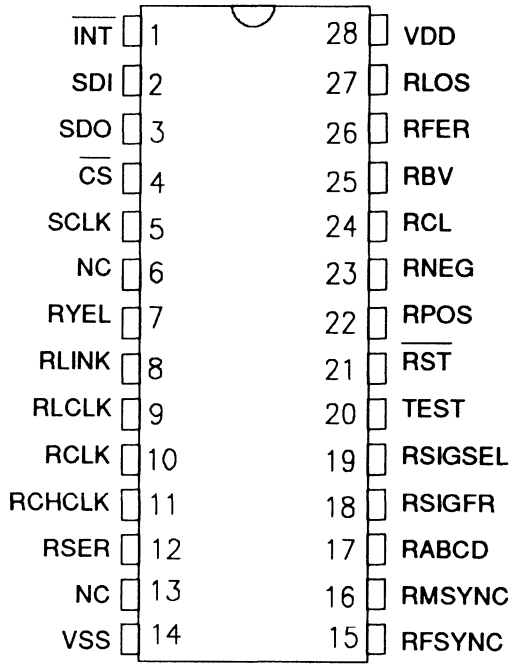
DALLAS SEMICONDUCTOR

DS2182
T1 LINE MONITOR

FEATURES

- Performs framing and monitoring functions
- Supports Superframe and Extended Superframe formats
- Designed to fulfill the requirements outlined in TA-TSY-000147 (DS1 Rate Digital Service Monitoring Unit) and TR-TSY-000194 (ESF Interface Specification)
- Four onboard error counters
  - 16-bit bipolar violation
  - 8-bit CRC
  - 8-bit OOF
  - 8-bit frame bit error
- Indication of the following
  - yellow and blue alarms
  - incoming B8ZS code words
  - 8 and 16 zero strings
  - change of frame alignment
  - loss of sync
  - carrier loss
- Simple serial interface used for configuration, control and status monitoring
- Burst mode allows quick access to counters for status updates
- Automatic counter reset feature
- Single 5V supply; low-power CMOS technology
- Available in 28-pin DIP and 28-pin PLCC

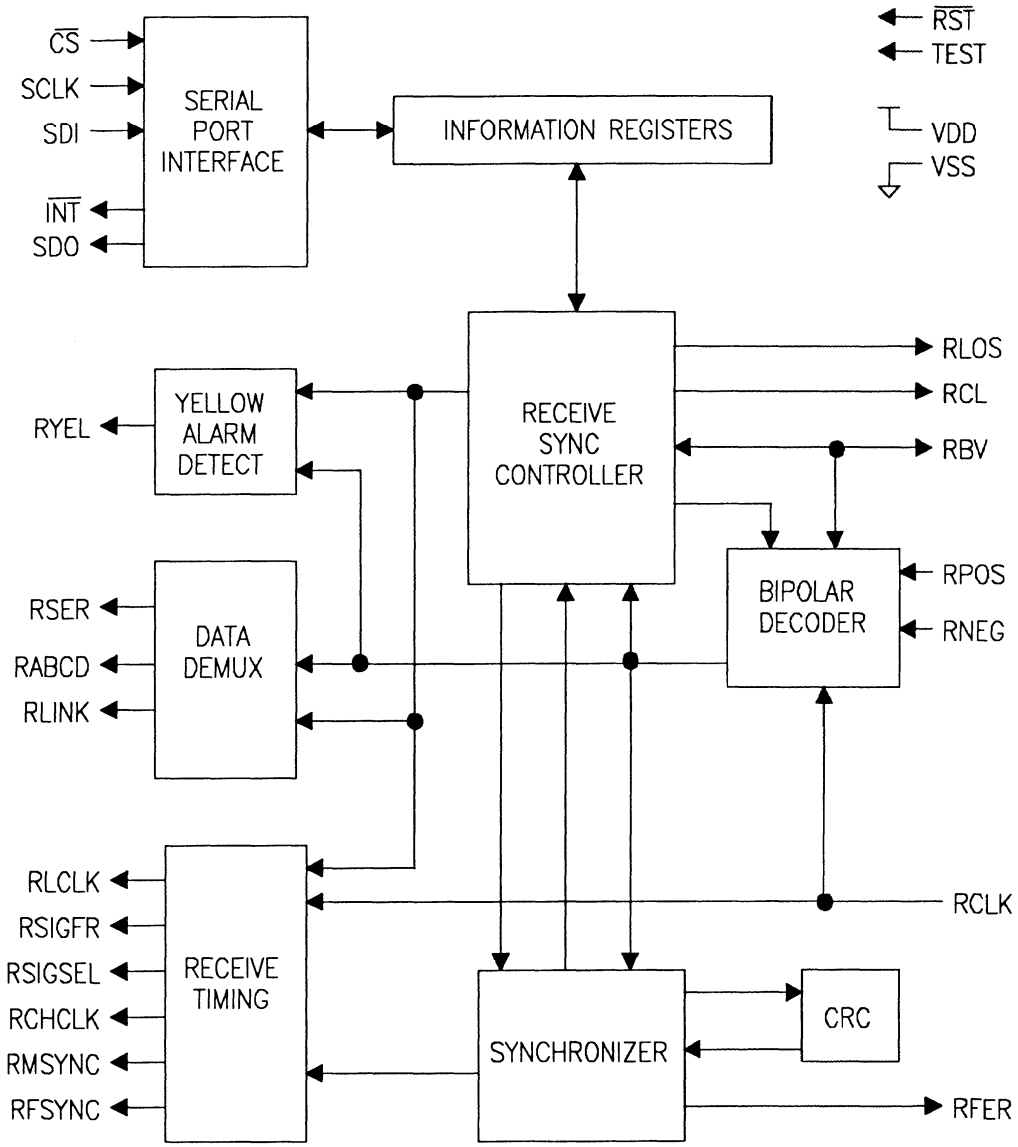
PIN DESCRIPTION



DESCRIPTION

The DS2182 is a monolithic CMOS device designed to monitor real-time performance on T1 lines. The DS2182 frames to the data on the line, counts errors, and supplies detailed information about the status and condition of the line. Large onboard counters allow the accumulation of errors for extended periods, which permits a single CPU to monitor a number of T1 lines. Output clocks that are synchronized to the incoming data stream are provided for easy extraction of S-Bits, FDL bits, signaling bits and channel data.

DS2182 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
6	NC	-	**No Connect.** No internal connection. This pin can be tied to either VSS or VDD, or it can be floated.
7	RYEL	O	**Receive Yellow Alarm.** Transitions high when yellow alarm detected; goes low when alarm clears.
8	RLINK	O	**Receive Link Data.** Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
9	RLCLK	O	**Receive Link Clock.** 4 KHz demand clock for RLINK.
10	RCLK	I	**Receive Clock.** 1.544 MHz primary clock.
11	RCHCLK	O	**Receive Channel Clock.** 192 KHz clock; identifies time slot (channel) boundaries.
12	RSER	O	**Receive Serial Data.** Received NRZ serial data; updated on rising edges of RCLK.
13	NC	-	**No Connect.** No internal connection. This pin can be tied to either VSS or VDD, or it can be floated.
15	RFSYNC	O	**Receive Frame Sync.** Extracted 8 KHz clock, one RCLK wide; F-bit position in each frame.
16	RMSYNC	O	**Receive Multiframe Sync.** Extracted multiframe sync; positive-going edge indicates start of multiframe; 50% duty cycle.
17	RABCD	O	**Receive ABCD Signaling.** Extracted signaling data output; valid for each channel in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
18	RSIGFR	O	**Receive Signaling Frame.** High during signaling frames; low during non-signaling frames (and during resync).

19	RSIGSEL	O	**Receive Signaling Select**. In 193E framing, a .667 KHz clock that identifies signaling frames A and C; a 1.33 KHz clock in 193S.
21	RST\	I	**Reset**. A high-low transition clears all internal registers and resets counters. A high-low-high transition initiates a resync.
22 23	RPOS RNEG	I	**Receive Bipolar Data Inputs**. Sampled on falling of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.
24	RCL	O	**Receive Carrier Loss**. High if 192 consecutive zeros appear at RPOS and RNEG; goes low after next one's appearance.
25	RBV	O	**Receive Bipolar Violation**. High during accused bit time at RSER if bipolar violation detected, low otherwise.
26	RFER	O	**Receive Frame Error**. High during F-bit time when FT or FS errors occur (193S), or when FPS or CRC errors occur (193E). Low during resync.
27	RLOS	O	**Receive Loss of Sync**. Indicates sync status; high when internal resync is in progress, low otherwise.

PORT PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
1	INT\	O	**Receive Alarm Interrupt**. Flags host controller during alarm conditions. Active low; open drain output.
2	SDI	I	**Serial Data In**. Data for onboard registers. Sampled on rising edge of SCLK.
3	SDO	O	**Serial Data Out**. Control and status information from onboard registers. Updated on falling edge of SCLK; tri-stated during serial port write or when CS\ is high.
4	CS\	I	**Chip Select**. Must be low to read or write the serial port.
5	SCLK	I	**Serial Data Clock**. Used to read or write the serial port registers.

POWER AND TEST PIN DESCRIPTION Table 3

PIN	SYMBOL	TYPE	DESCRIPTION
14	VSS	-	**Signal Ground.** 0.0 volts.
20	TEST	I	**Test Mode.** Tie to VSS for normal operation.
28	VDD	-	**Positive Supply.** 5.0 volts.

REGISTER SUMMARY Table 4

REGISTER	ADDRESS	DESCRIPTION/FUNCTION
BVCR2	0000	**Bipolar Violation Count Register 2.** LSW of a 16-bit presettable counter that records individual bipolar violations.
BVCR1	0001	**Bipolar Violation Count Register 1.** MSW of a 16-bit presettable counter that records individual bipolar violations.
CRCCR	0010	**CRC Error Count Register.** 8-bit presettable counter that records CRC6 errored words in the 193E frame mode.
OOFCR	0011	**OOF Count Register.** 8-bit presettable counter that records OOF events. OOF events are defined by RCR1.5 and RCR1.6.
FECR	0100	**Frame Error Count Register.** 8-bit presettable counter that records individual bit errors in the framing pattern.
RSR1	0101	**Receive Status Register 1.** Reports alarm conditions.
RIMR1	0110	**Receive Interrupt Mask Register 1.** Allows masking of individual alarm-generated interrupts from RSR1.
RSR2	0111	**Receive Status Register 2.** Reports alarm conditions.
RIMR2	1000	**Receive Interrupt Mask Register 2.** Allows masking of individual alarm-generated interrupts from RSR2.
RCR1	1001	**Receive Control Register 1.** Programs device operating characteristics.
RCR2	1010	**Receive Control Register 2.** Programs device operating characteristics.

SERIAL PORT INTERFACE

The port pins of the DS2182 serve as a microprocessor/microcontroller-compatible serial port. Eleven onboard registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. The port on the DS2182 can be read or written to at any time. Serial port reads and writes are independent of T1 line timing signals RCLK, RPOS, and RNEG. However, RCLK is needed in order to clear RSR1 and RSR2 after reads.

ADDRESS/COMMAND

Reading or writing the control, configuration or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. The following four bits identify the register address. The next two bits are reserved and must be set to zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively read or written to. Data is read and written to the DS2182 LSB first.

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the CS\ input low. Input data is latched on the rising edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the CS\ input transitions high. Port control logic is disabled and SDO is tri-stated when CS\ is high.

DATA I/O

Following the eight SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edge of the next eight SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edges of the next 8 SCLK cycles. The SDO pin is tri-stated during device write and can be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE

The burst mode allows all onboard registers to be consecutively written to or read by the host processor. A burst read is used to poll all registers; RSR1 and RSR2 contents will be unaffected. This feature minimizes device initialization time on system power-up or reset. Burst mode is initiated when ACB.7 is set and the address is 0000. A burst is terminated by a low-high transition on CS\.

ACB: ADDRESS COMMAND BYTE Figure 2

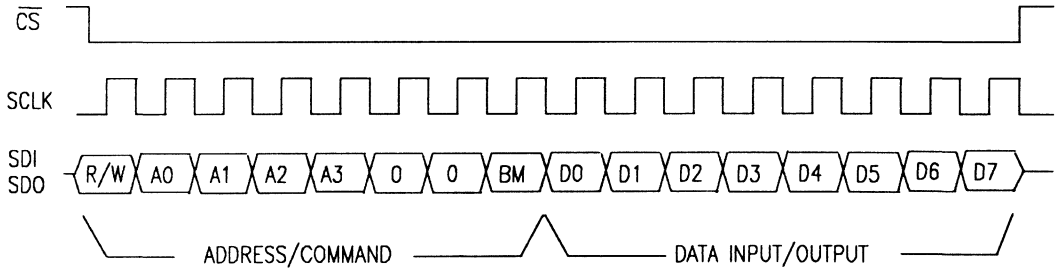
(MSB) (LSB)

BM	-	-	ADD3	ADD2	ADD1	ADD0	R/W

SYMBOL	POSITION	NAME AND DESCRIPTION
BM	ACB.7	**Burst Mode.** If set (and register address is 0000) burst read or write is enabled.
-	ACB.6	Reserved, must be 0 for proper operation.
-	ACB.5	Reserved, must be 0 for proper operation.
ADD3	ACB.4	MSB of register address.
ADD0	ACB.1	LSB of register address.
R/W	ACB.0	**Read/Write Select.** 0 = write addressed register 1 = read addressed register

5

SERIAL PORT READ/WRITE Figure 3



NOTES:

1. SDI is sampled on rising edge of SCLK.
2. SDO is updated on falling edge of SCLK.

OPERATION OF THE COUNTERS

All four of the counters in the DS2182 can be preset by the user to establish an event count interrupt threshold. The counters count up from the preset value until they reach saturation. At saturation, each additional event occurrence sets the appropriate bit in RSR2 and generates an interrupt if enabled by RIMR2.

The DS2182 contains an auto counter reset feature in the burst read mode. If RCR1.4 is set, then the user can burst read the four counters (five registers), and all four counters will be automatically reset to zero after the read takes place. Since the burst mode can be terminated at any time by taking CS\ high, the user has the option of reading all of the registers or only the counters. If RCR1.4 is set, then any read of the registers, burst mode or not, will clear the count in all four counters. If the user wishes to read the port and not clear the counters, then RCR1.4 must be cleared first.

The counter registers can be read or written to at any time with the serial port, which operates totally asynchronously with the monitoring of the T1 line. Reading a register will not affect the count as long as RCR1.4 is cleared. The dual buffer architecture of the DS2182 insures that no error events will be missed while the serial port is being accessed for reads.

BVCR1: BIPOLAR VIOLATION COUNT REGISTER 1; BVCR2: BIPOLAR VIOLATION COUNT REGISTER 2 Figure 4

(MSB)							(LSB)
BV7	**BV6**	**BV5**	**BV4**	**BV3**	**BV2**	**BV1**	**BV0**

SYMBOL	POSITION	NAME AND DESCRIPTION
BV7	**BVCR.7**	MSB of bipolar violation count
BV0	**BVCR.0**	LSB of bipolar violation count

Bipolar Violation Count Register 1 (BVCR1) is the most significant word and BVCR2 is the least significant word of a presettable 16-bit counter that records individual bipolar violations. If the B8ZS mode is enabled (RCR2.2 = 1), then B8ZS code words are not counted. This counter increments at all times and is not disabled by a loss of sync condition (RLOS = 1). The counter saturates at 65,535 and generates an interrupt for each occurrence after saturation if RIMR2.0 is set.

NOTE:
In order to properly preset the Bipolar Violation Count Register, BVCR2 must be written to before BVCR1 is written to.

CRCCR: CRC COUNT REGISTER Figure 5

(MSB)							(LSB)
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC7	CRCCR.7	MSB of CRC6 word error count
CRC0	CRCCR.0	LSB of CRC6 word error count

The CRC Count Register (CRCCR) is an 8-bit presettable counter that records word errors in the Cyclic Redundancy Check (CRC). This 8-bit binary counter saturates at 255 and generates an interrupt for each occurrence after saturation if RIMR2.1 is set. The count in this register is only valid in the 193E framing mode (RCR2.4 = 1) and is reset and disabled in the 193S framing mode (RCR2.4 = 0). The count is disabled during a loss of sync condition (RLOS = 1).

5

OOFCR: OOF COUNT REGISTER Figure 6

(MSB)							(LSB)
OOF7	OOF6	OOF5	OOF4	OOF3	OOF2	OOF1	OOF0

SYMBOL	POSITION	NAME AND DESCRIPTION
OOF7	OOFCR.7	MSB of OOF event count
OOF0	OOFCR.0	LSB of OOF event count

The OOF Count Register (OOFCR) is an 8-bit presettable counter that records Out Of Frame (OOF) events. OOF events are defined by RCR1.5 and RCR1.6. This 8-bit counter saturates at 255 and generates an interrupt for each occurrence after saturation if RIMR2.2 is set. The count is disabled during a loss of sync condition (RLOS = 1).

FECR: FRAME ERROR COUNT REGISTER Figure 7

(MSB) (LSB)

FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0

SYMBOL	POSITION	NAME AND DESCRIPTION
FE7	FECR.7	MSB of frame error count
FE0	FECR.0	LSB of frame error count

The Frame Error Count Register (FECR) is an 8-bit presettable counter that records individual frame bit errors. In the 193E mode (RCR2.4 = 1), the FECR records bit errors in the FPS framing pattern (001011). In the 193S mode (RCR2.4 = 0), the FECR records bit errors in both the FT (101010) and FS (001110) framing patterns if RCR1.3 is set. If RCR1.3 is cleared, then the FECR only records bit errors in the FT pattern. This 8-bit counter saturates at 255 and generates an interrupt for each occurrence after saturation if RIMR2.3 is set. The count is disabled during a loss of sync condition (RLOS = 1).

RSR1: RECEIVE STATUS REGISTER 1 Figure 8

(MSB) (LSB)

8ZD	16ZD	RCL	RYEL	RLOS	B8ZSD	RBL	COFA

SYMBOL	POSITION	NAME AND DESCRIPTION
8ZD	RSR1.7	**8 Zero Detect.** Set when a string of eight consecutive zeros has been received at RPOS and RNEG.
16ZD	RSR1.6	**16 Zero Detect.** Set when a string of 16 consecutive zeros has been received at RPOS and RNEG.
RCL	RSR1.5	**Receive Carrier Loss.** Set when a string of 192 consecutive zeros has been received at RPOS and RNEG.
RYEL	RSR1.4	**Receive Yellow Alarm.** Set when yellow alarm is detected. The format of yellow alarm is determined by RCR2.3 and RCR2.4.
RLOS	RSR1.3	**Receive Loss of Sync.** Set when resync is in progress.

B8ZSD	**RSR1.2**	**B8ZS Code Word Detect**. Set when a B8ZS code word is received at RPOS and RNEG independent of whether the B8ZS mode is enabled or not (RCR2.2).
RBL	**RSR1.1**	**Receive Blue Alarm**. Set when two consecutive frames with less than three zeros total in the data stream have been received at RPOS and RNEG (F-bits are not tested). This alarm is considered cleared when three or more zeros in two frames have been received.
COFA	**RSR1.0**	**Change of Frame Alignment**. Set when the last resync resulted in a change of frame or multiframe alignment.

NOTE:
Alarms 8ZD, 16ZD, and RCL are cleared on the next occurrence of a one at RPOS and RNEG.

RECEIVE STATUS REGISTERS

The receive status registers (RSR1 and RSR2) can be used in either a polled or an interrupt configuration. In a polled configuration, the user reads the RSR at regular intervals to check for alarms. In an interrupt configuration, the user monitors the INT\ pin. When the INT\ pin goes low, an alarm condition has occurred and has been reported in one of the RSRs. The processor can then read the RSRs to find which bits have been set. All of the bits in the RSRs operate in a latched fashion. That is, once set, they remain set until read. The bits in the RSR are cleared when read unless the read was performed in the burst mode or the alarm condition still exists.

YELLOW ALARM

193S BIT 2. If RCR2.4 = 0 and RCR2.3 = 0, then the DS2182 examines bit 2 of all incoming channels for the presence of a yellow alarm. If bit 2 is set to zero in 256 consecutive channels, then the reception of a yellow alarm is declared. The alarm is considered cleared when the first channel with bit 2 set to a one is received.

193S S-BIT. If RCR2.4 = 0 and RCR2.3 = 1, then the DS2182 examines the S-bit position of frame 12 for the presence of a yellow alarm. The DS2182 declares the presence of a yellow alarm on the first occurrence of the S-bit in frame 12 being set to one. The alarm is considered cleared when this S-bit returns to zero.

193E FDL. If RCR2.4 = 1, then the DS2182 examines the FDL for a repeating 00FF pattern. If this pattern is received in the FDL 16 consecutive times without error, then a yellow alarm is declared. The alarm is considered cleared as soon as any pattern other than 00FF is received.

RIMR1: RECEIVE INTERRUPT MASK REGISTER 1 Figure 9

(MSB) (LSB)

8ZD	16ZD	RCL	RYEL	RLOS	B8ZSD	RBL	COFA

SYMBOL	POSITION	NAME AND DESCRIPTION
8ZD	RIMR1.7	**8 Zero Detect Mask.** 1 = interrupt enabled 0 = interrupt masked
16ZD	RIMR1.6	**16 Zero Detect Mask.** 1 = interrupt enabled 0 = interrupt masked
RCL	RIMR1.5	**Receive Carrier Loss Mask.** 1 = interrupt enabled 0 = interrupt masked
RYEL	RIMR1.4	**Receive Yellow Alarm Mask.** 1 = interrupt enabled 0 = interrupt masked
RLOS	RIMR1.3	**Receive Loss Of Sync Mask.** 1 = interrupt enabled 0 = interrupt masked
B8ZSD	RIMR1.2	**B8ZS Code Word Detect Mask.** 1 = interrupt enabled 0 = interrupt masked
RBL	RIMR1.1	**Receive Blue Alarm Mask.** 1 = interrupt enabled 0 = interrupt masked
COFA	RIMR1.0	**Change Of Frame Alignment Mask.** 1 = interrupt enabled 0 = interrupt masked

RSR2: RECEIVE STATUS REGISTER 2 Figure 10

(MSB)							(LSB)
-	-	-	FERR	FECS	OOFCS	CRCCS	BPVCS

SYMBOL	POSITION	NAME AND DESCRIPTION
-	RSR2.7	Not defined; could be any value when read.
-	RSR2.6	Not defined; could be any value when read.
-	RSR2.5	Not defined; could be any value when read.
FERR	RSR2.4	**Frame Bit Error.** Set when FT (193S) or FPS (193E) bit errors occur.
FECS	RSR2.3	**Frame Error Count Saturation.** Set on the next frame error event after the 8-bit Frame Error Count Register (FECR) saturates at 255.
OOFCS	RSR2.2	**Out Of Frame Count Saturation.** Set on the next OOF event after the 8-bit OOF Count Register (OOFCR) saturates at 255.
CRCCS	RSR2.1	**CRC Count Saturation.** Set on the next CRC error event after the 8-bit CRC Count Register (CRCCR) saturates at 255.
BPVCS	RSR2.0	**Bipolar Violation Count Saturation.** Set on the next BPV error event after the 16-bit Bipolar Violation Count Register (BVCR) saturates at 65,535.

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RIMR2: RECEIVE INTERRUPT MASK REGISTER 2 Figure 11

(MSB)							(LSB)
-	-	-	FERR	FECS	OOFCS	CRCCS	BPVCS

SYMBOL	POSITION	NAME AND DESCRIPTION
-	RIMR2.7	Reserved; set to 0 for proper operation.
-	RIMR2.6	Reserved; set to 0 for proper operation.
-	RIMR2.5	Reserved; set to 0 for proper operation.

FERR	**RIMR2.4**	**Frame Bit Error Mask.** 1 = interrupt enabled 0 = interrupt masked
FECS	**RIMR2.3**	**Frame Error Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
OOFCS	**RIMR2.2**	**Out Of Frame Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
CRCCS	**RIMR2.1**	**CRC Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked
BPVCS	**RIMR2.0**	**Bipolar Violation Count Saturation Mask.** 1 = interrupt enabled 0 = interrupt masked

RCR1: RECEIVE CONTROL REGISTER 1 Figure 12

(MSB) (LSB)

ARC	**OOF1**	**OOF2**	**ACR**	**SYNCC**	**SYNCT**	**SYNCE**	**RESYNC**

SYMBOL	POSITION	NAME AND DESCRIPTION
ARC	**RCR1.7**	**Auto Resync Criteria.** 1 = resync on OOF event only 0 = resync on OOF event or Receive Carrier Loss (RCL)
OOF1	**RCR1.6**	**Out Of Frame 1.** OOF event description. Valid when RCR1.5 is cleared 1 = 2 out of 5 frame bits (FT or FPS) in error 0 = 2 out of 4 frame bits (FT or FPS) in error
OOF2	**RCR1.5**	**Out Of Frame 2.** OOF event description. 1 = 2 out of 6 frame bits (FT or FPS) in error 0 = follow OOF event described in RCR1.6

ACR	**RCR1.4**	**Auto Counter Reset**. When set, all four of the counters will be reset to zero when read.
SYNCC	**RCR1.3**	**Sync Criteria**. Determines the type of algorithm utilized by the receive synchronizer; differs for each frame mode. **193S Framing (RCR2.4 = 0)** 0 = synchronize to frame boundaries using FT pattern, then search for multiframe by using FS. 1 = cross couple FT and FS patterns in sync algorithm. **193E Framing (RCR2.4 = 1)** 0 = normal sync (utilizes FPS only). 1 = validate new alignment with CRC before declaring sync.
SYNCT	**RCR1.2**	**Sync Time**. 1 = validate 24 consecutive F-bits before declaring sync. 0 = validate 10 consecutive F-bits before declaring sync.
SYNCE	**RCR1.1**	**Sync Enable**. If clear, the DS2182 automatically begins a resync if the conditions described in RCR1.7 are met. If set, no auto resync occurs.
RESYNC	**RCR1.0**	**Resync**. When toggled low to high, the DS2182 initiates a resync immediately. The bit must be cleared and set again for subsequent resyncs.

SYNCHRONIZER

The heart of the monitor is the receive synchronizer. This circuit serves two purposes: 1) monitors the incoming data stream for loss of frame or multiframe alignment, and 2) searches for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off-line search for the new alignment; all output timing signals remain at the old alignment with the exception of RSIGFR, which is forced low during resync. When one and only one candidate is qualified, the output timing moves to the new alignment at the beginning of the next multiframe. One frame later, RLOS will transition low, indicating valid sync and the resumption of the normal sync monitoring mode. Several bits in the RCR1 allow tailoring of the resync algorithm by the user. These bits are described below.

SYNC CRITERIA (RCR1.3)

193E. Bit RCR1.3 determines which sync algorithm is utilized when resync is in progress (RLOS = 1). In 193E framing, when RCR1.3 = 0, the synchronizer will lock only to the FPS pattern and will move to the new frame and multiframe alignment after the framing candidate is qualified. RLOS will go low one frame after the move to the new alignment. When RCR1.3 = 1, the

new alignment is further tested by a CRC6 code match. RLOS will transition low after a CRC6 match occurs. If no CRC6 match occurs in three attempts (three multiframes), the algorithm resets and a new search for the FPS pattern begins. It takes 9 ms for the synchronizer to check the first CRC6 code after the new FPS alignment has been loaded. Each additional CRC6 test takes 3 ms. Regardless of the state of RCR1.3, if more than one candidate exists after 24 ms, the synchronizer begins eliminating emulators by testing their CRC6 codes in order to find the true framing candidate.

193S. In 193S framing, when RCR1.3 = 1, the synchronizer cross-checks the FT pattern with the FS pattern to help eliminate false framing candidates such as digital milliwatts. The FS patterns are compared to the repeating pattern ...00111000111000...(00111x0 if RCR2.3 = 1). In this mode, FT and FS must be correctly identified by the synchronizer before sync is declared. Clearing RCR1.3 causes the synchronizer to search for the FT pattern (101010...) without cross-coupling the FS pattern. Frame sync is established using the FT information, while multiframe sync is established only if valid FS information is present. If no valid FS pattern is identified, the synchronizer moves to the FT alignment, RLOS goes low, and a false multiframe position may be indicated by RMSYNC. RFER indicates when the received S-bit pattern does not match the assumed internal multiframe alignment. This mode will be used in applications where non-standard S-bit patterns exist. In such applications, multiframe alignment information can be decoded externally by using the S-bits present at RLINK.

SYNC TIME (RCR1.2)

Bit RCR1.2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR1.2 =1, the algorithm validates 24 bits; if RCR1.2 = 0, 10 bits are validated. Validating 24 bits results in superior false framing protection while 10-bit testing minimizes reframe time. In either case, the synchronizer only establishes resync when one and only one candidate is found (see Table 5).

AVERAGE REFRAME TIME Table 5

FRAME MODE	RCR1.2 = 0			RCR1.2 = 1		
	min.	avg.	max.	min.	avg.	max.
193S	3.0ms	3.75ms	4.5ms	6.5ms	7.25ms	8.0ms
193E	6.0ms	7.5ms	9.0ms	13.0ms	14.5ms	16.0ms

NOTE:

Average reframe time is defined here as the average time it takes from the start of resync (rising edge of RLOS) to the actual loading of the new alignment (on a multiframe edge) into the output receive timing.

SYNC ENABLE (RCR1.1)

When RCR1.1 is cleared, the receiver initiates automatic resync if an OOF event occurs or if carrier loss (192 consecutive zeros) occurs (depends on RCR1.7). When RCR1.1 is set, the automatic resync circuitry is disabled. In this case, resync can only be initiated by setting RCR1.0 to 1 or externally transitioning RST\ from low to high. Note that using RST\ to initiate a resync resets the output timing while RST\ is low; use of RCR1.1 will not affect the output timing until the new alignment is located.

RESYNC (RCR1.0)

A zero-to-one transition of RCR1.0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

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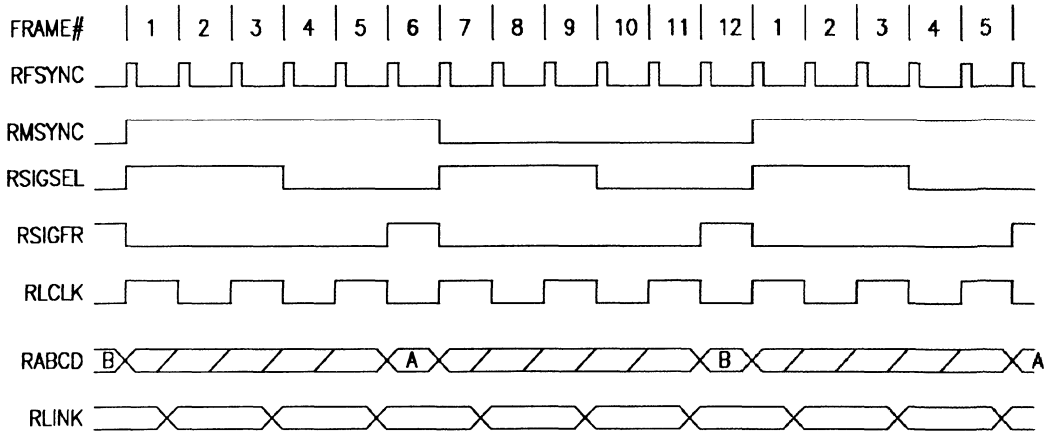
RCR2: RECEIVE CONTROL REGISTER 2 Figure 13

(MSB)							(LSB)
-	-	-	FM	SFYEL	B8ZS	-	-

SYMBOL	POSITION	NAME AND DESCRIPTION
-	RCR2.7	Reserved; must be 0 for proper operation.
-	RCR2.6	Reserved; must be 0 for proper operation.
-	RCR2.5	Reserved; must be 0 for proper operation.
FM	RCR2.4	**Frame Mode.** 1 = Extended Superframe (193E, 24 frames per Superframe). 0 = Superframe (193S or D4, 12 frames per Superframe).
SFYEL	RCR2.3	**SF Yellow Mode Select.** 1 = 1 in the S-bit position of frame 12. 0 = 0 in bit 2 of all channels.
B8ZS	RCR2.2	**Bipolar Eight Zero Substitution.** 1 = B8ZS enabled. 0 = B8ZS disabled.
-	RCR2.1	Reserved; must be 0 for proper operation.
-	RCR2.0	Reserved; must be 0 for proper operation.

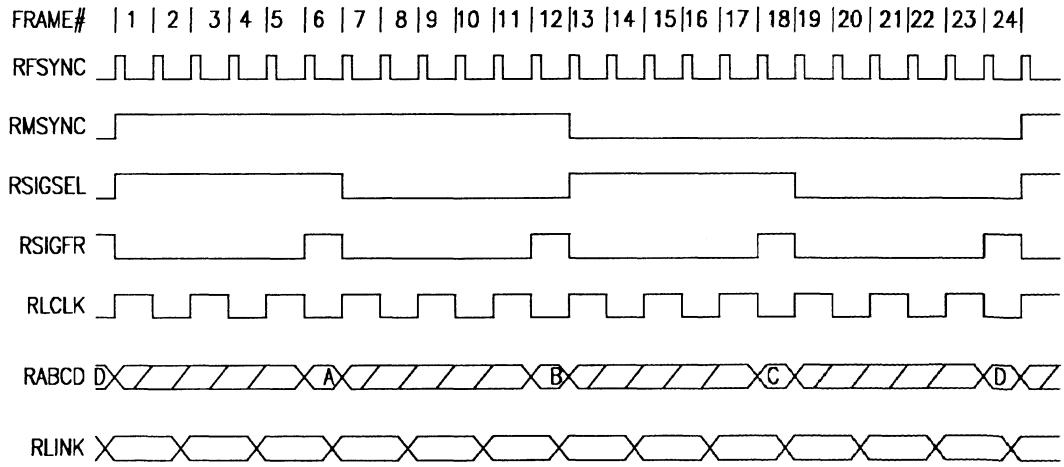
193S RECEIVE MULTIFRAME TIMING Figure 14



NOTES:

1. Signaling data is updated during signaling frames on channel boundaries. Pin RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit-time prior to S-bit frames and held for two frames.

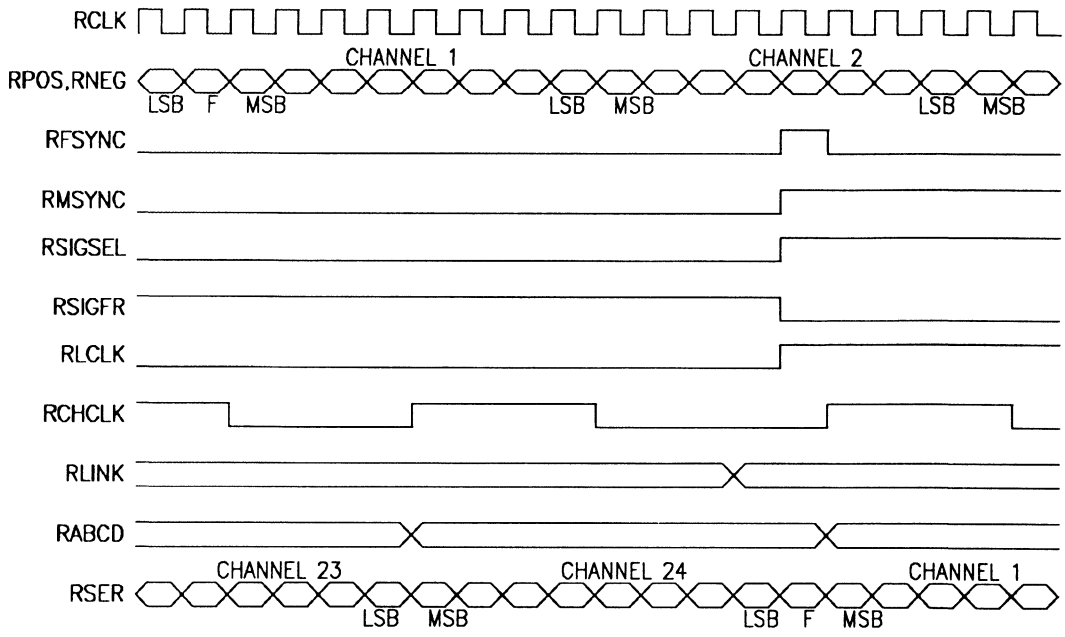
193E RECEIVE MULTIFRAME TIMING Figure 15



NOTES:

1. Signaling data is updated during signaling frames on channel boundaries. Pin RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL data) is updated one bit-time prior to odd frames and held for two frames.

RECEIVE MULTIFRAME BOUNDARY TIMING Figure 16



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NOTES:

1. RLINK timing is shown for 193E; in 193S, RLINK is updated on even frame boundaries and is held across multiframe edges.
2. Total delay from RPOS and RNEG to RSER output is 13 RCLK periods.

ALARM OUTPUTS

The transceiver also provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the onboard alarm logic.

RLOS OUTPUT

The receive loss of sync output indicates the status of the receiver synchronizer circuitry; when high, an off-line resynchronization is in progress and a high-low transition indicates that resync is complete. The RLOS bit (RSR1.3) is a latched version of the RLOS output. If the auto-resync mode is selected (RCR1.1 = 0), RLOS is a real-time indication of a carrier loss or OOF event occurrence.

RYEL OUTPUT

The yellow alarm output transitions high when a yellow alarm is detected. A high-low transition indicates the alarm condition has been cleared. The RYEL bit (RSR1.4) is a latched version of the RYEL output.

RBV OUTPUT

The bipolar violation output transitions high when the accused bit emerges at RSER. RBV goes low at the next bit time if no additional violations are detected.

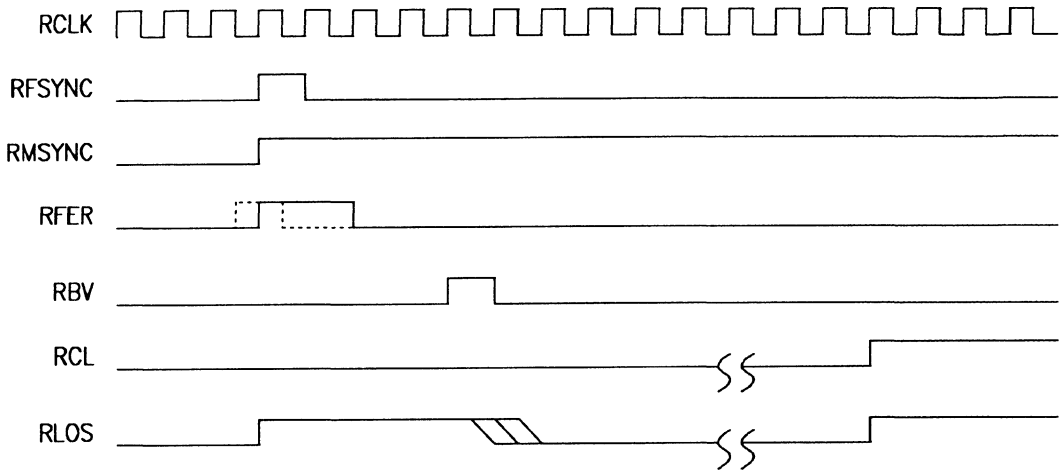
RFER OUTPUT

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S, framing FT and FS patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports CRC6 code word errors by a low-high-low transition (one bit period-wide) one-half RCLK period before a low-high transition on RMSYNC (see Figure 17).

RESET

A high-low transition on RST clears all registers and forces an immediate resync when RST returns high. RST must be held low on system power-up to insure proper initialization of the counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

ALARM OUTPUT TIMING Figure 17



NOTES:

1. RFER transitions high during F-bit time if received framing pattern bit is in error. (Frame 12 F-bits in 193S are ignored if RCR2.3 = 1.) Also, in 193E, RFER transitions high 1/2 bit-time before rising edge of RMSYNC to indicate a CRC6 error for the previous multiframe.
2. RBV indicates received bipolar violation and transitions high when accused bit emerges from RSER. If B8ZS is enabled, RBV will not report the zero replacement code.
3. RCL transitions high when 192 consecutive bits are zero; RCL transitions low when the next one is received.
4. RLOS transitions high during F-bit time that caused an OOF event if auto-resync is enabled (RCR1.1 = 0). Resync also occurs when loss of carrier is detected (RCL = 1) if RCR1.7 = 0. When RCR1.1 = 1, RLOS remains low until resync occurs, regardless of OOF or carrier loss flags. In this situation, resync is initiated only when RCR1.0 transitions low-to-high or the RST\ pin transitions high-low-high.

ABSOLUTE MAXIMUM RATINGS*

VOLTAGE ON ANY PIN RELATIVE TO GROUND	-	-1.0V to +7.0V
OPERATING TEMPERATURE	-	0^0 to 70^0 C
STORAGE TEMPERATURE	-	-55^0 to $+125^0$ C
SOLDERING TEMPERATURE	-	260^0 C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0^0 C to 70^0C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}	2.0		V_{DD}+.3	V
Logic 0	V_{IL}	-0.3		+0.8	V
Supply	V_{DD}	4.5		5.5	V

DC ELECTRICAL CHARACTERISTICS

(0^0 C to 70^0C, V_{DD}=5V $\pm$ 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		3		mA	1,2
Input Leakage	I_{IL}	-1.0		+1.0	uA	3
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	+4.0			mA	5
Output Leakage	I_{LO}	-1.0		+1.0	uA	6

NOTES:

1. RCLK = 1.544 MHz.
2. Outputs open.
3. $0V < V_{IN} < V_{DD}$.
4. All outputs except INT\ which is open collector.
5. All outputs.
6. Applies to SDO when tri-stated.

CAPACITANCE

($t_A = 25^0C$)

PARAMETER	SYMBOL		MAX	UNITS
Input Capacitance	C_{IN}		5	pF
Output Capacitance	C_{OUT}		7	pF

AC ELECTRICAL CHARACTERISTICS[1,2] SERIAL PORT

(0^0 C to 70^0 C, V_{DD} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SDI to SCLK Setup	t_{DC}	50			ns
SCLK to SDI Hold	t_{CDH}	50			ns
SDI to SCLK Falling Edge	t_{CD}	50			ns
SCLK Low Time	t_{CL}	250			ns
SCLK High Time	t_{CH}	250			ns
SCLK Rise and Fall Times	t_R,t_F			100	ns
CS\ to SCLK Setup	t_{CC}	50			ns
SCLK to CS\ hold	t_{CCH}	50			ns
CS\ Inactive Time	t_{CWH}	2.5			us
SCLK to SDO Valid	t_{CDV}			200	ns
CS\ to SDO High Z	t_{CDZ}			75	ns

NOTES:

1. Measured at V_{IH} = 2.0 or V_{IL} = .8 and 10ns maximum rise and fall time.
2. Output load capacitance = 100 pf.

AC ELECTRICAL CHARACTERISTICS[1,2] RECEIVE (0^0 C to 70^0 C, V_{DD} = 5V +-10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Propagation Delay RCLK to RMSYNC, RFSYNC, RSIGSEL,RSIGFR, RLCLK, RCHCLK	t_{PRS}			75	ns
Propagation Delay RCLK to RSER,RABCD,RLINK	t_{PRD}			75	ns
Transition Time All Outputs	t_{TTR}			20	ns
RCLK Period	t_P		648		ns
RCLK Pulse Width	t_{WL},t_{WH}		324		ns
RCLK Rise and Fall Times	t_R,t_F		20		ns
RPOS, RNEG Setup to RCLK Falling	t_{SRD}	50			ns
RPOS, RNEG Hold to RCLK Falling	t_{HRD}	50			ns
Propagation Delay RCLK to RLOS, RYEL, RBV, RCL, RFER	t_{PRA}			75	ns
Minimum RST\ Pulse Width	t_{RST}	1			us

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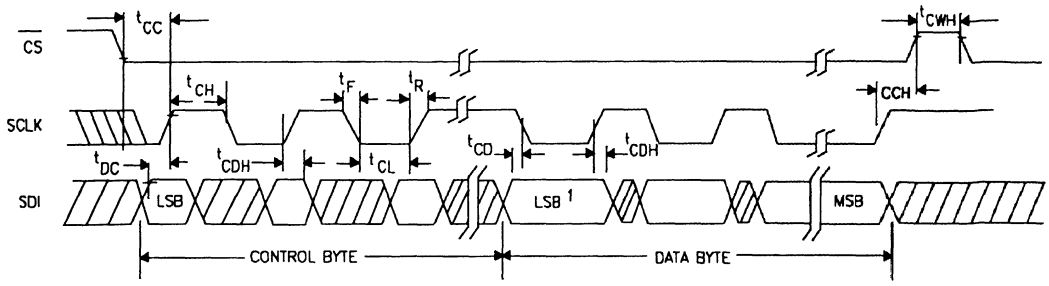
NOTES:
1. Measured at V_{IH} = 2.0 or V_{IL} = .8 and 10ns maximum rise and fall time.
2. Output load capacitance = 100 pF.

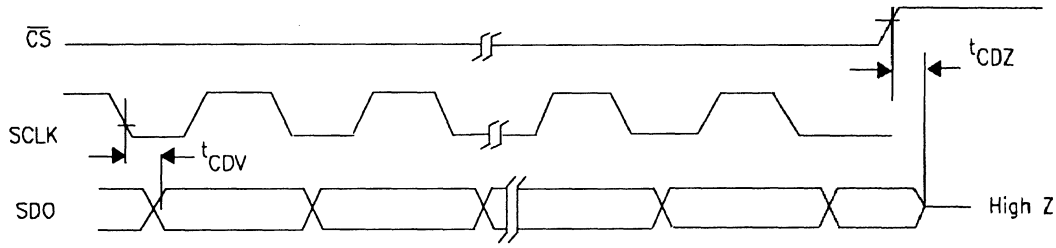
SERIAL PORT WRITE AC TIMING DIAGRAM Figure 18



NOTES:

1. Data byte bits must be valid across low clock periods to prevent transients in operating modes.
2. Shaded regions indicate don't-care states of input.

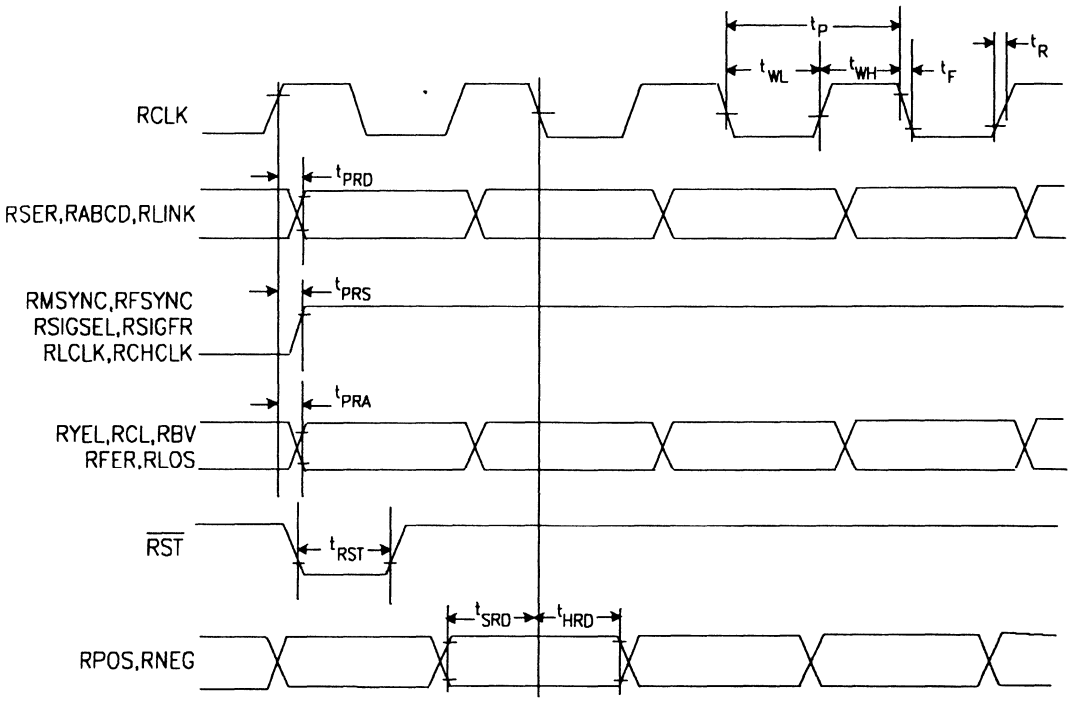
SERIAL PORT READ[1] AC TIMING DIAGRAM Figure 19



NOTE:

1. Serial port write must precede a port read to provide address information.

RECEIVE AC TIMING DIAGRAM Figure 20



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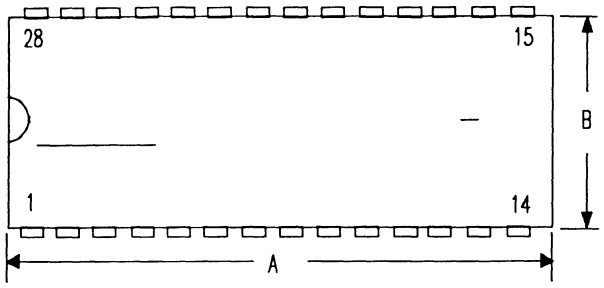
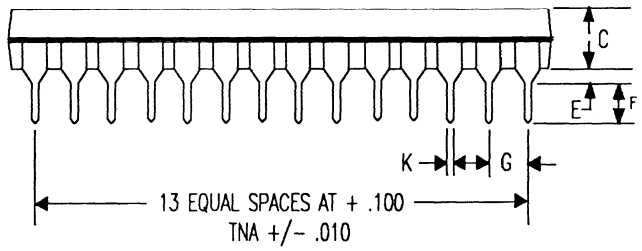
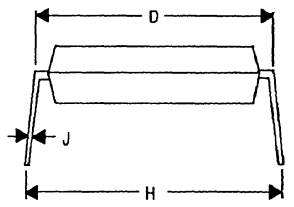
DS2182
T1 LINE MONITOR
28-PIN DIP

DIM.	INCHES	
	MIN.	MAX.
A	1.440	1.480
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

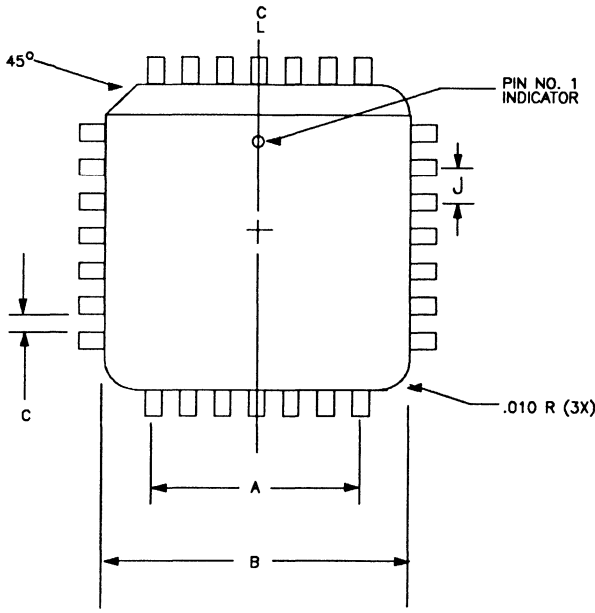


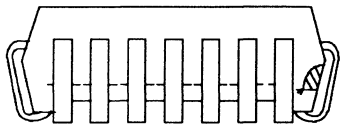


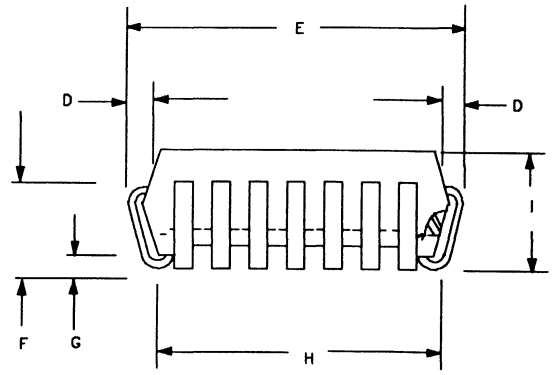


DS2182Q
T1 LINE MONITOR
28-PIN PLCC

DIM.	INCHES	
	MIN.	MAX.
A	.290	.310
B	.441	.451
C	.020	.024
D	.018	.022
E	.488	.492
F	.118	.122
G	.020	.030
H	.390	.430
I	.167	.173
J	.048	.052







LINE INTERFACES

6

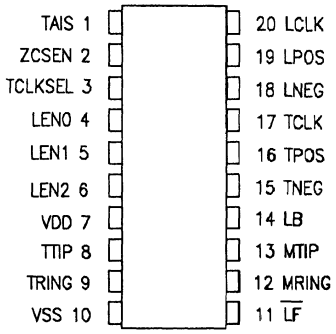
DALLAS SEMICONDUCTOR

DS2186
TRANSMIT LINE INTERFACE

FEATURES

- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- On-chip transmit LBO (line build out) and line drivers eliminate external components
- Programmable output pulse shape supports short-and long-loop applications
- Supports bipolar and unipolar input data formats
- Transparent B8ZS and HDB3 zero code suppression modes
- Compatible with DS2180A T1 and DS2181 CEPT Transceivers
- Companion to the DS2187 Receive Line Interface
- Single 5V supply; low-power CMOS technology

PIN CONNECTIONS



DESCRIPTION

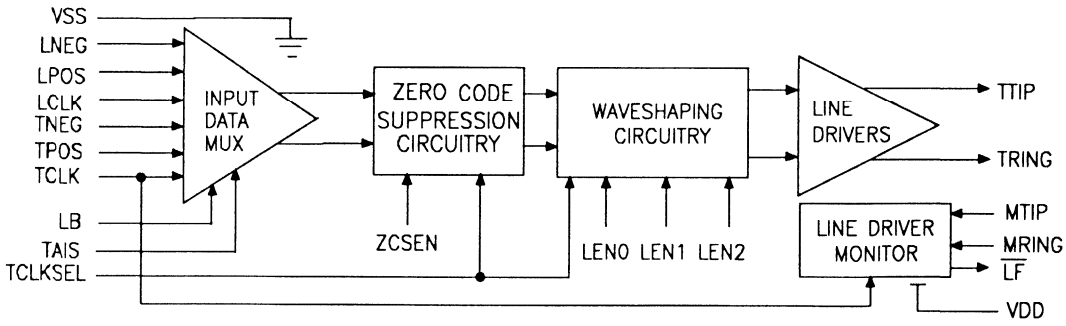
The DS2186 interfaces user equipment to North American (T1-1.544 MHz) and European (CEPT-2.048 MHz) primary rate communications networks. The device is compatible with all types of twisted pair and coax cable found in such networks.

Key on-chip components include: programmable waveshaping circuitry, line drivers, remote loopback and zero suppression logic. A line-coupling transformer is the only external component required.

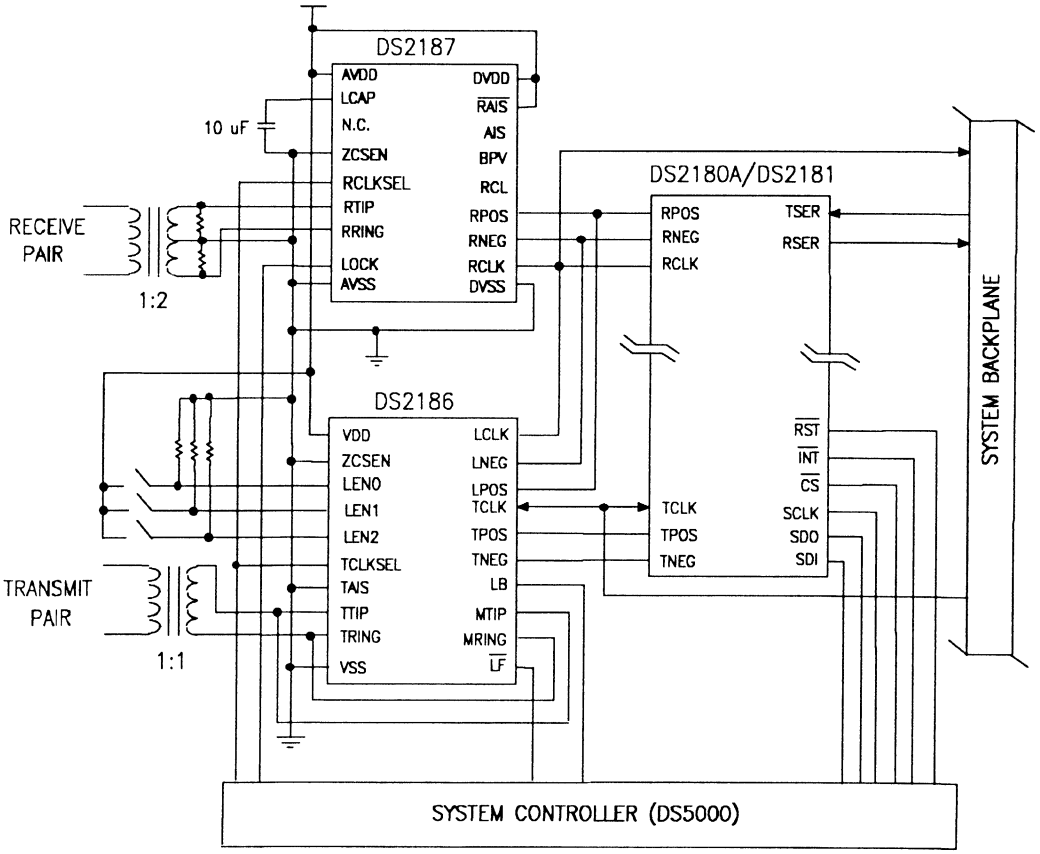
Short loop (DSX-1, 0 to 655 feet) and long loop (CSU; 0 dB, -7.5 dB and -15 dB) pulse templates found in T1 applications are supported. Appropriate CCITT Red Book recommendations are met in the CEPT mode.

Application areas include DACS, CSU, CPE, channel banks and PABX to computer interfaces such as DMI and CPI. Supports ISDN-PRI (Primary Rate Interface) specifications.

DS2186 BLOCK DIAGRAM Figure 1



SYSTEM LEVEL INTERCONNECT Figure 2



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**TAIS**	I	**Transmit Alarm Indication Signal** When high, output data is forced to all ones at the TCLK (LB = 0) or LCLK (LB = 1) rate.
2	**ZCSEN**	I	**Zero Code Suppression Enable** When high, B8ZS or HDB3 encoder enabled.
3	**TCLKSEL**	I	**Transmit Clock Select** Tie to VSS for 1.544 MHz (T1) applications, to VDD for 2.048 MHz (CEPT) applications.
4 5 6	**LEN0** **LEN1** **LEN2**	I	**Length Select 0, 1 and 2** State determines output T1 waveform shape and characteristics.
7	**VDD**	- -	**Positive Supply** 5.0 volts.
8 9	**TTIP,** **TRING**	O	**Transmit Tip and Ring** Line driver outputs; connect to transmit line transformer.
10	**VSS**	- -	**Signal Ground** 0.0 volts.
11	$\overline{\text{LF}}$	O	**Line Fault** Open collector active low output. Held low during an output driver fault and/or failure; tri-stated otherwise.
12 13	**MRING,** **MTIP**	I	**Monitor Tip and Ring** Normally connected to TTIP and TRING. Sense inputs for line fault detection circuitry.
14	**LB**	I	**Loopback** When high, input data is sampled at LPOS and LNEG on falling edges of LCLK; when low, input data is sampled at TPOS and TNEG on falling TCLK.
15 16	**TNEG,** **TPOS**	I	**Transmit Data** Sampled on falling edges of TCLK when LB = 0.
17	**TCLK**	I	**Transmit Clock** 1.544 MHz or 2.048 MHz primary data clock.
18 19	**LNEG,** **LPOS**	I	**Loopback Data** Sampled on falling edges of LCLK when LB = 1.
20	**LCLK**	I	**Loopback Clock** 1.544 MHz or 2.048 MHz loopback data clock.

INPUT DATA MODES
Input data is sampled on the falling edge of TCLK or LCLK and can be bipolar (dual rail) or unipolar (single rail, NRZ). TPOS, TNEG and TCLK are the data and clock inputs when LB = 0, LPOS, LNEG and LCLK when LB = 1. TPOS and TNEG (LPOS and LNEG) must be tied together in NRZ applications.

ZERO CODE SUPPRESSION MODES
Transmitted data is treated transparently (no zero code supression) when ZCSEN = 0. HDB3 code words replace any all-zero nibble when ZCSEN = 1 and TCLKSEL = 1. B8ZS code words replace any incoming all-zero byte when ZCSEN = 1 and TCLKSEL = 0.

ALARM INDICATION SIGNAL
When TAIS is set the all ones code is continuously transmitted at the TCLK rate (LB = 0) or the LCLK rate (LB = 1).

WAVESHAPING
The device supports T1 short loop (DSX-1; 0 to 655 feet), T1 long loop (CSU; 0 dB, -7.5 db and -15 dB) and CEPT (CCITT Red Book G.703) pulse template requirements. On-chip laser trimmed delay lines clocked by either TCLK or LCLK control a precision digital-to-analog converter to build the desired waveforms, which are buffered differentially by the line drivers.

The shape of the "pre-emphasized" T1 waveform is controlled by inputs LEN0, LEN1, and LEN2 (TCLKSEL = 0). These control inputs allow the user to select the appropriate output pulse shape to meet DSX-1 or CSU templates over a wide variety of cable types and lengths. Those cable types include ABAM, PIC and PULP.

The CEPT mode is enabled when TCLKSEL = 1. Only one output pulse shape is available in the CEPT mode; inputs LEN0, LEN1 and LEN2 can be any state except all zeros.

The line coupling transformer also contributes to the pulse shape seen at the cross-connect point. Transformers for T1 applications must be 1:1.35. Transformers for CEPT applications can be either 1:1.35 or 1:1.

The waveshaping circuitry does not contribute significantly to output jitter (less than 0.01 UIpp broadband). Output jitter will be dominated by the jitter on TCLK or LCLK. TCLK and LCLK need only be accurate in frequency, not duty cycle.

LINE DRIVERS
The on-chip differential line drivers interface directly to the output transformer. To optimize device performance, length of the TTIP and TRING traces should be minimized and isolated from neighboring interconnect.

FAULT PROTECTION
The line drivers are fault-protected and will withstand a shorted transformer secondary (or primary) without damage. Inputs MTIP and MRING are normally tied to TTIP and TRING to provide fault monitoring capability. Output LF\ will transition low if 192 TCLK cycles occur without a one occuring at MTIP or MRING. LF\ will tri-state on the next one occurrence or two TCLK periods later, whichever is greater.

The one threshold of MTIP and MRING varies with the line type selected at LEN0, LEN1 and LEN2. This insures detection of the lowest level zero to one transition (-15 dB buildout) as it occurs on TTIP and TRING.

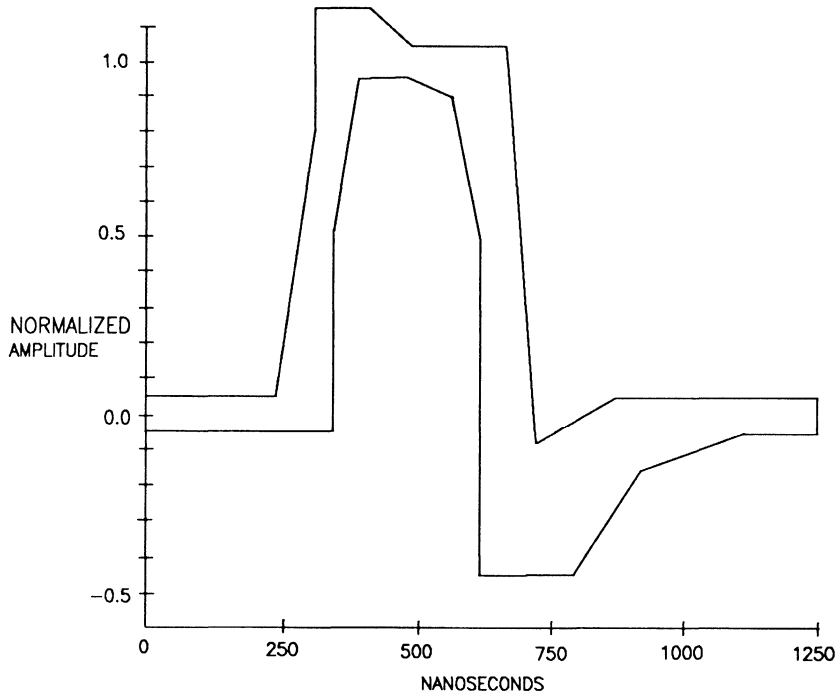
T1 LINE LENGTH SELECTION Table 2

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	0	0	Test mode	Do not use
0	0	1	-7.5 dB buildout	T1 CSU
0	1	0	-15 dB buildout	T1 CSU
0	1	1	0 dB buildout, 0 - 133 feet	T1 CSU, DSX-1 Crossconnect
1	0	0	133 - 266 feet	DSX-1 Crossconnect
1	0	1	266 - 399 feet	DSX-1 Crossconnect
1	1	0	399 - 533 feet	DSX-1 Crossconnect
1	1	1	533 - 655 feet	DSX-1 Crossconnect

NOTE:

1. The LEN0, LEN1 and LEN2 inputs control T1 output waveshapes when TCLKSEL = 0. The G.703 (CEPT) template is selected when TCLKSEL = 1 and LEN0, LEN1 and LEN2 are at any state except all zeros.

DSX-1 ISOLATED PULSE TEMPLATE Figure 3

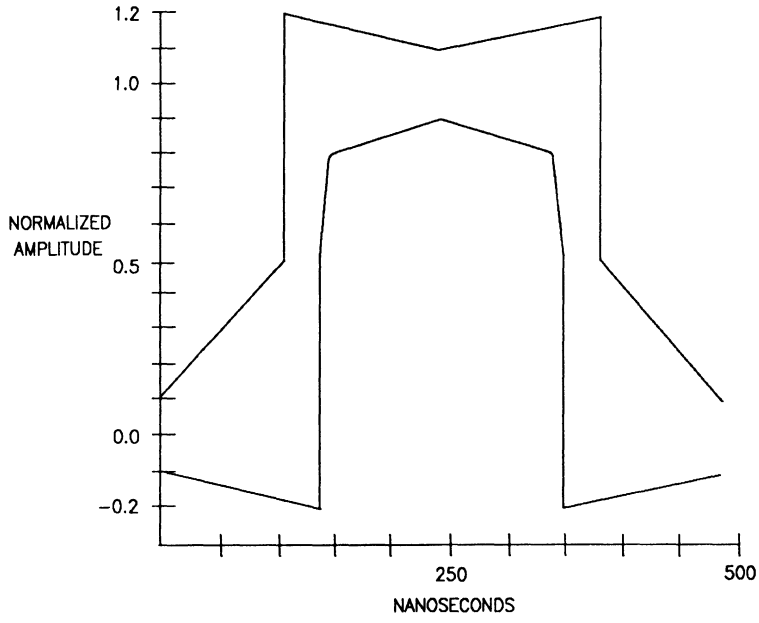


NOTES:

1. Template shown is measured at the cross-connect point.
2. Amplitude shown is normalized; the actual midpoint voltage measured may be between 2.4 and 3.6 volts.
3. The corner points shown below are joined by straight lines to form the template.

MAXIMUM CURVE	MINIMUM CURVE
(0, 0.05)	(0, -0.05)
(250, 0.05)	(350, -0.05)
(325, 0.80)	(350, 0.5)
(325, 1.15)	(400, 0.95)
(425, 1.15)	(500, 0.95)
(500, 1.05)	(600, 0.9)
(675, 1.05)	(650, 0.5)
(725, -0.07)	(650, -0.45)
(875, 0.05)	(800, -0.45)
(1250, 0.05)	(925, -0.2)
	(1100, -0.05)
	(1250, -0.05)

OUTPUT PULSE TEMPLATE AT 2.048 MHz Figure 4



NOTES:

1. Unlike the DSX-1 template, which is specified at the cross-connect point, the CEPT (2.048 MHz) template is specified at the transmit line output.
2. The template shown above is normalized. The actual pulse height is cable dependent and is specified in Table 3.
3. The corner points shown below are joined by straight lines to form the template.

MAXIMUM CURVE	MINIMUM CURVE
(0, 0.1)	(0, -0.1)
(109.5, 0.5)	(134.5, -0.2)
(109.5, 1.2)	(134.5, 0.5)
(244, 1.1)	(147, 0.8)
(378.5, 1.2)	(244, 0.9)
(378.5, 0.5)	(341, 0.8)
(488, 0.1)	(353.5, 0.5)
	(353.5, -0.2)
	(488, -0.1)

CHARACTERISTICS OF T1 AND CEPT INTERFACES Table 3

CHARACTERISTIC	T1	CEPT
LINE RATE	1.544 MHz	2.048 MHz
LINE CODE	AMI[1] or B8ZS	AMI or HDB3
TEST LOAD IMPEDANCE	100 Ohm Resistive	120 Ohm Resistive (wire pair) 75 Ohm Resistive (coax)
NOMINAL PEAK VOLTAGE	2.4 V to 3.6 V[2]	3.0 V (wire pair) 2.37 V (coax)
PULSE SHAPE	--Scaled to fit templates shown--	
NOMINAL PULSE WIDTH	324 ns.	244 ns.
PULSE IMBALANCE	< 0.5 dB difference between total power of positive and negative pulses.	1) Negative peak = positive peak peak +/- 5% 2) Positive width at nominal half amplitude = negative width at nominal half amplitude +/- 5%.

NOTES:
1. With a ones density of at least 12.5% and no more than 15 consecutive zeros.
2. Measured at the cross-connect (DSX-1) point; CSU applications may be 7.5 to 15 dB below these levels.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	1.0V to +7V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply	V_{DD}	4.75		5.25	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70° C, V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{DD}		50		mA	2,3
Supply Current	I_{DD}		35		mA	2,4
Supply Current	I_{DD}		20		mA	2,5
Input Leakage	I_{IL}	-1.0		+1.0	uA	6
Output Current @ 0.4V	I_{OL}	+4.0			mA	7

NOTES:

1. All inputs except MTIP and MRING.
2. V_{DD} = 5.25v; TCLK = LCLK = 1.544 MHz; output line transformer and load as shown in Figure 2.
3. TAIS = 1
4. 50% ones density.
5. All zeros at data inputs.
6. 0.0V $\leq V_{IN} \leq$ 5.0V.
7. Output LF (open collector).

CAPACITANCE (t_A = 25°C)

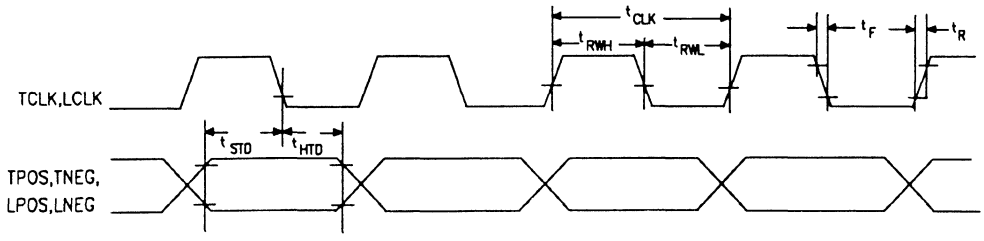
PARAMETER	SYMBOL		MAX	UNITS
Input Capacitance	C_{IN}		5	pF
Output Capacitance	C_{OUT}		7	pF

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
TCLK, LCLK Period	t_{CLK}		648		ns	1
TCLK, LCLK Period	t_{CLK}		488		ns	2
TCLK, LCLK Pulse Width	t_{RWH}, t_{RWL}	70	324		ns	1
TCLK, LCLK Pulse Width	t_{RWH}, t_{RWL}	70	244		ns	2
TCLK, LCLK Rise and Fall Times	t_R, t_F			20	ns	
TPOS, TNEG Setup to TCLK Falling	t_{STD}	50			ns	
LPOS, LNEG Setup to LCLK Falling	t_{STD}	50			ns	
TPOS, TNEG Hold from TCLK Falling	t_{HTD}	50			ns	
LPOS, LNEG Hold from LCLK Falling	t_{HTD}	50			ns	

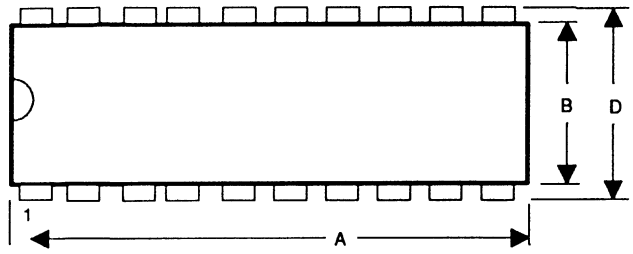
NOTES:
1. T1 applications.
2. CEPT applications.

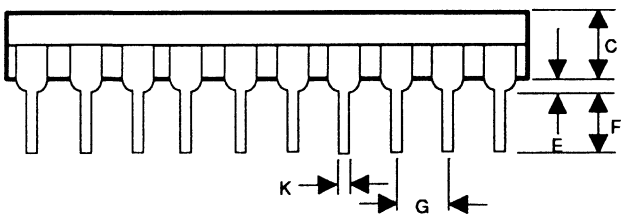
AC TIMING DIAGRAM Figure 5

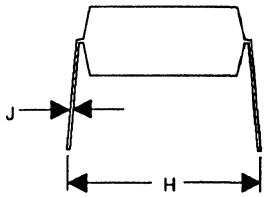


DS2186
TRANSMIT LINE INTERFACE
20-PIN DIP

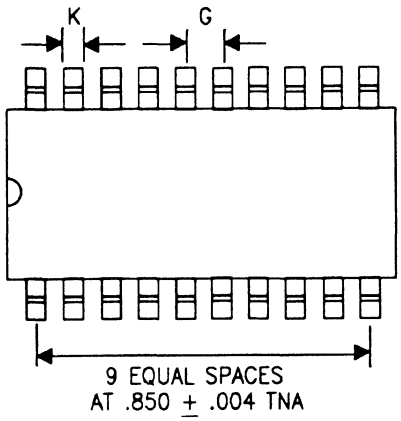
DIM.	INCHES	
	MIN.	MAX.
A	.960	1.040
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021



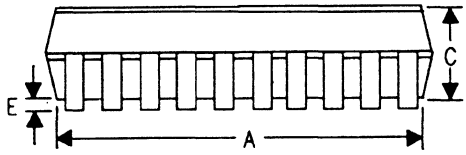


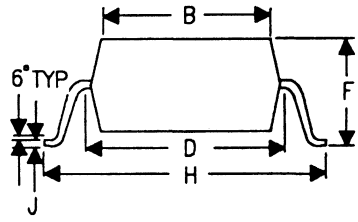


DS2186S
TRANSMIT LINE INTERFACE
20-PIN SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.503	.511
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019



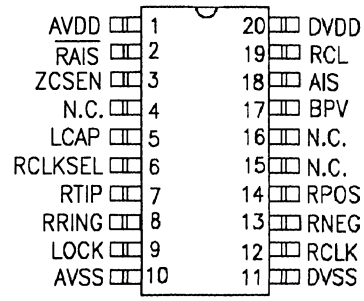


DALLAS SEMICONDUCTOR

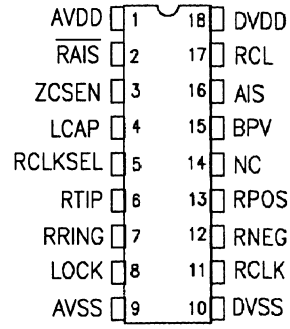
DS2187
RECEIVE LINE INTERFACE

FEATURES
- Line interface for T1 (1.544 MHz) and CEPT (2.048 MHz) primary rate networks
- Extracts clock and data from twisted pair or coax
- Meets requirements of PUB 43801, PUB 62411 and applicable CCITT G.823
- Precision on-chip PLL eliminates external crystal or LC tank -- no tuning required
- Decodes AMI, B8ZS and HDB3 coded signals
- Designed for short loop applications such as terminal equipment to DSX-1
- Reports alarm and error events
- Compatible with the DS2180A T1 and DS2181 CEPT Transceivers
- Companion to the DS2186 Transmit Line Interface
- Single 5V supply; low-power CMOS technology

PIN CONNECTIONS



20-PIN SOIC

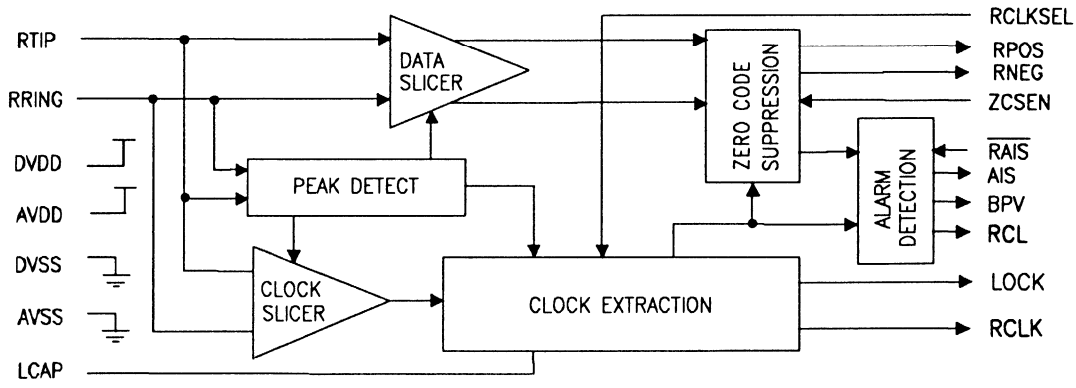


18-PIN DIP

DESCRIPTION
The DS2187 interfaces user equipment to North American (T1 - 1.544 MHz) and European (CEPT 2.048 MHz) primary rate communication networks. The device extracts clock and data from twisted pair or coax transmission media and eliminates expensive discrete components and/or manual tuning required in existing T1 and CEPT line termination electronics.

Application areas include DACS, CSU, CPE, channel banks and PABX-to-computer interfaces such as DMI and CPI.

DS2187 BLOCK DIAGRAM Figure 1



6

LINE INPUT

Input signals are coupled to the DS2187 via a 1:2 center-tapped transformer as shown in Figure 2. For T1 applications, R1 and R2 must be 200 ohms in order to properly terminate the line at 100 ohms. R1 and R2 are set at 150 ohms for CEPT applications. Special internal circuitry of the RTIP and RRING inputs permits negative signal excursions below VSS, which will occur in the circuit in Figure 2.

PEAK DETECTOR AND SLICERS

Signal pulses present at RTIP and RRING are sampled by an internal peak detect circuit. The data slicer threshold is set for 50% of the sampled peak voltage. The clock slicer threshold is set higher at 70% to prevent the negative undershoot of a worst-case DSX-1 pulse from causing erroneous clocking.

Peak input levels at RRIP and RRING must exceed 0.6 volts to establish minimum slicer thresholds. Signals below this level will cause RCL to transition high after 192 bit times.

CLOCK EXTRACTION

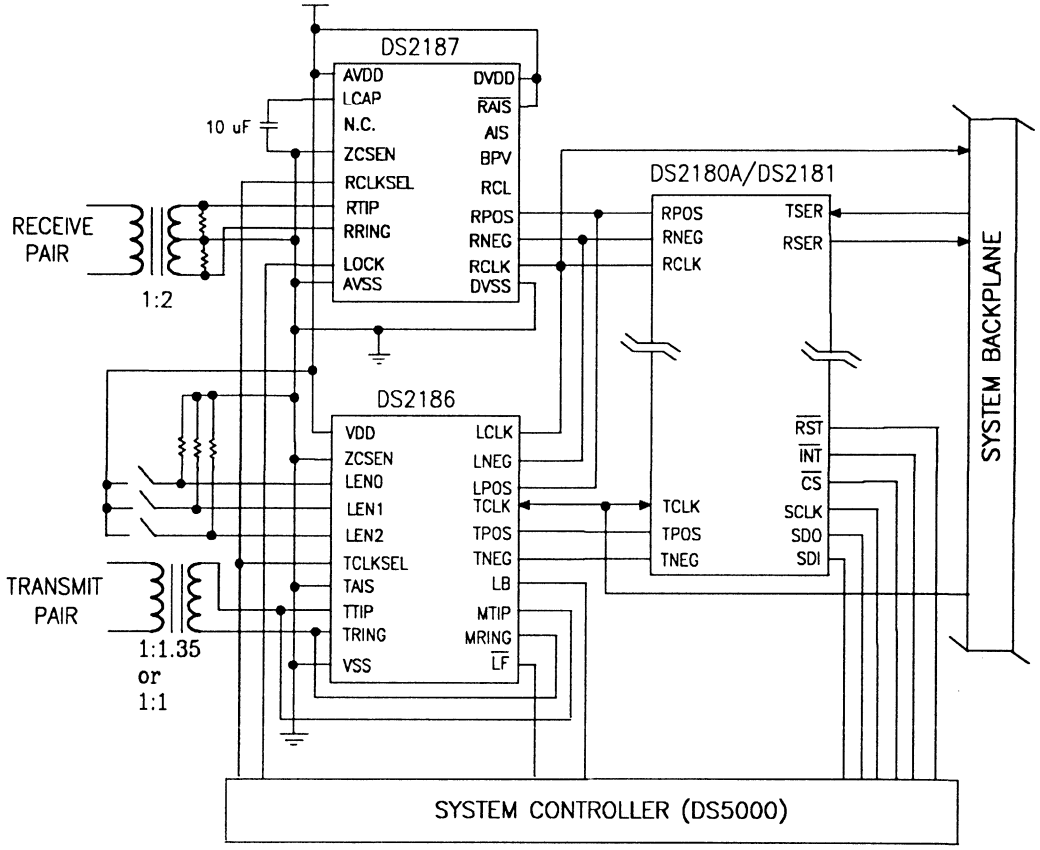
The DS2187 utilizes both frequency-locked (FLL) and digital phase locked (DPLL) loops to recover data and clock from the incoming AMI signal. The DPLL characteristics differ for T1 and CEPT modes. T1 applications utilize a 18.528 MHz clock divided by either 11, 12, or 13 to match the phase of the incoming jittered line signal. This technique affords exceptional jitter tracking which enables the DS2187 to meet the latest AT&T PUB 62411 and ECSA jitter specifications. A 16.384 MHz clock divided by 7, 8, or 9 provides jitter tracking in the CEPT mode. The DPLL output is buffered and presented at RCLK. An on-chip, laser-trimmed voltage controlled oscillator (VCO) provides the precision 18.528 MHz and 16.384 MHz frequency sources utilized in the FLL. The FLL is a high-Q circuit which tracks the average frequency of the incoming signal, minimizing the effect of the DPLL on output jitter.

During the acquisition time or if RCL goes high, the LOCK pin will go low to indicate a loss of synchronization to the line signal. Once this pin goes high, the FLL has achieved frequency lock and valid data is present at the RPOS and RNEG outputs.

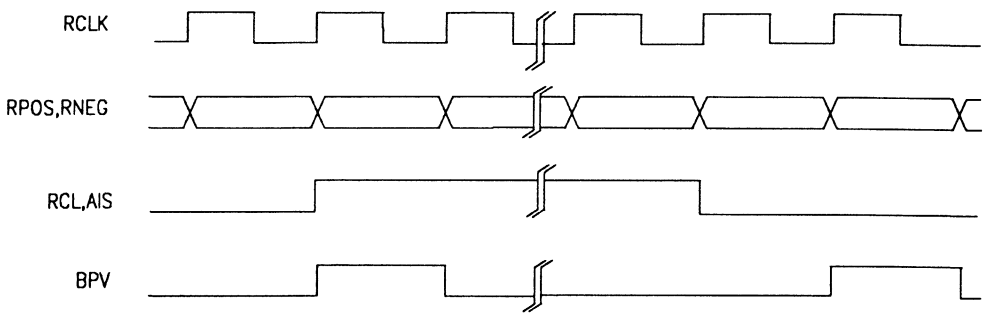
PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**AVDD**	-	**Analog Positive Supply.** 5.0 Volts.
2	**$\overline{\text{RAIS}}$**	I	**Reset Alarm Indication Signal.** Every other low pulse at this input establishes the AIS alarm detection period.
3	**ZCSEN**	I	**Zero Code Supression Enable.** When high, incoming B8ZS (RCLKSEL = 0) or HDB3 (RCLKSEL =1) code words are replaced with all zeros at RPOS and RNEG; when low, no code replacement occurs.
4	**LCAP**	-	**Loop Cap.** Part of internal loop filter; attach a 10 microfarad capacitor from this pin to VSS.
5	**RCLKSEL**	I	**Receive Clock Select.** Tie to VSS for 1.544 MHz (T1) applications, to VDD for 2.048 MHz (CEPT) applications.
6 7	**RTIP** **RRING**	I	**Receive Tip and Ring.** Connect to line transformer as shown in Figure 2.
8	**LOCK**	0	**Frequency Lock.** High state indicates that internal circuitry is phase-and frequency-locked to the incoming signal at RRING and RTIP.
9	**AVSS**	-	**Analog Signal Ground.** 0.0 Volts.
10	**DVSS**	-	**Digital Signal Ground.** 0.0 Volts.
11	**RCLK**	-	**Receive Clock.** Extracted line rate clock.
12, 13	**RNEG** **RPOS**	0	**Receive Data.** Extracted receive data; updated on rising edge of RCLK.
14	**NC**	-	**No Connect.** Do not connect to this pin.
15	**BPV**	0	**Bipolar Violation.** Transitions high for the full bit period when a bit in violation appears at RPOS or RNEG; B8ZS or HDB3 code words are not accused when ZCSEN = 1.
16	**AIS**	0	**Alarm Indication Signal.** High when the received data stream has contained less than three zeros during the last two periods of the $\overline{\text{RAIS}}$ signal.
17	**RCL**	0	**Receive Carrier Loss.** High if 192 zeros appear at RPOS and RNEG; reset on next one occurrence.
18	**DVDD**	-	**Digital Positive Supply.** 5.0V.

SYSTEM LEVEL INTERCONNECT Figure 2



OUTPUT TIMING Figure 3



ZERO CODE SUPPRESSION

The device will decode incoming B8ZS (RCLKSEL = 0) or HDB3 (RCLKSEL = 1) code words and replace them with an all zero code when ZCSEN = 1. When ZCSEN = 0, code words will pass through the device without being altered. This feature can be disabled when the DS2187 is used with transceiver devices such as the DS2180A or DS2181.

ALARM DETECTION

The extracted data is monitored for network alarm and error conditions. RCL is set when 192 consecutive zeros occur; it is cleared on the next one occurrence. AIS is set when less than three zeros have appeared at RPOS and RNEG during the last two periods of the RAIS signal; once set, AIS will remain high for the next two periods of RAIS. $\overline{\text{AIS}}$ will return low when more than two zeros appear. BPV reports bipolar violations as they occur at RPOS and RNEG; B8ZS and HDB3 code words will not be flagged by BPV when ZCSEN = 1.

BYPASSING AND LAYOUT CONSIDERATIONS

The DS2187 contains both precision analog and high-speed digital circuitry on the same chip. The power supplies of these circuits (AVDD, AVSS, DVDD and DVSS) should be connected to system analog and digital supplies. If separate system supplies do not exist, the appropriate supply pins can be tied together. Tying the analog and digital supplies together on the DS2187 will not degrade its performance.

To assure optimum performance, the length of LCAP, RTIP and RRING printed circuit board traces should be minimized and isolated from neighboring interconnect.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground**	-	-1.0V to +7V
Operating Temperature	-	0°C to 70°C
Storage Temperature	-	-55°C to 125°C
Soldering Temperature	-	260°C for 10 Sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect reliability.
** Inputs other than RTIP and RRING.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX.	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1
Supply RTIP, RRING	V_{DD}	4.75		5.25	V	
Input Voltage Swing	V_{IN}	-7.0		12.0	V	

D.C. ELECTRICAL CHARACTERISTICS (0° C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Supply Current	I_{DD}		18	25	mA	2
Input Leakage	I_{IL}	-1.0		+10	uA	1,3
Output Current @ 2.4V	I_{OH}	-1.0			mA	4
Output Current @ 0.4V	I_{OL}	+4.0			mA	4

NOTES:
1. All inputs except RTIP and RRING.
2. Outputs open.
3. $0.0V < V_{IN} < V_{DD}$.
4. All outputs.

ANALOG ELECTRICAL CHARACTERISTICS

(0° to 70°C, V_{DD} = 5V +/-5%)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
Clock Acquisition	t_{LOCK}		50		ms	1
RTIP, RRING Minimum Sensitivity	V_{THRES}		.4	.6	V_{pk}	2
FLL Loop Bandwidth	f_{BW}		50		Hz	3
Capture Range	f_{CAP}		± 6		%	4
Input Jitter Tolerance	J_{IN}	200			UI	5

NOTES:
1. Time from reappearance of a valid signal at RPOS and RNEG to a LOCK = 1.
2. Minimum peak voltage necessary for proper processing of signal.
3. Loop bandwidth when in lock (LOCK = 1).
4. When out-of-lock (LOCK = 0); measured as a percent of incoming clock frequency.
5. Maximum input jitter in unit-intervals at 10 Hz.

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

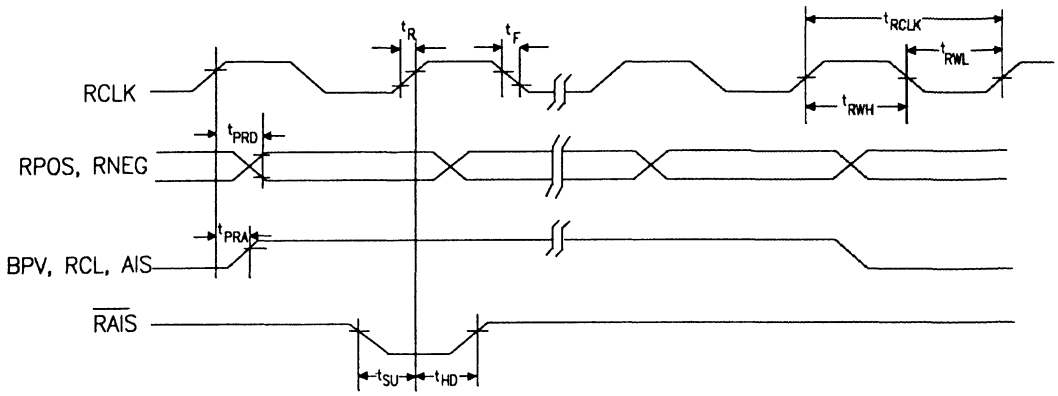
AC ELECTRICAL CHARACTERISTICS

(0° to 70°C, V_{DD} = 5V ± 5%)

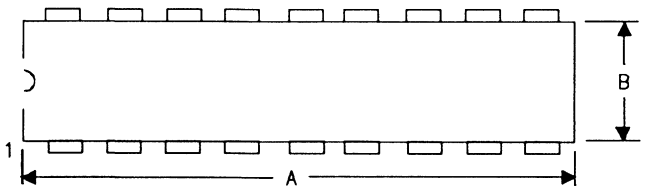
PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS	NOTES
RCLK Period	t_{RCLK}	594	648	702	ns	1,3
RCLK Period	t_{RCLK}	427	488	549	ns	2,3
RCLK Pulse Width	t_{RWH}, t_{RWL}		324		ns	1
RCLK Pulse Width	t_{RWH}, t_{RWL}		244		ns	2
RCLK Rise and Fall Time	t_R, t_F			20	ns	
Propagation Delay RCLK to RPOS, RNEG	t_{PRD}			75	ns	
Propagation Delay RCLK to BPV, RCL, AIS	t_{PRA}			75	ns	
$\overline{\text{RAIS}}$ Setup	t_{SU},t_{HD}	50			ns	

NOTES:
1. T1 applications (RCLKSEL = 0).
2. CEPT applications (RCLKSEL = 1).
3. Minimum and maximum limits shown reflect changes in DPLL divide ratio as required to track jitter.

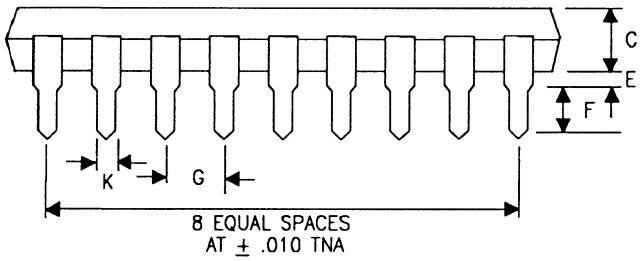
AC TIMING DIAGRAM Figure 4

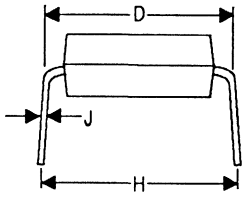


DS2187
RECEIVE LINE INTERFACE
18-PIN DIP

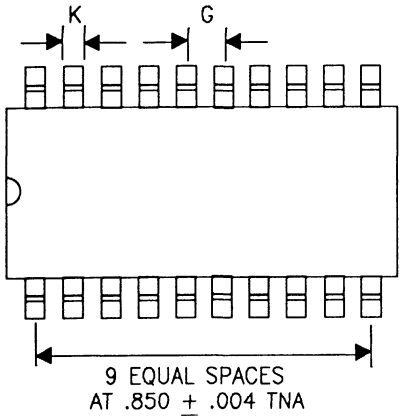


DIM.	INCHES	
	MIN.	MAX.
A	.850	.910
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.040
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021

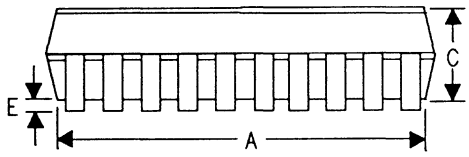


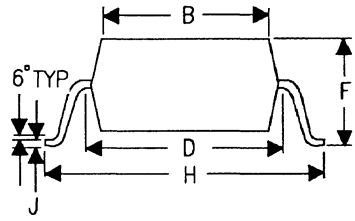


DS2187S
RECEIVE LINE INTERFACE
20-PIN SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.503	.511
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019





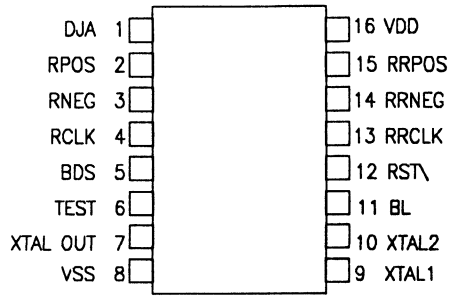
DALLAS SEMICONDUCTOR

DS2188
T1/CEPT JITTER ATTENUATOR

FEATURES

- Attenuates clock and data jitter present in T1 or CEPT lines
- Meets the jitter attenuation templates outlined in TR62411, TR-TSY-000170, G.735, and G.742
- Only one external component required; either a 6.176MHz (T1) or 8.192MHz (CEPT) crystal
- Selectable buffer size of 128 or 32 bits
- Jitter attenuation is easily disabled
- Single +5V supply; low-power CMOS technology
- Available in 16-pin DIP and 16-pin SOIC

PIN DESCRIPTION



6

DESCRIPTION

The DS2188 contains a 128 X 2-bit buffer which, in conjuction with an external 4X crystal, is used to attenuate the incoming jitter present in clock and data. The device meets all of the latest applicable specifications including those outlined in TR 62411(ACCUNET* T1.5 Service Description and Interface Specifications- December 1988), TR-TSY-000170(Digital Cross-Connect System Requirements and Objectives -November 1985), and the CCITT Recommendations G.735 and G.742. The DS2188 is compatible with the DS2180A and DS2181 transceivers and it is the companion to the DS2187 Receive Line Interface and DS2186 Transmit Line Interface. It can also be used in conjunction with the DS2190 Network Interface Unit.

*Service mark of AT&T Communciations

OVERVIEW

The RCLK input is fed to a 128 x 2 bit FIFO where it drives the write pointer for the positive (RPOS) and negative (RNEG) data. The read pointer of the FIFO and RRCLK is generated by dividing the frequency of the crystal connected to XTAL1 and XTAL2 by four. The frequency of the crystal is adjusted by a DPLL to the long-term average frequency of RCLK. As long as the jitter present at RCLK is less than 120 unit intervals peak-to-peak (UIpp), then the FIFO buffer will be able to absorb the incoming jitter and it will be attenuated in accordance with TR 62411 (December 1988). In this situation, the BL (Buffer Limit) pin will remain low. How the DS2188 performs in T1 and CEPT environments is shown in Figures 1 and 2.

If the incoming jitter has excursions greater than 120 UIpp, then the crystal is adjusted to track the short-term frequency variations of the incoming signal so that there is no loss of data. This adjustment is accomplished by dividing the 4X crystal by either 3 1/2 or 4 1/2 instead of 4. When the incoming jitter is greater than 120UIpp, the BL pin will go high. When the incoming jitter returns to less than 120UIpp, the BL pin will return low.

The jitter attenuator in the DS2188 can be disabled by tying the DJA pin high. When the jitter attenuator is disabled, the FIFO is bypassed and jitter received at RCLK, RPOS and RNEG is passed through the DS2188 to RRCLK, RRPOS, and RRNEG. In this situation, the BL pin has no significance and XTAL OUT will not be coherent with RRCLK.

How to use the DS2188 with Dallas Semiconductor's other T1 and CEPT line interface parts is shown in Figures 3 through 5. Figure 3 demonstrates how to place the DS2188 in the receive path along with a DS2187 Receive Line Interface. Figure 4 shows how to use the DS2188 in the transmit path with the DS2186 Transmit Line Interface. And a description of how to use the DS2188 with the DS2190 Network Interface Unit appears in Figure 5.

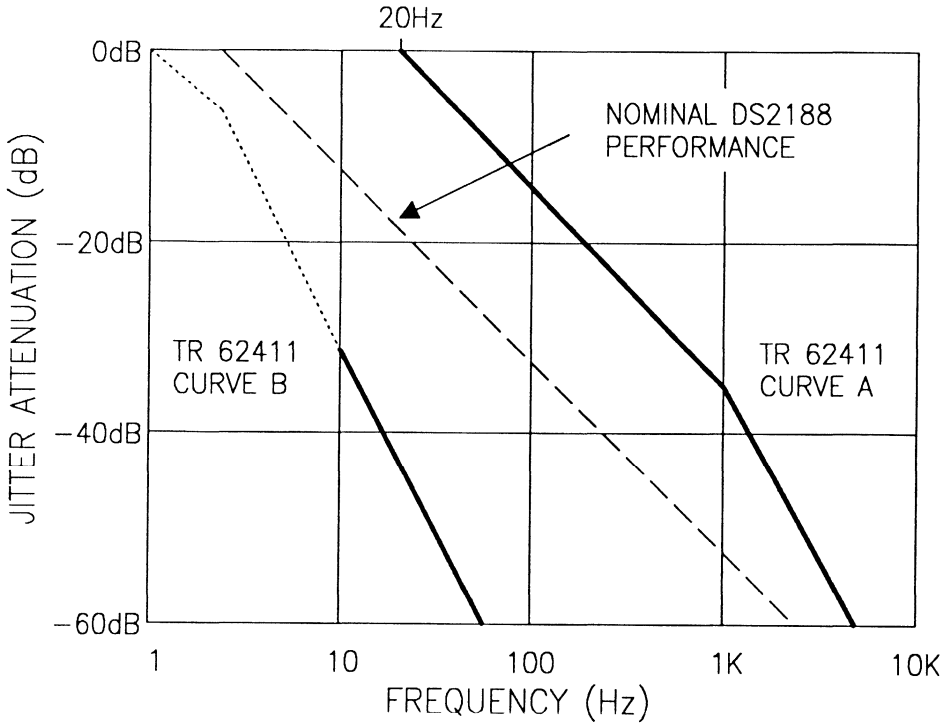
BUFFER DEPTH SELECT

The buffer size on the DS2188 can be configured to either 128 or 32 bits via the BDS pin. If BDS is tied low, then the buffer depth will be 128 bits and hence can handle input jitter up to 120 UIpp without losing its full attenuation capabilities as is described above in the Overview. If BDS is tied high, then the buffer depth is shortened to 32 bits. In this configuration, the DS2188 can handle input jitter up to 28 UIpp without losing its full jitter attenuation capabilities. The user may wish to limit the buffer size to 32 bits in applications where throughput delay is critical or into existing applications that already have 32 bits of buffer space.

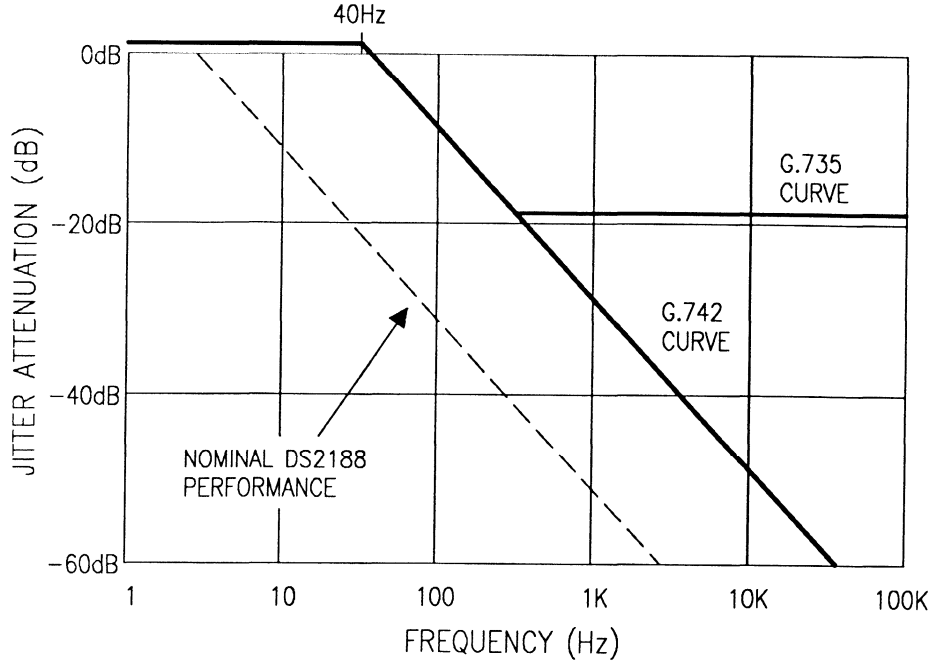
RESET

The buffer on the DS2188 is automatically centered on power-up. The user can recenter the 128-bit (or 32-bit) buffer on demand via the RST\ pin. The RST\ pin on the DS2188 is negative-edge triggered. When this pin transitions from high-to-low, the buffer is recentered. The RST\ pin can be held either high or low during operation of the DS2188; only a negative going signal will initiate a recentering. In most cases, a reset of the DS2188 will corrupt data that is currently passing through the buffer.

DS2188 T1 JITTER ATTENUATION PERFORMANCE Figure 1

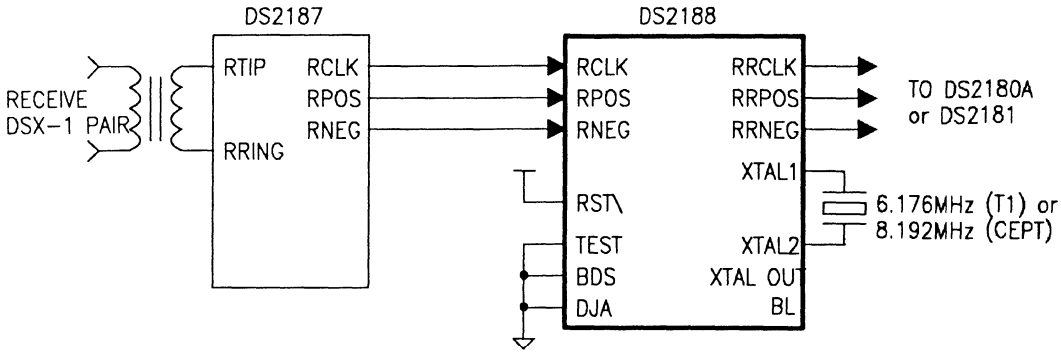


DS2188 CEPT JITTER ATTENUATION PERFORMANCE Figure 2

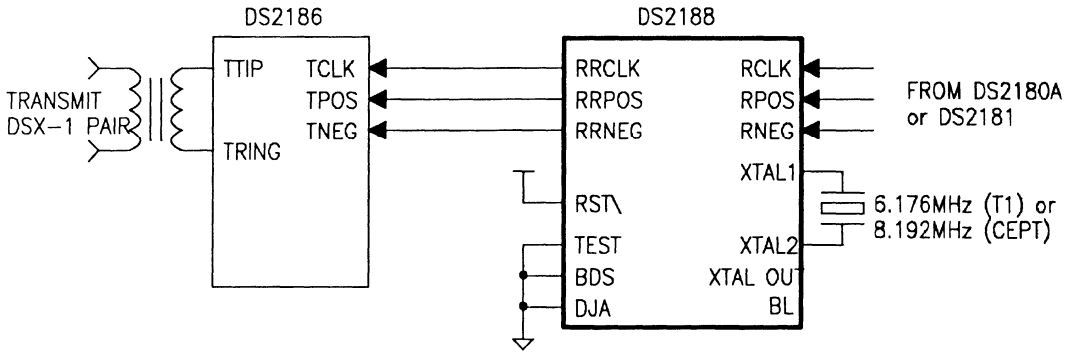


6

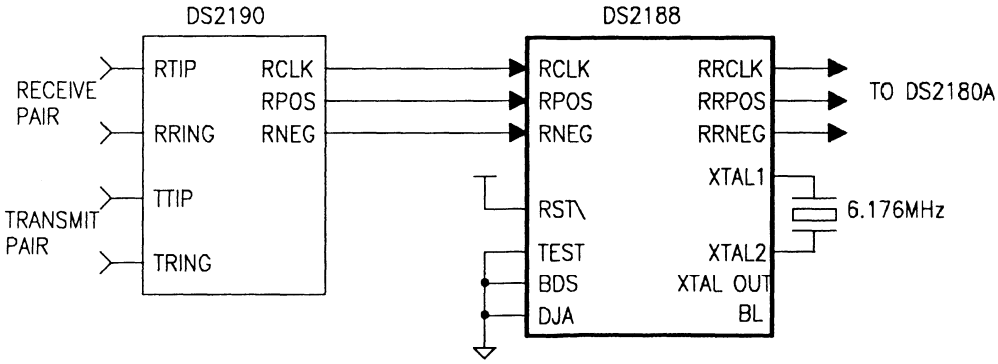
DS2188 IN THE RECEIVE PATH Figure 3



DS2188 IN THE TRANSMIT PATH Figure 4



USE OF DS2188 WITH THE DS2190 Figure 5



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**DJA**	I	**Disable Jitter Attenation.** When high, jittered data and clock at RPOS, RNEG, and RCLK is passed directly to RRPOS, RRNEG, and RRCLK.
2	**RPOS**	I	**Receive Positive Data Input.** Jittered data input. Sampled on the falling edge of RCLK.
3	**RNEG**	I	**Receive Negative Data Input.** Jittered data input. Sampled on the falling edge of RCLK.
4	**RCLK**	I	**Receive Clock Input.** Jittered input 1.544MHz or 2.048MHz clock.
5	**BDS**	I	**Buffer Depth Select.** 0 = 128 bits 1 = 32 bits
6	**TEST**	I	**Test Input.** In normal applications, this pin should be tied low.
7	**XTAL OUT**	O	**Crystal Frequency Output.** Buffered output of the 4X crystal connected to XTAL1 and XTAL2.
8	**VSS**	-	**Ground.** 0.0 Volts.
9 10	**XTAL1** **XTAL2**	I O	**Crystal Connections.** In T1 environments, connect a 6.176MHz crystal to these pins. In CEPT environments, connect a 8.192MHz crystal to these pins.
11	**BL**	O	**Buffer Limit.** Transitions high when the buffer fills or empties to within either 4 bits (BDS=0) or 2 bits (BDS=1) of its capacity. Indicates that the jitter at RCLK is greater than 120UIpp (BDS=0) or 28UIpp (BDS=1).
12	**RST**	I	**Reset.** Negative-edge triggered; a high-low transition will recenter the buffer. Activation of this pin will corrupt data through the DS2188.
13	**RRCLK**	O	**Receive Reference Clock.** Dejittered 1.544MHz or 2.048MHz clock.
14	**RRNEG**	O	**Receive Reference Negative Data Output.** Dejittered data output. Updated on the rising edge of RRCLK.
15	**RRPOS**	O	**Receive Reference Positive Data Output.** Dejittered data output. Updated on the rising edge of RRCLK.
16	**VDD**	-	**Positive Supply.** 5.0 Volts.

032190 5/10

CRYSTAL REQUIREMENTS

The DS2188 must have a crystal connected to the XTAL1 and XTAL2 pins. For T1 environments, the frequency of this crystal should be 6.176MHz. For CEPT environments, the frequency of this crystal should be 8.192MHz. Table 2 lists some suggested crystal manufacturers that are recommended for use with the DS2188.

CRYSTAL MANUFACTURERS Table 2

Manufacturer	Part #	Frequency
JAN Crystal	6323-00	6.176MHz 8.192MHz
M-TRON	MP-1 6.176 MP-1 8.192	6.176MHz 8.192MHz

CRYSTAL SELECTION GUIDELINES FOR THE DS2188

1. The crystal should be designed to nominally resonate with a parallel capacitance of 18pF to 20pF.

2. When the crystal is resonating with its proper parallel resonance capacitance (18pF to 20pF), it should resonate at a frequency within +/- 50ppm of its nominal frequency (6.176MHz or 8.192MHz).

3. In order to guarantee pullability, the crystal should have one of the following two parameters:

A. The difference between the open circuit parallel resonance (no shunt capacitor) and the series resonance should be on the order of 2100ppm (+/-30%).

-or-

B. The ratio of the holder capacitance to the motional capacitance should be on the order of 230 (+/-30%).

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic1	VIH	2.0		VCC+0.3	V	1
Logic 0	VIL	-0.3		+0.8	V	1
Supply	VDD	4.50		5.50	V	

NOTES:

1.Does not apply to XTAL1.

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		5		pF	
Output	COUT		10		pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	IDD		4	8	mA	1
Input Leakage	IL	-1.0		+1.0	uA	2,3
Output Current (2.4V)	IOH	-1.0			mA	3
Output Current (0.4V)	IOL	+4.0			mA	3

NOTES:

1. RCLK = 1.544MHZ; VDD = 5.50; outputs open.
2. VSS < Vin < VDD: XTAL1 = XTAL2 = V_{DD}.
3. Does not apply to XTAL1 or XTAL2.

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AC ELECTRICAL CHARACTERISTICS

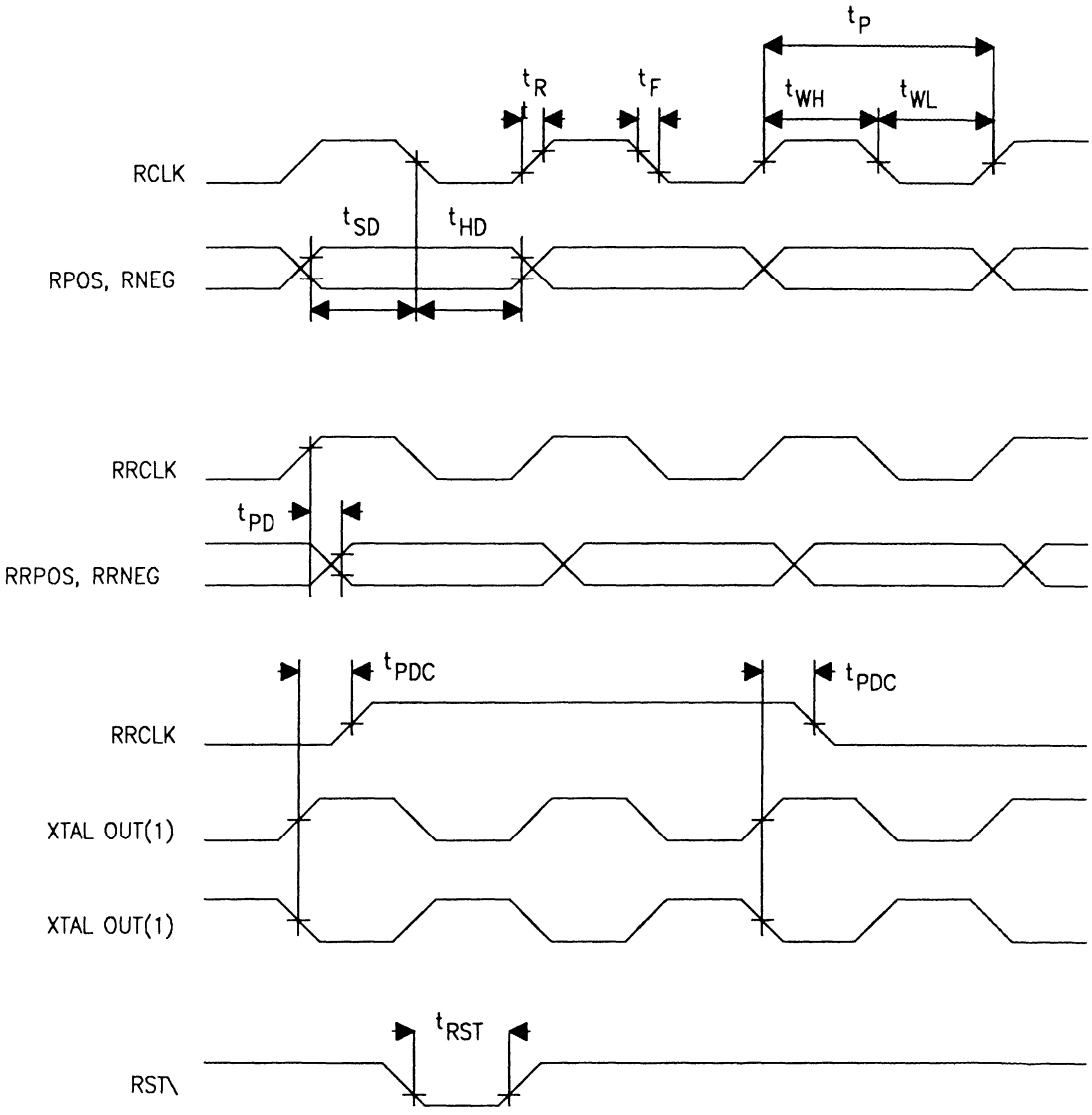
(0°C to 70°C; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_P	-200		+200	ppm	1
RCLK Pulse Width	t_{WH},t_{WL}	100			ns	
RCLK Rise and Fall Times	t_R, t_F			50	ns	
RPOS, RNEG Setup to RCLK	t_{SD}	50			ns	
RPOS, RNEG Hold from RCLK	t_{HD}	50			ns	
Propagation Delay from RRCLK to RRPOS, RRNEG Valid	t_{PD}			50	ns	
Propagation Delay from XTAL OUT to	t_{PDC}			50	ns	2
RRCLK RST\ Pulse Width	t_{RST}	1			us	

NOTES:

1. The average period of RCLK must be within +/-200ppm of the fundamental frequency of the crytsal divided by four.
2. Only valid when the incoming jitter is less than 120UIpp (BDS=0) or 28UIpp (BDS=1).

AC TIMING DIAGRAM Figure 6

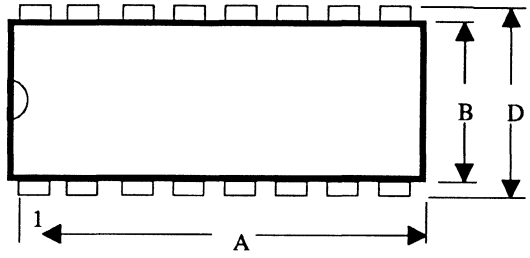


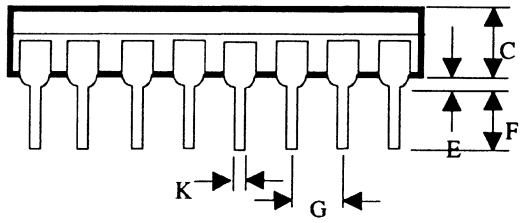
NOTE:

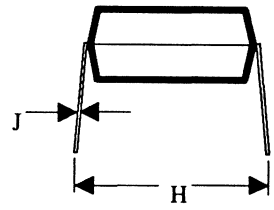
1. The phase relationship between XTAL OUT and RRCLK can be of either form.

DS2188
T1/CEPT JITTER ATTENUATOR
16-PIN DIP

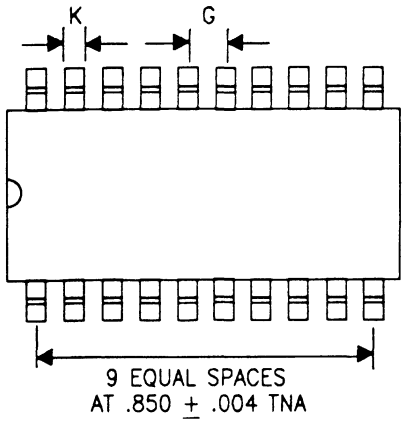
DIM.	INCHES	
	MIN.	MAX.
A	.740	.780
B	.240	.260
C	.120	.140
D	.290	.310
E	.020	.030
F	.110	.130
G	.090	.110
H	.320	.370
J	.008	.012
K	.015	.021



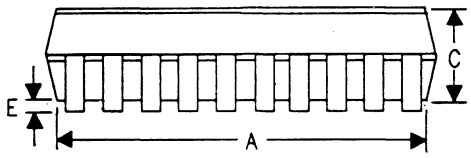


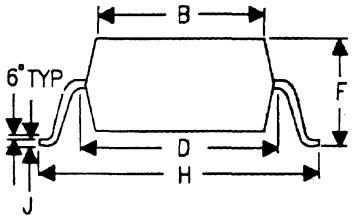


DS2188S
T1/CEPT JITTER ATTENUATOR
16-PIN SOIC



DIM.	INCHES	
	MIN.	MAX.
A	.503	.511
B	.290	.296
C	.089	.095
D	.325	.330
E	.008	.012
F	.097	.105
G	.046	.054
H	.402	.410
J	.006	.011
K	.013	.019





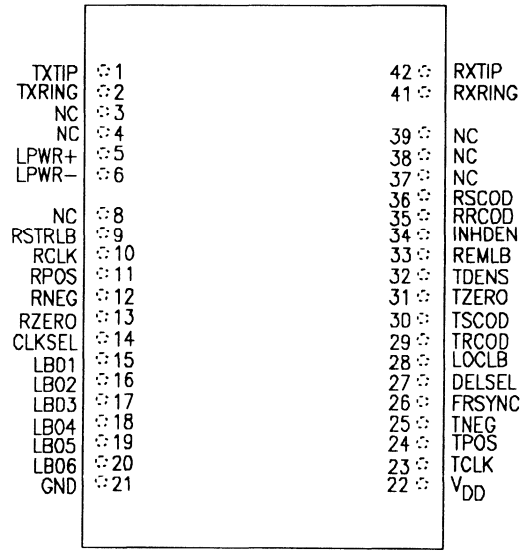
DALLAS SEMICONDUCTOR

DS2190-003
T1 NETWORK INTERFACE UNIT (NIU)

FEATURES

- Modularized network interface for 1.544 Mbps T1 services
- Network side connects directly to T1 line
- Compatible with DS2180A Transceiver
- Small size--approximately six square inches--permits integration onto line cards
- Compatible with ATT publication 62411
- FCC Part 68 and Part 15 pre-registration
- Extracts clock and data with no external components or tuning
- Detects and generates in-band loopback codes
- Assures proper ones density to network
- Powered by a local +5 volt supply

PIN CONNECTIONS



6

DESCRIPTION

The DS2190 is a small sealed module designed to meet the recommendations of ATT Publication 62411 for interfacing to T1 1.544 Mbps services (such as Accunet* T1.5, Skynet* T1.5 and High Capacity Digital Service). Because of the DS2190's FCC approval (Parts 68/15) and small footprint, T1 equipment makers can integrate an NIU into their products, reducing cost and increasing total system performance. Basic functions of the DS2190 are: clock and data recovery, isolation and surge protection, loopback detection and generation, and keep-alive signal generation. The DS2190 is compatible with D4 and ESF framing formats as well as B8ZS Clear Channel Coding. Also provided are alarm outputs for transmit and receive line status monitoring.

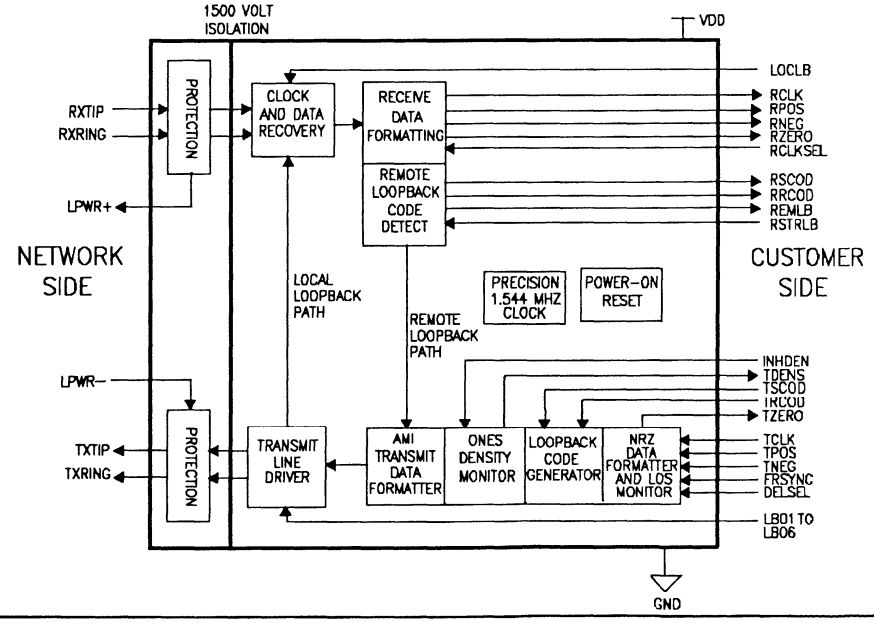
*Service marks of AT&T Communications

The DS2190 Network Interface Unit (NIU) is a self-contained module which provides direct access to the T1 network. The *network* side of the module connects directly to the twisted pair. The *customer* side is a digital interface to the communication system. The module is functionally organized into a *receive* section and a *transmit* section. In addition, the module contains an onboard precision timing reference for keep-alive and monitoring functions, and an integral reset circuit to ensure proper operation at power-on. The module is powered from a single +5.0 volt source. If line-powering is provided by the carrier, this may be accessed at module pins. Figure 1 is a block diagram of the NIU module.

The AMI signal received from the network is passed through a Clock and Data Recovery circuit to extract the timing information. This circuit contains an integral automatic line build out (ALBO) circuit to compensate for cable loss. The locally generated transmit signal can be looped back through this block to test the system equipment and the NIU module itself. The recovered clock and data are converted by the Receive Data Formatting circuit to a bipolar NRZ signal. This circuit also monitors the line for loss of signal. The formatted data is analyzed by the Remote Loopback Code Detect circuit for in-band maintenance loopback codes.

Data is fed to the transmit section as either a unipolar or a bipolar NRZ signal. The NRZ Data Formatter and LOS Monitor clocks in this data. It also generates a keep-alive signal in the event of an external clock failure. The Loopback Code Generator transmits in-band maintenance loopback codes to perform testing of the remote equipment and T1 span. The Ones Density Monitor ensures that the signal presented to the network meets the pulse density requirements. The AMI Transmit Data Formatter generates data pulses of the proper timing, which are transmitted onto the network by the Transmit Line Driver. Alternately, the received data will be transmitted back into the network if a remote loopback is enabled. The transmitted signal is also coupled back to the receive section for the local loopback.

DS2190 BLOCK DIAGRAM Figure 1



NETWORK-SIDE PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1 2	TXTIP TXRING	O	**TRANSMIT TIP AND RING OUTPUTS.** These are the transmit output connections to the T1 network. These outputs are transformer-coupled and reflect a source impedance of 100 ohms. Signal level and waveshaping are programmable through the strapping of the LBO.
41 42	RXTIP RXRING	I	**RECEIVE TIP AND RING INPUTS.** These are the receive input connections to the T1 network. These inputs are transformer-coupled and terminated at 100 ohms. Signals in the range of +0 to -30 dBSX can be applied here.
5 6	LPWR+ LPWR-	O	**LOOP POWER CONNECTIONS.** These pins connect to the internal center-taps of the transmit and receive transformers which provide access to the simplex DC power on the T1 line (if power is supplied by the carrier). These two pins should be tied together if the NIU is locally powered.

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CUSTOMER-SIDE PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DESCRIPTION
9	RSTRLB	I	**RESET REMOTE LOOPBACK STATE.** The remote loopback state is reset when this pin is pulsed high. If this pin is strapped high, the DS2190 will never enter the remote loopback state.
10	RCLK	O	**RECEIVE CLOCK.** Recovered 1.544 MHz clock from the network.
11 12	RPOS RNEG	O	**RECEIVE BIPOLAR DATA OUTPUTS.** Recovered digital data. Updates occur on rising edges of RCLK and are latched for the full clock period. Bipolar violations from the network are preserved.
13	RZERO	O	**RECEIVE ZEROS.** This pin transitions high when there has been an absence of signal for 32 consecutive bit times. RZERO will return low when a valid signal pulse is detected at RXTIP and RXRING.

14	CLKSEL	I	**CLOCK SELECT.** If this pin is tied high, the RCLK output will switch to an internal 1.544 MHz clock when RZERO goes high (indicating a loss of signal). RCLK will revert to the normal recovered clock when RZERO goes low. If CLKSEL is tied low, RCLK will go to a low logic state when RZERO goes high.
15 - 20	LBO1 to LBO6	-	**LINE BUILD OUT SELECT PINS.** Strapping these pins together determines the amount of attenuation for the transmit T1 signal. Refer to Table 3 later in this data sheet for proper settings.
21	GND	-	**SIGNAL GROUND.** 0.0 volts.
22	VDD	-	**POSITIVE SUPPLY.** 5.0 volts±5%. All module operations will cease if power is removed from this pin.
23	TCLK	I	**TRANSMIT CLOCK.** TPOS and TNEG inputs are sampled at the falling edge of this clock. TCLK also determines the TXTIP and TXRING pulse timings.
24 25	TPOS TNEG	I	**TRANSMIT BIPOLAR DATA INPUTS.** Data to be transmitted to the network.
26	FRSYNC	I	**FRAME SYNC INPUT.** 8 KHz clock which identifies F-bit positions in the TPOS and TNEG data stream. This clock is only used to preserve the F-bits when the transmit loopback code function is enabled.
27	DELSEL	I	**DELAY SELECT.** If this pin is strapped low, a rising edge on FRSYNC marks the beginning of the F-bit time on TPOS and TNEG. If this pin is strapped high, the rising edge of FRSYNC leads the F-bit by 10 bit times, which corresponds to the delay through a DS2180A.
28	LOCLB	I	**LOCAL LOOPBACK ENABLE.** The DS2190 enters the local loopback state when this pin is taken high, and the transmit signal is looped back to the receive clock and data recovery circuits. Meanwhile, TXTIP and TXRING will continue to operate normally.

29	TRCOD	I	**TRANSMIT RESET CODE.** When this pin is taken high, the in-band loopback reset code will be transmitted. This code consists of a repeating pattern of 001... that is overwritten by F-bit information.
30	TSCOD	I	**TRANSMIT SET CODE.** When this pin is taken high, the in-band loopback set code will be transmitted. This code consists of a repeating pattern of 00001... that is overwritten by F-bit information.
31	TZERO	O	**TRANSMIT ZEROS DETECT.** This pin will go high when the TCLK input has failed to transition for 150 ms. At this time, a keep-alive signal (AIS), consisting of a one in every bit position, will be transmitted to the network. The timing for this signal will come from an internal 1.544 MHz clock source.
32	TDENS	O	**TRANSMIT DENSITY VIOLATION.** A pulse will occur on this pin when a ones density violation has been detected in the transmit data.
33	REMLB	O	**REMOTE LOOPBACK DETECT.** This pin will transition high when the remote loopback state has been entered. It will return low when the DS2190 returns to normal operation. Remote loopback is entered by receipt of the in-band loopback set code for at least 4.75 seconds. It is terminated by either receipt of the in-band loopback reset code or the RSTRLB pin.
34	INHDEN	I	**INHIBIT DENSITY MONITOR.** If this pin is tied high, the DS2190 will not alter the transmit data to correct ones density violations. This pin should be strapped low to ensure that the ones density criteria is met unless the DS2190 is being used in a private network where this requirement does not apply.
35	RRCOD	O	**RECEIVE LOOPBACK RESET CODE.** This pin transitions high when the inband loopback reset code (a repeating "001" pattern) is being received and will stay high as long as a valid reset code continues to be received.
36	RSCOD	O	**RECEIVE LOOPBACK SET CODE.** This pin transitions high when the inband loopback set code (a repeating "00001" pattern) is being received and will stay high as long as a valid set code continues to be received.

NOTE: Do not connect to pins 3, 4, 8, 37, 38, and 39.

INTRODUCTION

In order to connect telecommunications equipment to a public T1 network, certain specifications must be met in the interface circuitry. The FCC has issued publication Part 68 for addressing concerns over network harm, whether it be the public switched telepone network or, in this case, the T1 network. Part 68 is also concerned about functionality of the interface circuit when exposed to a potential hazard such as lightning. The FCC has issued Part 15 in order to specify limits for EMI. However, for issues of performance, an accepted recommendation is AT&T Communications' Technical Reference 62411 (Dec 1988), hereafter noted as PUB 62411. This document addresses such issues as loopback, framing format, keep-alive signal, jitter and output pulse shaping. Compliance to these recommendations helps to ensure uniformity of performance when connecting to AT&T or any other T1 carrier.

The DS2190 Network Interface Unit (NIU) is preregistered with the FCC as an approved T1 network interface under Parts 68 and 15. What this means to a user is that with very little design effort an FCC-approved interface on a T1 line card can be implemented. The NIU is also functionally compatible with the relevant sections of PUB 62411. By adding a DS2180A T1 Transceiver and DS2176 Receive Buffer, a complete T1 line card can be designed, connecting an equipment backplane to a T1 carrier. An example of such an implementation is shown in Figure 4.

ISOLATION

One of the primary functions of the DS2190 is to provide galvanic isolation between the network and the customer premise equipment (CPE). The network-side pins (1,2,5,6,41, and 42) have at least 1500 volts DC isolation from all customer-side pins. In order to maintain this isolation, all PCB traces to the network-side pins should be at least 200 mils away from any normal board trace (i.e, logic or system traces). The network-side traces should be at least 20 mils wide and should be as short as possible. Typically, for a T1 line card application, the DS2190 should be very close to the physical T1 connector (RJ48C or similar connector). If the T1 connector is not on the same PCB as the DS2190, then locate the DS2190 near the network connection leads at the backplane inputs.

POWERING

The functions performed by the DS2190 are critical to the operation of the T1 network. If power is removed from the NIU, it will cease to produce a T1 signal and oscillation in the line repeaters could occur. For this reason, the NIU's VDD pin should be connected to a non-interruptible power source. There are two methods for providing this non-interruptible power source: line powering and local powering.

In many cases the T1 carrier provides a simplex DC current for line powering. Access to this power source is available at the NIU's LPWR+ and LPWR- pins. Because the DC power source on a typical T1 line is current-limited to 60 mA, a switching DC-DC converter will be necessary to be able to power the DS2190. For FCC approval, this converter must meet all provisions of Part 68 for isolation and Part 15 for EMI. Contact the Telecom marketing group for assistance in such an application.

In new applications, the FCC permits local powering of the NIU. This local power should be battery backed in the event of a CPE power failure so that the DS2190 can still function. When local powering is used, the LPWR+ and LPWR- leads should be tied together to permit pass-through of the DC power loop.

Exercise extreme caution with these pins since voltages in the range of +130 to -130 volts could exist here.

RECEIVE DATA PROCESSING

Receive signals from the T1 network are coupled to the DS2190 by connecting RXTIP and RXRING to the T1 receive pair. Signals in the range of +0 dBSX to -30 dBSX can be applied here (typically, a carrier will limit signals to a range much less than this). The receive interface includes clock and data extraction with an integral ALBO (automatic line build out) circuit which adjusts for loop length of up to 6000 feet of 22-gauge ABAM cable. The extracted clock and data are formatted and presented at the RCLK, RPOS, and RNEG pins. The RCLK will be nominally 1.544 MHz at a 50% duty cycle. RPOS and RNEG are the recovered bipolar data in a non-return format (i.e., valid for an entire RCLK cycle) and can be sampled on the falling edge of RCLK.

The network timing is conveyed in the received data pulses, and long strings of zeros will cause timing synchronization to be lost. When the DS2190 detects 32 consecutive zeros at RXTIP and RXRING, it brings the RZERO pin high. If the CLKSEL pin is strapped low, the RCLK output will go low at this time. If the CLKSEL pin is strapped high, RCLK will be switched to an onboard 1.544 MHz timing reference. As soon as a data pulse is detected at either the RXTIP or RXRING input, the RZERO pin will return low and RCLK will return to the extracted clock signal.

REMOTE LOOPBACK CODE PROCESSING

The DS2190 recognizes the in-band codes which control remote loopbacks at the DS-1 level. The code to enter (set) the remote loopback state is a repeating "00001" pattern. The code to leave (reset) the remote loopback state is a repeating "001" pattern. These codes can be either framed or unframed. After receipt of a valid set code for approximately 4.75 seconds, the DS2190 enters a loopback condition. The REMLB output will transition high, and the received data will be transmitted as-is through TXTIP and TXRING. The received data will continue to appear at RPOS and RNEG as normal. While in loopback, the data at TPOS and TNEG will be ignored. Once in the remote loopback state, the set code from the network need not be sustained.

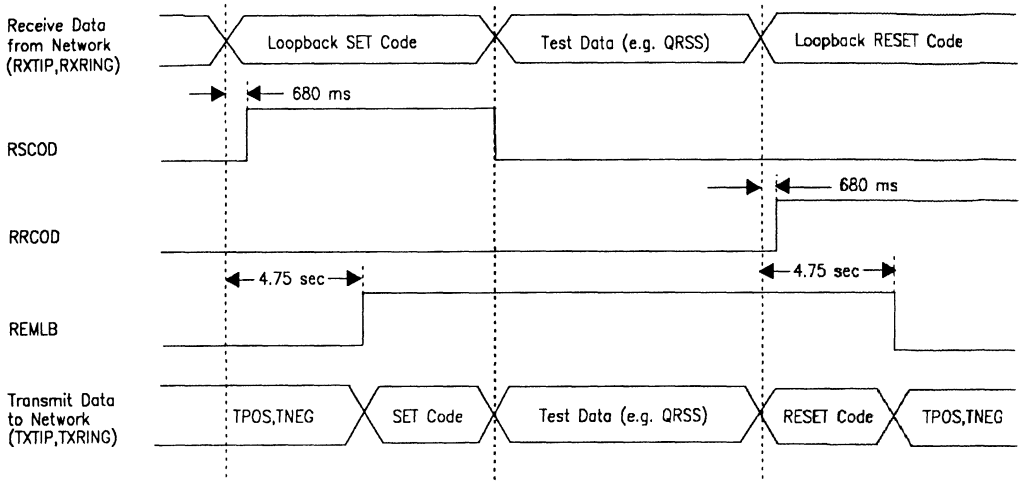
After receipt of a valid reset code for approximately 4.75 seconds, the DS2190 will return to normal operation. The REMLB output will return low and the information at TPOS and TNEG will be processed as normal.

The remote loopback sequence may be monitored at the RSCOD and RRCOD pins. They indicate reception of a valid set and reset code, respectively. These pins transition high when a valid code has been received for approximately 680 ms and remain high as long as a valid code is detected. This is illustrated in Figure 2A.

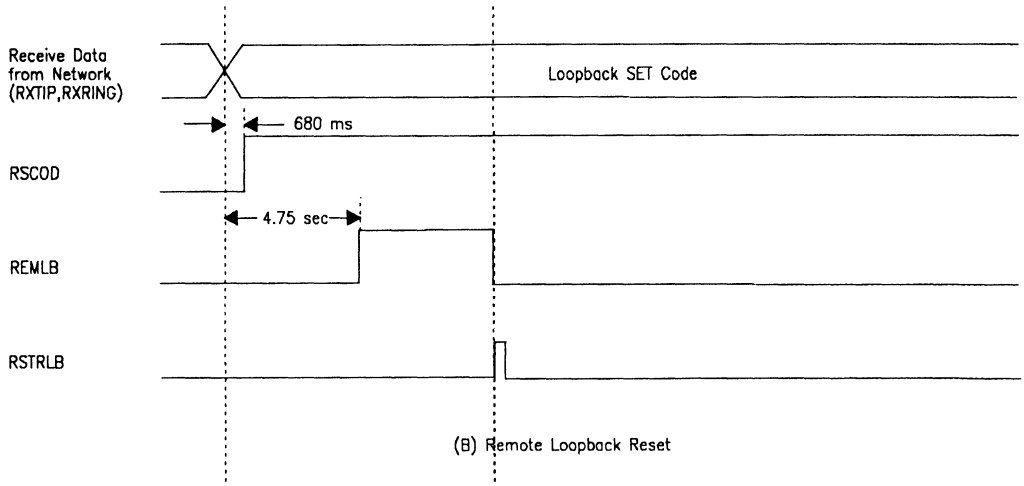
The RSTRLB pin resets the remote loopback state. If this pin is strapped high, the DS2190 will never enter the remote loopback state. If this pin is pulsed high while the DS2190 is in the remote loopback state, it will return to normal operation. If RSTRLB is activated while the DS2190 is in a remote loopback state and a valid set code is still being received, the current set code sequence will not trigger the remote loopback state again. The RSCOD and RRCOD pins are not affected by the RSTRLB pin. This is illustrated in Figure 2B.

Loopbacks are used to isolate network problems. To aid in this diagnosis, the DS2190's loopback code detectors are tolerant to abnormally high error rates, even up to a 10^{-2} bit error rate.

REMOTE LOOPBACK PROCESSING Figure 2



(A) Remote Loopback Code Handling



(B) Remote Loopback Reset

TRANSMIT TIMING REQUIREMENTS

Data to be transmitted into the network is presented at the TPOS and TNEG inputs. Normally this input data is in a bipolar, NRZ-coded format. Although the DS2190 allows these two inputs to be connected together and driven with unipolar data, the bipolar configuration is preferred. Timing for this data is provided at the TCLK input. The transmit signal to the T1 network will appear at TXTIP and TXRING. The timing integrity of this signal is totally dependent on TCLK. To meet FCC Part 68 requirements and PUB 62411 recommendations, the TCLK source must have a frequency of 1.544 MHz±64Hz (±48ppm). The emerging ANSI specification will probably require an accuracy of ±50Hz (about ±32ppm) for new equipment. Therefore, it is recommended that the TCLK clock source be accurate to at least ±50Hz to

meet all existing and proposed standards.

The duty-cycle of the TCLK input is also very important since a T1 pulse is nominally 324 nsec in width (half the 1.544 MHz). A duty cycle of 50% ±1% is required to meet the network pulse template requirements. The DS2190 will perform all necessary wave-shaping to conform to these specifications given that the duty-cycle requirements are met. The output pulse characteristics will meet the specifications in Section 5.4.4 and Figure 2.4 of PUB 62411.

Another important requirement of the TCLK source is that it be relatively jitter-free. PUB 62411 recommends a maximum of 0.05 unit-intervals peak-to-peak (UIpp) measured without bandlimiting. This document describes other jitter limits measured in specific frequency bands. For full compliance to AT&T recommendations on output jitter, please see this publication. Jitter specifications are undergoing study by several organizations and these requirements may change in the future. However, a TCLK input with less than 0.05 UIpp of total jitter should meet existing and proposed recommendations from a T1 network interface.

TRANSMIT LOSS OF SIGNAL

If the DS2190 detects no transitions at the TCLK input for 150 msec, a loss of signal (LOS) condition will be declared and the DS2190 will transmit a blue alarm to the network. This alarm is also known as an Alarm Indication Signal (AIS) and consists of an unframed all ones pattern. The timing for the AIS is based on the internal reference clock. The TZERO output will transition high to indicate that the DS2190 has declared a LOS condition.

The DS2190 recognizes the loss of TCLK signal within approximately 5 µsec (8 clock intervals) and switches transmit timing control from the TCLK input to the internal reference. This guarantees that between this time and the declaration of a LOS condition, the DS2190 will still generate a signal which meets the network ones density requirements. As soon as a rising edge and a falling edge are detected at TCLK, the DS2190 returns to normal operation.

REMOTE LOOPBACK CODE TRANSMISSION

The DS2190 can transmit the codes to place the remote data terminal equipment (DTE) into a loopback state. This feature is controlled with the TRCOD and TSCOD pins. Please refer to the Remote Loopback Code Processing section for information on these codes.

The remote loopback codes are framed, in-band patterns. The FRSYNC input indicates the position of the framing bit at the TPOS and TNEG inputs. This bit overwrites the loopback code in the transmitted data. When the DELSEL pin is strapped low, the frame bit occurs at the bit position of the FRSYNC pulse. When DELSEL is strapped high, the frame bit occurs 10 bit positions later than the FRSYNC pulse, which corresponds to the delay through a DS2180A. If FRSYNC is strapped high or low, an unframed loopback pattern will be produced, regardless of the DELSEL strapping.

The DS2190 is fully transparent to B8ZS encoding; all data (including bipolar violations) are passed to the network as presented at TPOS and TNEG. When the DS2190 is transmitting a remote loopback code, a frame bit which has been altered from a zero to a one by an external B8ZS encoder will be received as a one by the remote equipment. This is because the remainder of the B8ZS code word is overwritten by the loopback code. To maintain framing at the remote equipment, B8ZS encoding should be inhibited while TRCOD or TSCOD are active. Note, however, that the DS2190 is able to recognize loopback codes even in the presence of framing errors.

TRANSMIT PULSE DENSITY

The term "pulse density" (also called "ones density") refers to the number of ones present in the T1 signal. With bipolar signals, a pulse is only present when a one is to be transmitted; a zero is represented by the absence of a pulse. Therefore, when a long string of zeros is to be transmitted in a bipolar fashion, there is no signal present on the line during this time. This can lead to excessive jitter or even failure in the repeater clock recovery circuits if these strings of zeros are not controlled in length and in density. The DS2190 ensures that its outgoing transmit signal (present at TXTIP and TXRING) meets the pulse density recommendations in PUB 62411, which are as follows:

1) no more than 15 zeros in a row, and
2) at least N ones in every time window of 8(N+1), where $1 \leq N \leq 23$.

The DS2190 will monitor the data at TPOS and TNEG to ensure that these requirements are met. If the DS2190 detects a pulse density violation, it will signal this condition by a one-bit period pulse on the TDENS output. If the INHDEN pin is strapped low, a one will be inserted into the transmitted data to ensure the pulse density conditions are met. If the INHDEN pin is strapped high, the data will not be altered.

Note that a signal with Bit 7 zero-supression or B8ZS coding will always meet these requirements, and therefore will not be altered by the DS2190. However, in the event of TCLK loss, INHDEN must be low to guarantee that the ones density criteria is met during the interval from TCLK loss to the declaration of a transmit LOS condition.

TRANSMIT LBO SELECTION

Line build out (LBO) is the process of inserting into the transmit path a circuit which simulates the characteristics of a certain length of wire. The DS2190 contains three LBO circuits which provide 0dB, 7.5dB, or 15dB of attenuation at 772 KHz (the center of the signal spectrum), which cover cable lengths from 0 to 6000 feet. The characteristics of these circuits conform to FCC Part 68 recommendations. In most applications, LBO selection is determined at the time of installation of the CPE by a telephone craftsman. It is recommended that a mechanical switch be installed on the board that is easily accessible and clearly marked to indicate the proper settings. The switch should strap the appropriate LBO pins together for the corresponding cable loss as shown in Table 3.

INSTALLATION INSTRUCTIONS FOR THE DS2190

In order to comply fully with FCC Part 68, the following specifications must met when installing the DS2190 into a piece of equipment:

1. Mounting of the DS2190 on the final unit must be made so that the unit is isolated from exposure to any hazardous voltages within the assembly. Adequate separation and restraint of cables and cords must be provided.

2. The circuitry from the DS2190 to the telephone line may not be routed in the same cable or conductor harness as leads to either power sources, other than non-hazardous power sources, or leads to non-FCC registered equipment.

3. A label should be visable from the outside of the final assembly listing the following information:

FCC Registration Number: GIDUSA-60872-DE-N

This is in addition to the label on the DS2190 itself. Labels are available upon request from Dallas Semiconductor.

4. The FCC-required information, which is outlined in a Dallas Semiconductor document titled "FCC Information for Final Users of the DS2190," is to be provided to the user of the final assembly.

5. The instructions contained in the DS2190 data sheet concerning the use of the simplexed power leads (LPWR+ and LPWR-), the line build out (LBO1 to LBO6) leads, and the precautions for printed circuit board layout for maintaining isolation should be carefully followed.

FCC INFORMATION FOR FINAL USERS OF THE DS2190

Note to manufacturers: As required by FCC Rules and Regulations, the following information must be suplied to users of the final assemblies which contain the DS2190. Although this exact format is not required, the main points of information must be covered. If registration of the final assembly is obtained under Part 68 of the FCC Rules, then the information listed under "Service Other Code" may no longer be appropriate, and the SOC of 6.0N may need to be listed as 6.0F.

General Instructions Regarding the Use of Customer-Provided Telephone Equipment

FCC regulations and telephone company procedures prohibit connection of customer-provided equipment to telephone company-provided equipment coin service (central office implemented systems). Connection to party lines service is subject to State Tariffs.

The goal of the telephone company is to provide you with the best service it can. In order to do this, it may occasionally be necessary for them to make changes in their equipment, operations, or procedures. If these changes might affect your service or the operation of your equipment, the telephone company will give you notice, in writing, to allow you to make any changes necessary to maintain uninterrupted service.

If you have any questions about your telephone line, such as how many pieces of equipment you can connect to it, the telephone company will provide this information upon request.

In certain circumstances, it may be necessary for the telephone company to request information from you concerning the equipment which you have connected to your telephone line. Upon request of the telephone company, provide the FCC registration number and the ringer equivalence number (REN) of the equipment which is connected to your line; both of these items are typically listed on the equipment label. The sum of all of the REN's on your telephone line should be less than five in order to assure proper service from the telephone company. In some cases, a sum of five may not be usable on a given line.

FCC and Telephone Company Procedures and Requirements

In order to connect to the network, the local operating company must be provided with the registration number of this equipment and the proper connections must be ordered.

To order the proper service, provide the telephone company with:

- the USOC number of the required jack (see the Table below)
- the facility interface code
- the service code

Type of Interface	USOC Jack Connector Code	Service Code	Facility Interface
1.544Mbps digital interface with D4 framing format	RJ48C	6.0N	04DU9-B
1.544Mbps digital interface with ESF framing format	RJ48C	6.0N	04DU9-C

If Problems Arise

If any of your telephone equipment is not operating properly, you should immediately remove it from your telephone line, as it may cause harm to the telephone network. If the telephone company notes a problem, they may temporarily discontinue service. When practical, they notify you in advance of this disconnection. If advance notice is not feasible, you will be notified as soon as possible. When you are notified, you will be given the opportunity to correct the problem and informed of your right to file a complaint with the FCC.

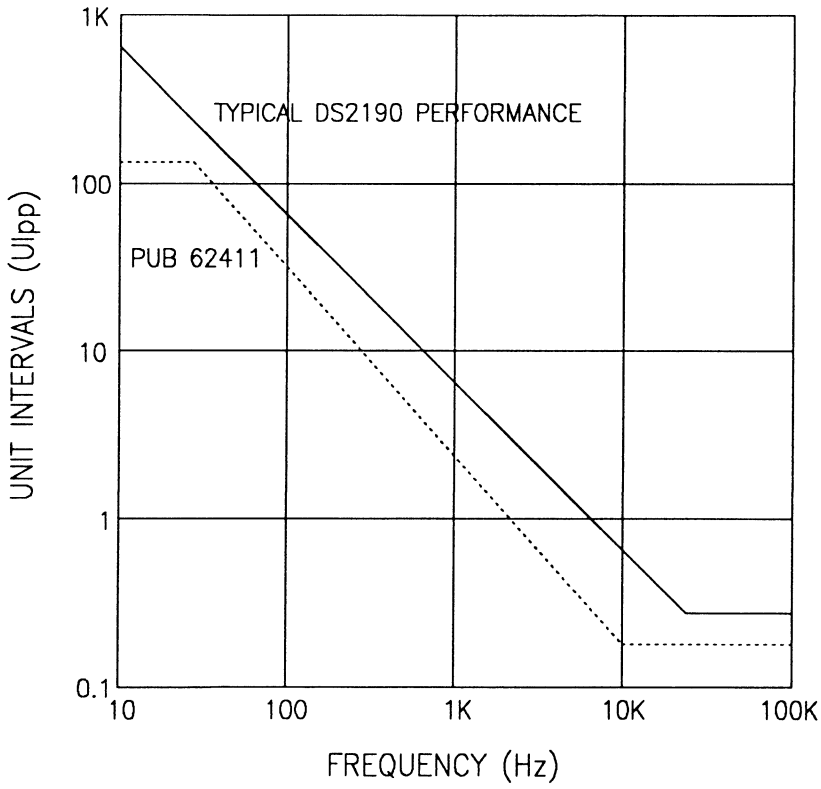
In the event repairs are ever needed on this equipment, they should be performed by (name of the final assembler) or an authorized representative of (name of the final assembler). For information contact:

(name and address of the final assembler)

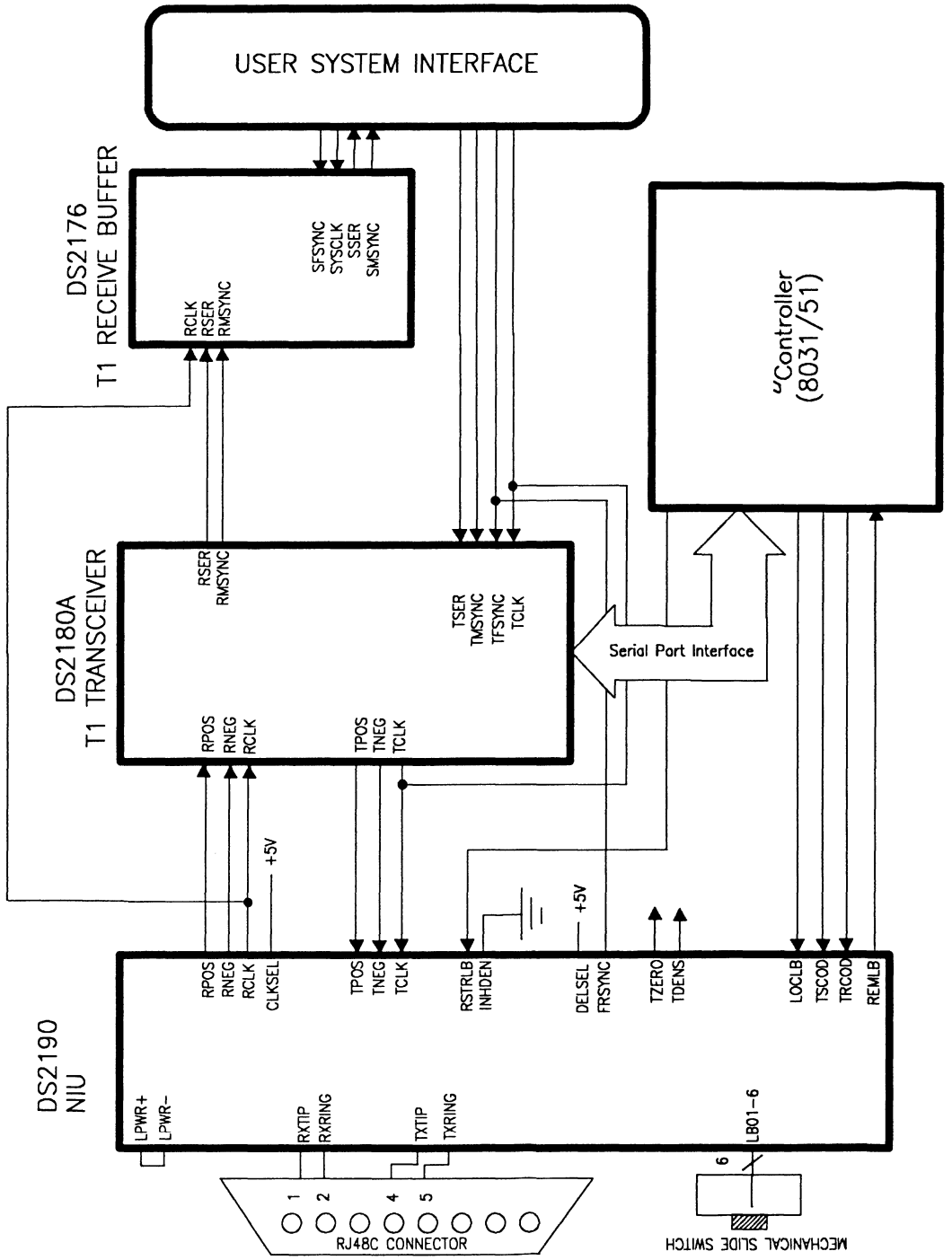
LBO Strapping Chart Table 3

For equivalent loss at 772 KHz,	strap these inputs together.
0.0dB	LB01 to LB06
7.5dB	LB01 to LB02 LB05 to LB06
15.0dB	LB01 to LB02 LB03 to LB05 LB04 to LB06

DS2190 JITTER TOLERANCE Figure 3



TYPICAL T1 LINE CARD APPLICATION Figure 4



ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON ANY PIN RELATIVE TO GROUND (CUSTOMER SIDE)	-0.3V to +7V
OPERATING TEMPERATURE	0° C to 70°C
STORAGE TEMPERATURE	-25°C to +85°C
SOLDERING TEMPERATURE	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{DD} = +5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power supply voltage	VDD	4.75	5.0	5.25	V	
Power supply current	I_{DD}		75	110	mA	2,3
Input logic 1 voltage	V_{IH}	2.0		VDD+.3	V	1
Input logic 0 voltage	V_{IL}	-0.3		0.8	V	1
Output high voltage @I_{OH}=-1mA	V_{OH}	2.4			V	1
Output low voltage @I_{OL}=4 mA	V_{OL}			0.4	V	1
Input leakage current $0V \leq V_{IN} \leq V_{DD}$	I_{IL}		0.1	10	uA	1

NOTES:

1. DC characteristics apply to all customer side pins except LB01 to LB06.
2. $I_{DD, MAX}$ specified driving all ones into 6000 ft. of 22 AWG cable (worst case).
3. $I_{DD, TYP}$ specified driving 50% ones into 6000 ft. of 22 AWG cable.

AC DIGITAL CHARACTERISTICS - TRANSMIT (T_A=0°C to 70°C; V_{DD} = +5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Transmit Data Setup	t_{TDS}	50			ns	
Transmit Data Hold	t_{TDH}	50			ns	
Frame Sync Setup	t_{FSS}	-125		+125	ns	
Frame Sync Width	t_{FSW}	100			ns	
Output Delay	t_{TOD}			75	ns	
Transmit Clock Frequency	$1/t_{TCW}$	-50ppm	1.544	+50ppm	MHz	1
Transmit Clock High Time	t_{TCH}	-1%	324	+1%	ns	1
Transmit Clock Rise Time	t_{TCR}			10	ns	
Transmit Clock Fall Time	t_{TCF}			10	ns	

NOTES:

1. Required to meet PUB 62411 and FCC Part 68 specifications.
2. Measurements made at 1.5V.
3. Measured with100 pF output load unless otherwise specified.

AC DIGITAL CHARACTERISTICS - RECEIVE (T_A=0°C to 70°C; V_{DD} = +5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Receive Data Delay	t_{RDD}	-50		+50	ns	
Output Delay	t_{ROD}			100	ns	
Receive Clock Frequency	$1/t_{RCW}$		1.544		MHz	
Receive Clock High Time	t_{RCH}	314	324	334	ns	
Receive Clock Low Time	t_{RCL}	314	324	334	ns	
Receive Clock Rise Time	t_{RCR}			20	ns	
Receive Clock Fall Time	t_{RCF}			20	ns	

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AC DIGITAL CHARACTERISTICS - REMOTE LOOPBACK

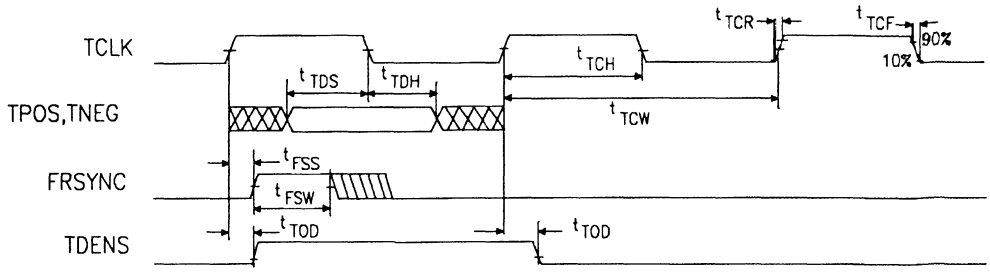
(T_A = 0°C to 70°C, V_{DD} =5V+5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Code Valid Recognition	t_{RLBCV}	650	680	710	ms	
Code Invalid Recognition	t_{RLBCX}			200	ms	
Remote Loopback State Change	t_{RLB}	4600	4750	4900	ms	1
Remote Loopback Reset Delay	t_{RLBRD}			100	ns	
Remote Loopback Reset Pulse Width	t_{RLBPW}	100			ns	

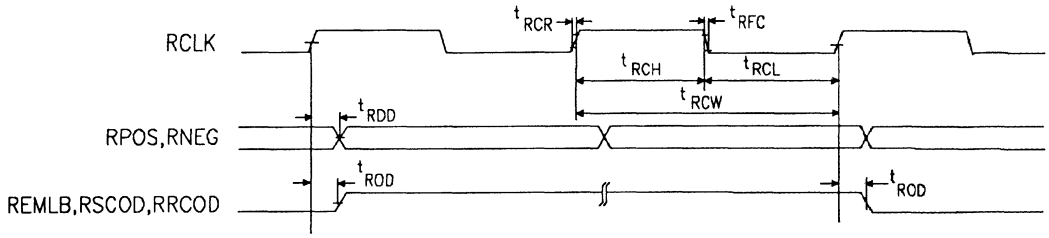
NOTES:

1. With REMLB low.
2. Measurements made at 1.5V.
3. Measured with 100pF output load.

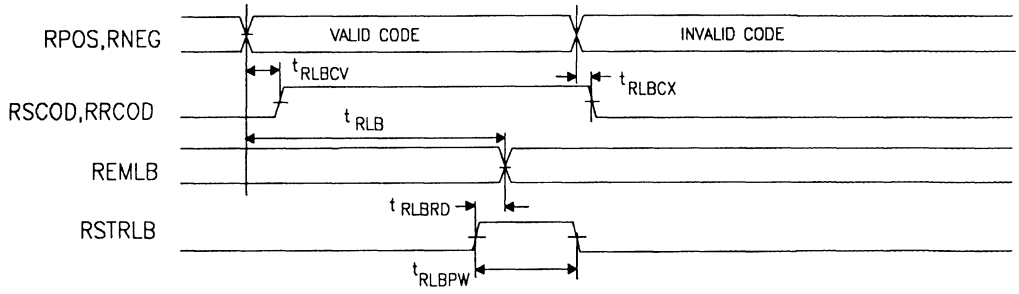
TRANSMIT AC TIMING DIAGRAM Figure 10



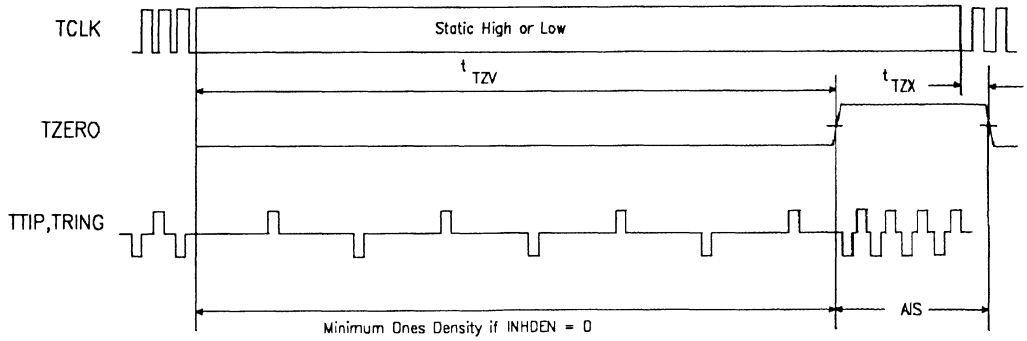
RECEIVE AC TIMING DIAGRAM Figure 11



REMOTE LOOPBACK AC.TIMING DIAGRAM Figure 12



TZERO AC TIMING DIAGRAM Figure 13



AC DIGITAL CHARACTERISTICS - TZERO

(t_A = 0°C to 70°C, V_{DD} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TZERO Valid Delay	t_{TZV}	140	150	160	ms	1
TZERO Invalid Delay	t_{TZX}			4	us	

NOTE:

1. Transmit waveform will meet pulse density requirements if INHDEN is strapped low.

NETWORK INTERFACE CHARACTERISTICS

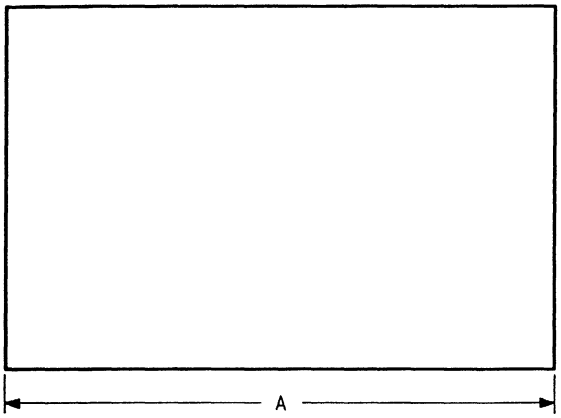
(t_A = 0°C to 70°C, V_{DD} = +5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
A.C. receive, transmit impedance	Z_R, Z_T		100		ohms	
Receive input signal range	V_{IR}	-30		+0	dBSX	1
RCLK output jitter generation	RxJ_0			0.25	Ulpp	2
Longitudinal balance	LBAL	35			dB	
Transmit ones density (over 192 bits)	TXDENS	12			%	3
Transmit signal level (TXTIP,TXRING)	TXLVL		0		dBSX	4,5
Transmit keep-alive frequency tolerance (about 1.544 MHz)	TXFTOL	-35		+35	ppm	

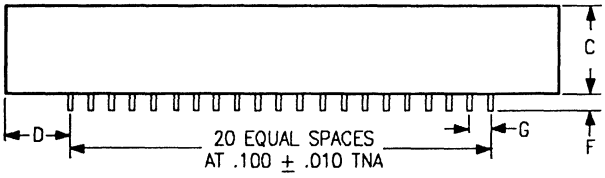
NOTES:

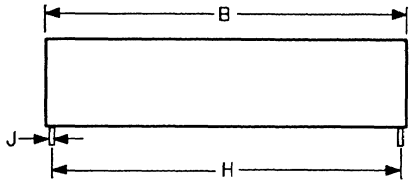
1. 0 dBSX = 3V peak.
2. RXTIP and RXRING are connected to a QRSS signal with no jitter present.
3. The ones density of the outgoing transmit signal complies with section 5.5.1 of PUB # 62411. For every time window of 8 X (n + 1) bits-where n can equal 1 through 23-there will be at least "n" ones present. Also there will be no more that 15 zeros in a row. The DS2190 will ensure that input data at TPOS and TNEG meet these requirements by inserting ones at the violation times (only if INHDEN is low).
4. 0 dB of LBO selected.
5. Transmit level is directly proportional to V_{DD}.

T1 NETWORK INTERFACE UNIT (NIU)
DS2190-003



INCHES		
DIM.	MIN	MAX
A	3.170	3.190
B	2.070	2.090
C	0.565	0.585
D	0.570	0.590
F	0.135	0.165
G	0.090	0.110
H	1.790	1.810
J	0.016	0.020





NOTE: Pins 7 and 40 missing by design.

SIP STIKS

7

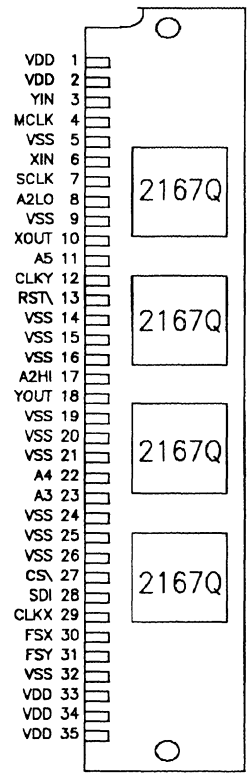
DALLAS SEMICONDUCTOR

DS2264
DS2268
ADPCM Stik™

FEATURES

- Provides four channels (DS2264) or eight channels (DS2268) of parallel full-duplex ADPCM processing in a pre-fabricated, snap-in module
- Based on the DS2167Q ADPCM Processor which implements the T1.301 and CCITT G.721 recommendations
- Occupies only 2 square inches of board space
- Conforms to popular JEDEC standard 35 position Single In-Line connector
- Easily cascadable up to 64 full-duplex channels in multiples of four or eight
- Both A-law and U-law compatible
- Utilizes serial interface port for microprocessor control of time slot assignments
- Includes onboard buffers for all critical signals

PIN DESCRIPTION

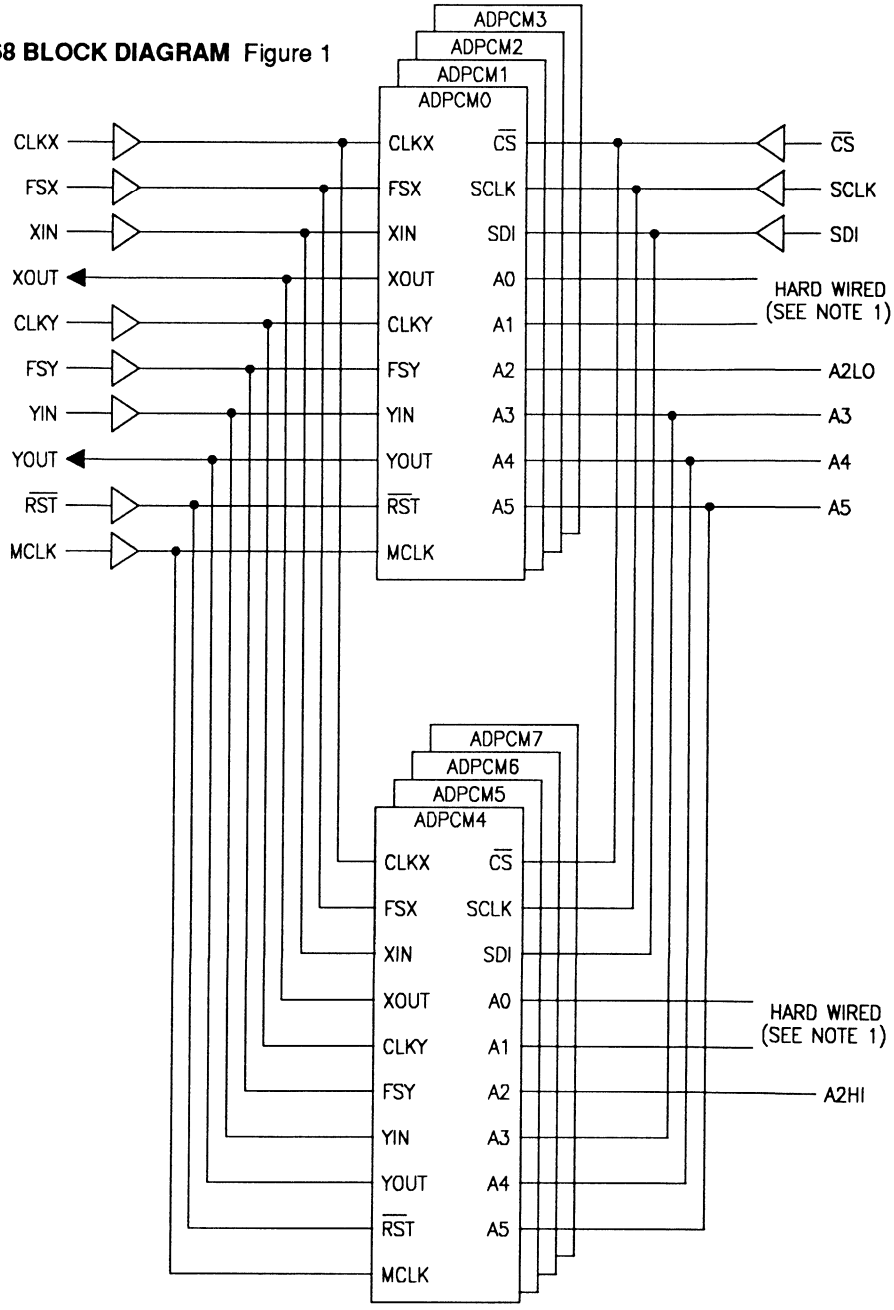


(actual size)

DESCRIPTION

The DS2264 and DS2268 are complete, pre-fabricated cards that perform either four or eight channels of full-duplex ADPCM processing. The ADPCM algorithm compresses 64Kbps voice data to 32Kbps. The DS2264 is only populated on one side and offers four channels while the DS2268 is populated on both sides of the Stik and offers eight channels. Control of the Stiks is handled by an external microcontroller via a serial port. Both Stiks are based on the DS2167Q ADPCM Processor. Specific details on the DS2167Q can be found in the DS2167 data sheet.

DS2264/DS2268 BLOCK DIAGRAM Figure 1



7

NOTES:

1. Pins A0 and A1 are configured as follows:

Processor	A1	A0
0 and 4	0	0
1 and 5	0	1
2 and 6	1	0
3 and 7	1	1

2. For the DS2264, processors 4 to 7 are not included and signal A2HI should be left open.

PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1 2	VDD	-	**Positive Supply.** 5.0 Volts
3	YIN	I	**Y Data In.** Sampled on falling edge of CLKY during selected time slots.
4	MCLK	I	**Master Clock.** 10 MHz clock for the ADPCM processing engine; may be asynchronous to SCLK, CLKX, and CLKY.
5	VSS	-	**Signal Ground.** 0.0 volts.
6	XIN	I	**X Data In.** Sampled on falling edge of CLKX during selected time slots.
7	SCLK	I	**Serial Data Clock.** Used to write to the serial port.
8	A2LO	I	**Address Bit 2.** Defines address selection for the lower four channels. May be tied either high or low on the DS2264. Must be tied low on the DS2268.
9	VSS	-	**Signal Ground.** 0.0 volts.
10	XOUT	O	**X Data Output.** Updated on rising edge of CLKX during selected time slots.
11	A5	I	**Address Bit 5.** Defines value for address bit 5.
12	CLKY	I	**Y Data Clock.** Data clock for the Y side PCM interface; must be synchronous with FSY.
13	RST\		**Reset.** Active low. A high-low-high transition clears all internal registers, resets the algorithms, and idles the outputs of all the channels.

14 15 16	VSS	-	**Signal Ground.** 0.0 volts.
17	A2HI	I	**Address Bit 2.** Defines address selection for upper four channels. Must be left open on the DS2264 and tied high on the DS2268.
18	YOUT	O	**Y Data Output.** Updated on rising edge of CLKY during selected time slots.
19 20 21	VSS	-	**Signal Ground.** 0.0 volts.
22	A4	I	**Address Bit 4.** Defines value for address bit 4.
23	A3	I	**Address Bit 3.** Defines value for address bit 3.
24 25 26	VSS	-	**Signal Ground.** 0.0 volts.
27	CS\	I	**Chip Select.** Active low. Serial port select; must be low to write to the serial port.
28	SDI	I	**Serial Data In.** Data for onboard control registers; sampled on the rising edge of SCLK. LSB sent first.
29	CLKX	I	**X Data Clock.** Data clock for the X side PCM interface; must be synchronous with FSX.
30	FSX	I	**X Frame Sync.** 8 KHz frame sync for the X side PCM interface.
31	FSY	I	**Y Frame Sync.** 8 KHz frame sync for the Y side PCM interface.
32	VSS	-	**Signal Ground.** 0.0 volts.
33 34 35	VDD	-	**Positive Supply.** 5.0 volts.

SYSTEM INTERFACE AND CONTROL

Both the DS2264 and DS2268 are designed to operate with an external microcontroller such as a DS5000 or an 8051/31. The microcontroller communicates to the APDCM Stiks over a three-wire serial port consisting of CS\, SCLK, and SDI. Data that is written to serial port can be either two or four bytes long. A four-byte write consists of the Address/Command byte, the Control byte, the Input Time Slot byte, and the Output Time Slot byte. A two-byte write only contains the Address/Command byte and the Control byte. Within the Address/Command byte, there is an address field. Each ADPCM processor on the Stik monitors the serial port and looks for a match between its address (set by the configuration of the A0 to A5 pins) and the address specified in the Address/Command byte. If a match occurs, then either the next one or three bytes are accepted as configuration data. Complete details on the operation of the serial port can be found in the DS2167 data sheet. Details on the four configuration registers are shown in Figures 2 through 5.

ADDRESS/COMMAND BYTE Figure 2

(MSB)							(LSB)
-	X/Y	A5	A4	A3	A2	A1	A0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	ACB.7	Reserved; must be zero for proper operation
X/Y	ACB.6	X/Y Channel Select. 0 = update channel Y characteristics 1 = update channel X characteristics
A5	ACB.5	MSB of Device Address
A4	ACB.4	
A3	ACB.3	
A2	ACB.2	
A1	ACB.1	
A0	ACB.0	LSB of Device Address

CONTROL REGISTER Figure 3

(MSB)							(LSB)
-	-	IPD	ALRST	BYP	U/A	-	CP/EX

SYMBOL	POSITION	NAME AND DESCRIPTION
-	CR.7	Reserved; must be zero for proper operation.
-	CR.6	Reserved; must be zero for proper operation.
IPD	CR.5	Idle and Power Down. 0 = channel enabled 1 = channel disabled (output 3-stated)
ALRST	CR.4	Algorithm Reset. 0 = normal operation 1 = reset algorithm for selected channel
BYP	CR.3	Bypass. 0 = normal operation 1 = bypass selected channel
U/A	CR.2	Data Format. 0 = A - law 1 = U - law
-	CR.1	Reserved; must be zero for proper operation.
CP/EX	CR.0	Channel Coding. 0 = expand (decode) selected channel 1 = compress (encode) selected channel

INPUT TIME SLOT REGISTER Figure 4

(MSB)							(LSB)
-	-	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	ITR.7	Reserved; must be zero for proper operation.
-	ITR.6	Reserved; must be zero for proper operation.
D5	ITR.5	MSB of input time slot register.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input time slot register.

OUTPUT TIME SLOT REGISTER Figure 5

(MSB)							(LSB)
-	-	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	OTR.7	Reserved; must be zero for proper operation.
-	OTR.6	Reserved; must be zero for proper operation.
D5	OTR.5	MSB of output time slot register.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output time slot register.

DATA BUSSING

The DS2264 and DS2268 can be cascaded to process up to 64 full-duplex ADPCM channels. For example, eight DS2268s can be combined in parallel to achieve 64 channels. All of the common PCM interface signals (CLKX, FSX, XIN, XOUT, CLKY, FSY, YIN, YOUT) should be tied together. Also, the serial interface signals (SCLK, CS\, SDI) should be tied together. Every processor will be assigned a unique address via the A0 to A5 pins on the processor. Address pins A0 and A1 are already assigned for each ADPCM processor, the user selects A2 through A5. The address range for the processors on a single module is defined by the strapping of the A5, A4, A3, A2LO, and A2HI address control pins.

Each DS2264 occupies four consecutive address locations. The exact placement of this four-address block is defined by the user via the address control pins. (See Table 2.) On the DS2264, the A2HI pin should be left open. Each DS2268 occupies eight consecutive address locations. (See Table 3.) On the DS2268, the A2HI pin should be tied to VDD and the A2LO pin should be tied to VSS. If the address control pins are tied so that each module in the stack has a unique range of addresses, then an external microcontroller will be able to select any processor in the group and configure it appropriately.

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DS2264 ADDRESS STRAPPING Table 2

			Four Block Address Selected	
A5	**A4**	**A3**	**A2LO = 0**	**A2LO = 1**
0	0	0	0 through 3	4 through 7
0	0	1	8 through 11	12 through 15
0	1	0	16 through 19	20 through 23
0	1	1	24 through 27	28 through 31
1	0	0	32 through 35	36 through 39
1	0	1	40 through 43	44 through 47
1	1	0	48 through 51	52 through 55
1	1	1	56 through 59	60 through 63

DS2268 ADDRESS STRAPPING Table 3

A5	A4	A3	Eight Block Address Selected
0	0	0	0 through 7
0	0	1	8 through 15
0	1	0	16 through 23
0	1	1	24 through 31
1	0	0	32 through 39
1	0	1	40 through 47
1	1	0	48 through 55
1	1	1	56 through 63

SYSTEM RESET

A system reset may be initialized with a high-low-high transition on the RST\ pin. This action clears all of the internal registers, resets the ADPCM algorithms, and places the processors in idle (outputs 3-stated). On system power-up, the RST\ pin should be held low for at least 1 millisecond after the master clock (MCLK) has stabilized to assure proper initialization. Use of a DS1231 or DS1232 will automatically generate a reset when power is applied. Please see the Dallas Semiconductor Data Book for more information on the DS1231 and DS1232.

SIP Stik CONNECTORS

The DS2264 and DS2268 are designed to connect into a standard 35-pin SIMM connector with a pin spacing pitch of 0.100 inches. Both vertical and inclined connectors are available from connector vendors such as AMP and Molex. Table 4 lists two such connectors.

35-PIN SIMM CONNECTORS FOR DS2264/DS2268 Table 4

Description	Vendor	Part Number
Vertical upright	AMP	821828-3
Low profile, 25 degree angle	Molex	15-46-0385

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{cc}+0.3V		
Logic 0	V_{IL}	-0.3		+0.8V		
Supply	V_{DD}	4.5		5.5V		

CAPACITANCE (t_A=25C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			20	pF	
Output Capacitance	C_{OUT}			40	pF	4
				80	pF	5

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{DDA}			175	mA	1,2,4
				280	mA	1,2,5
Standby Current	I_{DDPD}			50	mA	1,2,3,4
				50	mA	1,2,3,5
Input Leakage	I_I	-20.0		+20.0	uA	
Ouput Leakage	I_{IO}	-4.0		+4.0	uA	4,6
		-8.0		+8.0	uA	5,6
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. CLKX = CLKY = 1.544MHz; MCLK = 10MHz.
2. Outputs open; inputs swinging full supply levels.
3. All channels of all processors programmed to idle (IPD = 1).
4. For DS2264 only.
5. For DS2268 only.
6. XOUT and YOUT 3-stated.

PCM INTERFACE
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/-10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLKX, CLKY Period	t_{PXY}	244		5208	ns	4
CLKX, CLKY Pulse Width	t_{WXYL} t_{WXYH}	100			ns	
CLKX, CLKY Rise Fall Times	t_{RXY} t_{FXY}		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	t_{HOLD}	0			ns	1
Setup Time from FSX, FSY High to CLKX, CLKY Low	t_{SF}	50			ns	1
Hold Time from CLKX, CLKY Low to FSX, FSY Low	t_{HF}	100			ns	1
Setup Time for XIN, YIN to CLKX, CLKY Low	t_{SD}	50			ns	1
Hold Time for XIN, YIN to CLKX, CLKY Low	t_{HD}	50			ns	1
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	t_{DXYO}	10		150	ns	2
Delay Time from CLKX, CLKY to XOUT, YOUT 3-stated	t_{DXYZ}	20		150	ns	1,2,3

NOTES:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.
2. Load = 150pF + 2 LSTTL loads.
3. For LSB of PCM or ADPCM byte.
4. Maximum width of FSX and FSY is one CLKX or CLKY period.

MASTER CLOCK / RESET
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	1
MCLK Pulse Width	t_{WMH} t_{WML}	45	50	55	ns	
MCLK Rise/Fall Times	t_{RM}, t_{FM}			10	ns	
RST Pulse Width	t_{RST}	1			ms	

NOTE:
1. MCLK = 10MHz +/- 500ppm.

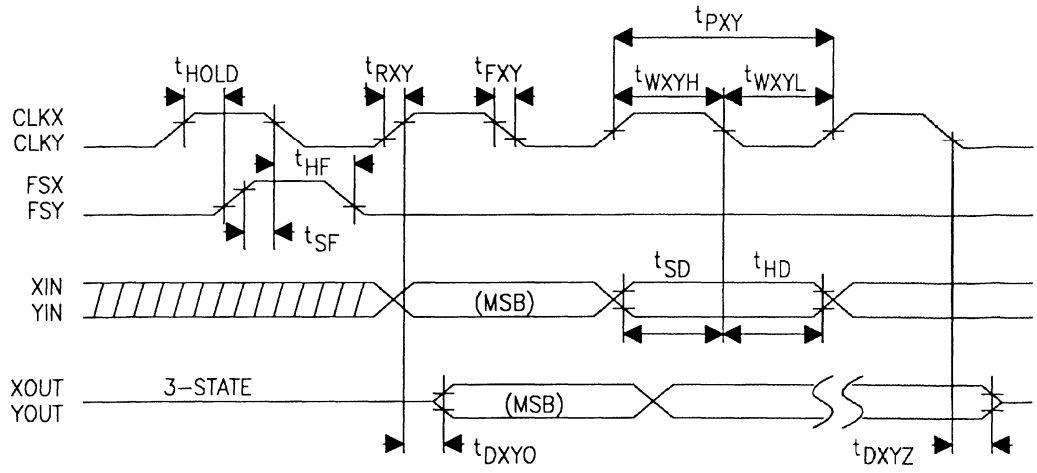
SERIAL PORT
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/- 10%)

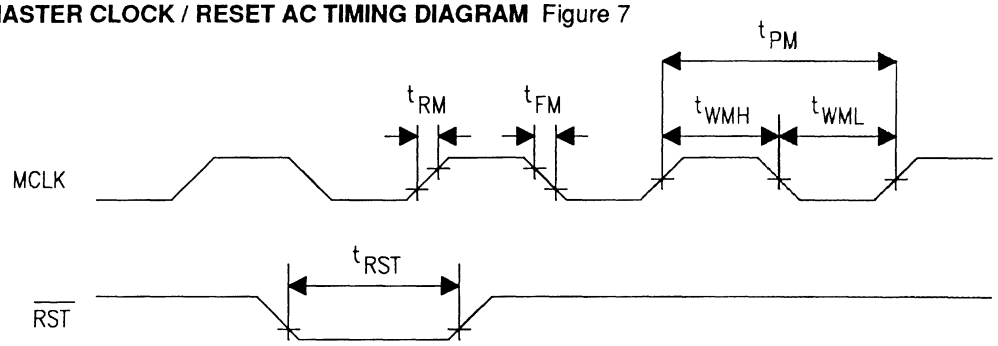
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Set Up	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Time	t_R, t_F			100	ns	1
CS to SCLK Set Up	t_{CC}	50			ns	1
SCLK to CS Hold	t_{CCH}	250			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
SCLK Set Up to CS Falling	t_{SCC}	50			ns	1

NOTE:
1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.

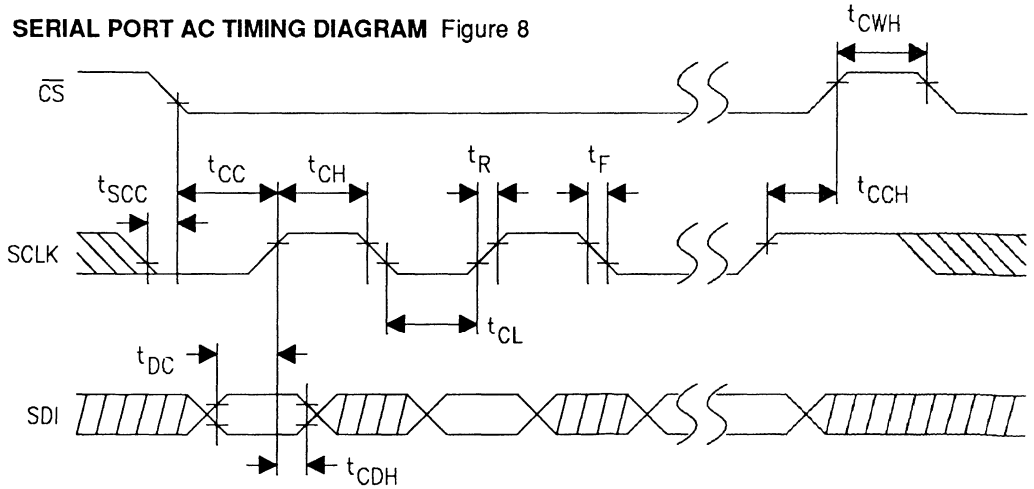
PCM INTERFACE AC TIMING DIAGRAM Figure 6



MASTER CLOCK / RESET AC TIMING DIAGRAM Figure 7

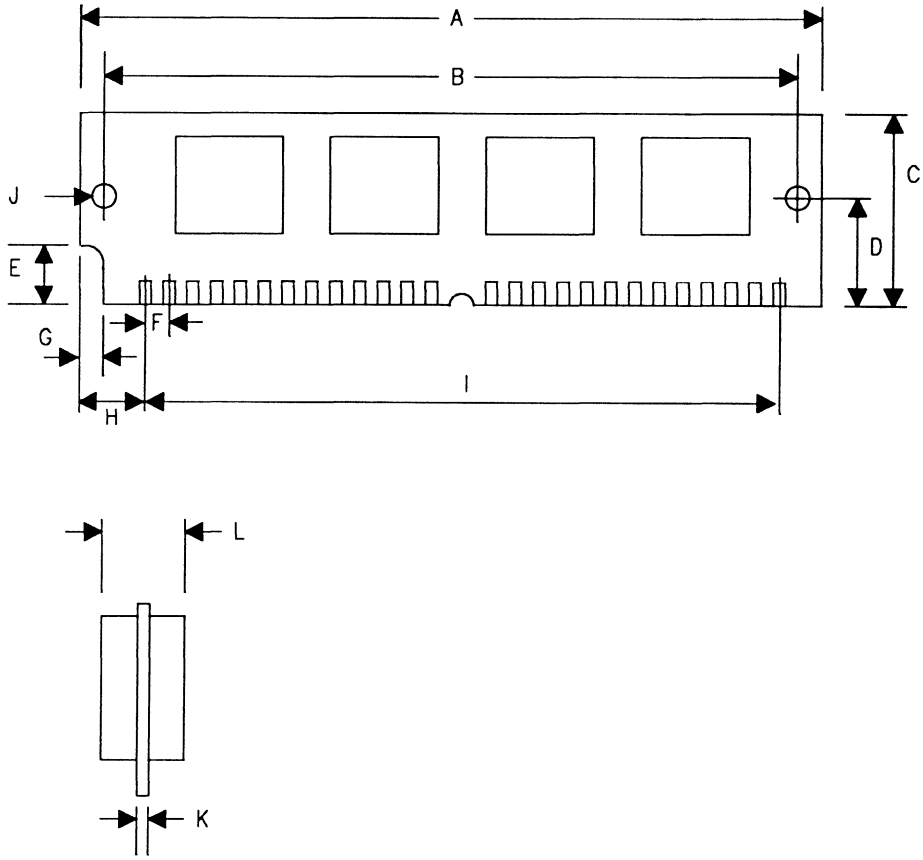


SERIAL PORT AC TIMING DIAGRAM Figure 8



DS2264
DS2268
ADPCM Stik

DIM.	INCHES
A	4.000
B	3.734
C	0.800
D	0.400
E	0.250
F	0.100
G	0.080
H	0.300
I	3.400
J	0.125 DIA
K	0.050
L	0.460



7

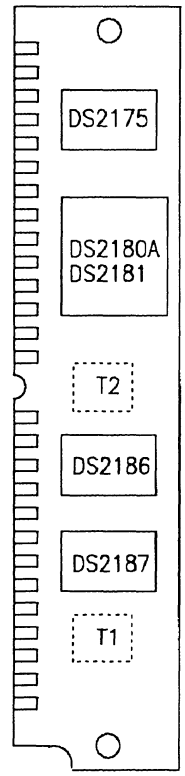
DALLAS SEMICONDUCTOR

DS2280
DS2281
T1 LINE CARD Stik™
CEPT LINE CARD Stik™

FEATURES

- Pretested, snap-In T1 or CEPT line card
- DS2280 T1 Line Card
  DS2281-075 75 ohm CEPT Line Card
  DS2281-120 120 ohm CEPT Line Card
- Consumes only 2 square inches of board space
- Performs four functions:
  - line interface
  - framing
  - monitoring
  - buffering
- DS2280 and DS2281 share the same pinout
- Includes line interface transformers and termination resistors
- Connects to both 1.544MHz and 2.048MHz backplanes
- Operates off a single +5V supply

Stik LAYOUT



(actual size)

DESCRIPTION

The DS2280 and DS2281 are T1 and CEPT line cards that consume only two square inches of printed circuit board space. The cards are designed to plug into standard 68-pin Single In-Line connectors. They have been arranged for maximum flexibility and contain all the necessary hardware to connect directly to either T1, or CEPT 75 ohm lines, or CEPT 120 ohm lines. The line interface function is performed by the DS2187 and DS2186. The monitoring and framing functions are performed by the DS2180A on the DS2280 and by the DS2181 on the DS2281. The buffering function is handled by the DS2175. The DS2280 and DS2281 provide all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). They also provide indication of frame errors, CRC-6 or CRC-4 errors, and bipolar violations.

OVERVIEW

The DS2280 contains four of Dallas Semiconductor's T1 integrated circuits; the DS2187 Receive Line Interface, the DS2186 Transmit Line Interface, the DS2180A T1 Transceiver, and the DS2175 Elastic Store. The DS2281 replaces the DS2180A with the DS2181 CEPT Transceiver. The operational specifics of each of these devices can be found in their individual data sheets. On the Line Card Stiks, the DS2187 connects to the receive signal through a 1:2 transformer. On the DS2280, the T1 line is properly terminated by two 200 ohm resistors (R1 and R2). On the DS2281-075, R1 and R2 are set to 150 ohms so that the CEPT lines can be properly terminated at 75 ohms. And on the DS2281-120, R1 and R2 are set at 240 ohms. The DS2187 recovers clock and data from the T1 or CEPT line and provides it to the DS2180A or DS2181. The transceiver frames to the incoming data stream and provide status information on the received data. The D2180A and DS2181 transceivers can be used in either the software or hardware modes. In the software mode, an external controller is used to access a set of internal registers via a serial port. These registers are used to configure the device and to retrieve monitoring information. In the hardware mode, the Stiks can used without an external controller. In this mode, the serial port pins are redefined as device configuration pins. Please consult the DS2180A and DS2181 data sheets for full details on both the software and hardware modes.

The DS2280 and DS2181 also contain an elastic store, the DS2175. The DS2175 can perform two functions. First, it can be used to absorb clock rate and phase differences between the clock recovered by the DS2187 and a system backplane clock. It can also be used to connect the DS2280 to 2.048MHz backplanes or to connect the DS2281 to 1.544MHz backplanes.

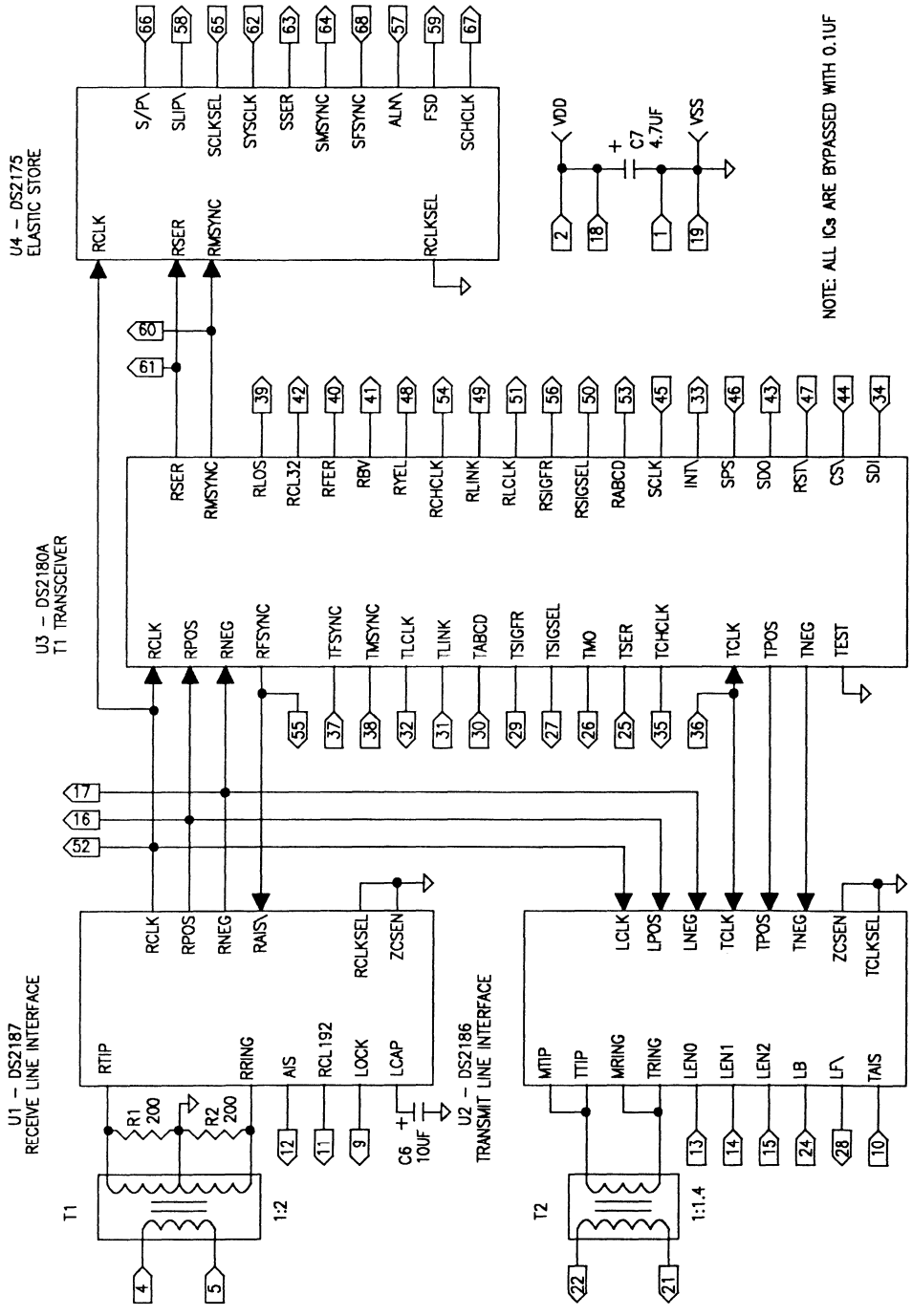
The DS2187, DS2180A, and DS2175 form the receive section of the DS2280. On the DS2281, the receive section is formed by the DS2187, DS2181, and DS2175. The transmit section of the DS2280 and DS2181 is formed by the transceiver and the Transmit Line Interface, the DS2186. Data that is to be transmitted onto the transmit T1 twisted wire pair or CEPT lines is clocked into the DS2180A or DS2181 tranceivers with a transmit clock (TCLK). The transceivers format the data stream and add any additional information (signaling, CRC-6 or CRC-4, etc.) that might be necessary. The transceiver also transforms the data stream from a unipolar to a bipolar format and, if selected, it will perform B8ZS or HDB3 encoding. Bipolar data from the DS2180A or DS2181 is clocked into the DS2186 where it is level shifted and driven onto the transmit T1 twisted pair or CEPT line via a 1:1.4 transformer. On the DS2280, the waveshape of the transmitted pulses is selected via the Line Build Out pins, LEN0 to LEN2. A schematic of the DS2280 is shown in Figure 1 and a schematic of the DS2281 is shown in Figure 2. The DS2280 and DS2281 are arranged for maximum flexibility. One possible configuration for each is shown in Figures 3 and 4.

The DS2280 and DS2281 are designed to connect into a standard 68-pin Single In-Line connector with a pin spacing pitch of 0.050 inches. Both inclined and vertical connectors are available from connector vendors such as AMP. A right angle connector will be offered by AMP in the near future. Table 1 lists a set of suitable connectors from AMP's MicroEdge™ Line.

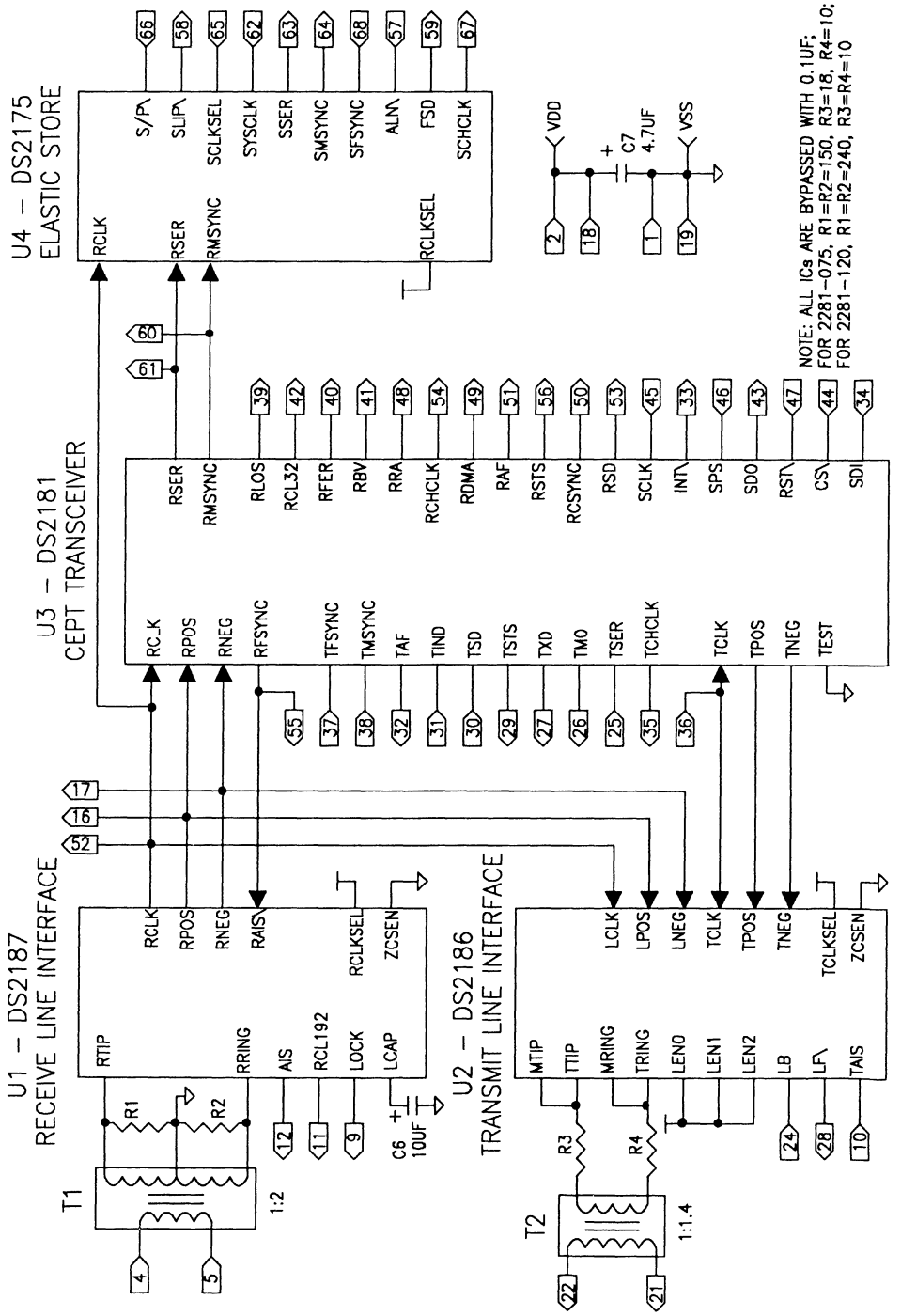
68-PIN CONNECTORS FOR DS2280 AND DS2281 Table 1

Description	Vendor	Part #
Vertical Single Row with Center Posts (Tin)	AMP	821824-2
Vertical Single Row without Center Posts (Tin)	AMP	821824-7
Vertical Single Row with Center Posts (Gold)	AMP	821825-2
Vertical Single Row without Center Posts (Gold)	AMP	821825-7
Inclined Single Row with Center Posts (Tin)	AMP	821907-2
Inclined Single Row without Center Posts (Tin)	AMP	821907-6
Inclined Single Row with Center Posts (Gold)	AMP	821902-2
Inclined Single Row without Center Posts (Gold)	AMP	821902-6

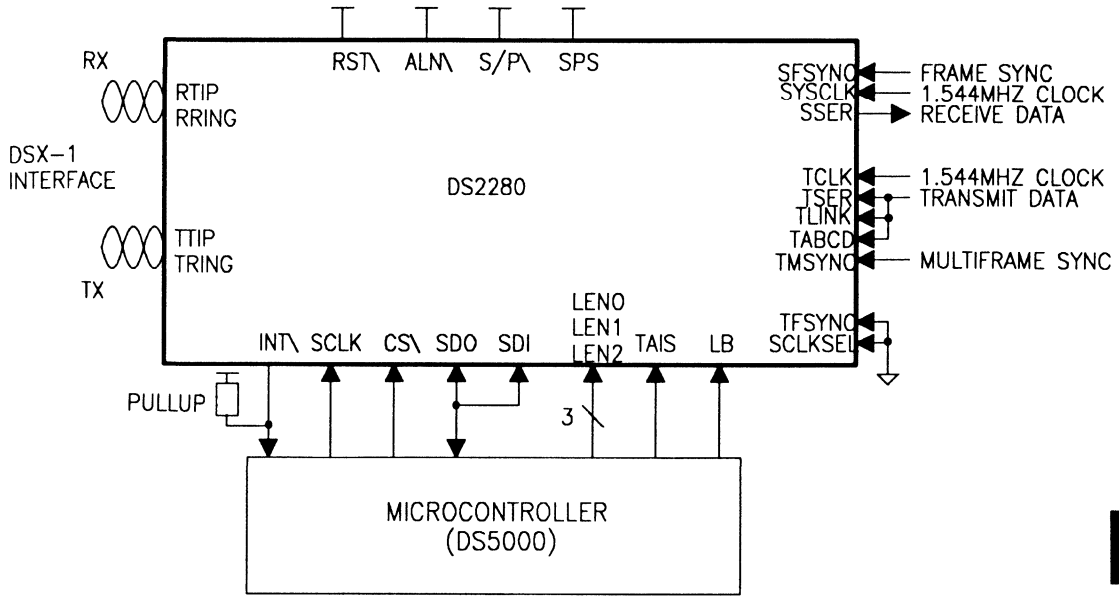
DS2280 SCHEMATIC Figure 1



DS2281 SCHEMATIC Figure 2



TYPICAL DS2280 APPLICATION Figure 3



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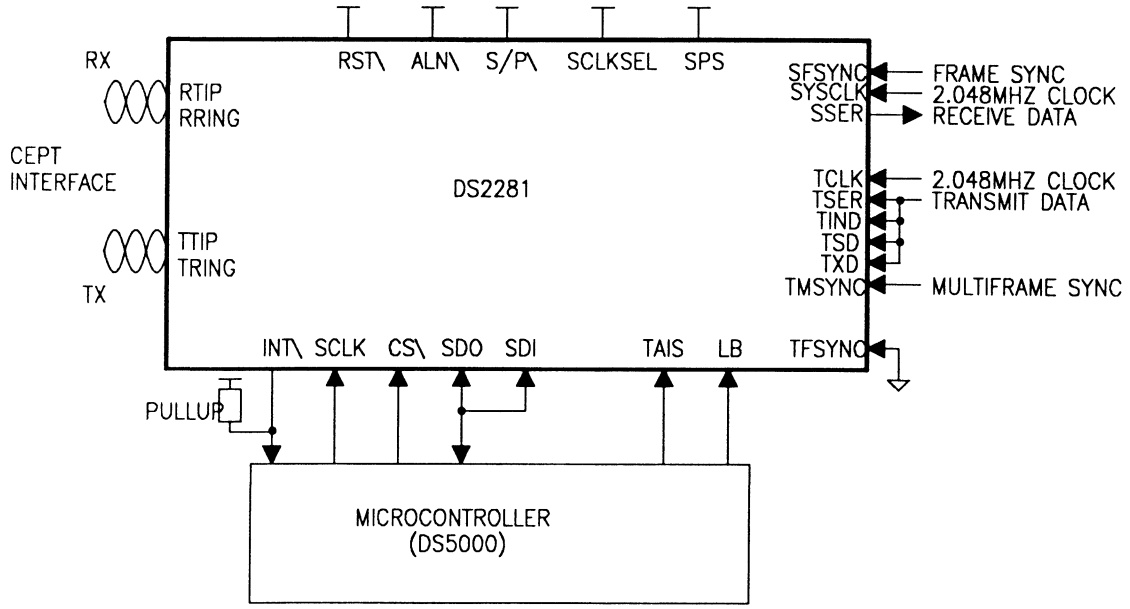
TYPICAL DS2281 APPLICATION Figure 4



PIN DESCRIPTION Table 2

PIN	SYMBOL	TYPE	DEVICE	DESCRIPTION
1	**VSS**	-	-	**Ground.** Connect to 0.0V.
2	**VDD**	-	-	**Positive Supply.** Connect to 5.0V.
3	**NC**	-	-	**No Connect.** No internal connection.
4 5	**RTIP** **RRING**	I	DS2187	**Receive Tip and Ring.** Connects directly to the receiver T1 twisted pair or CEPT lines.
6	**NC**	-	-	**No Connect.** No internal connection.
7	**NC**	-	-	**No Connect.** No internal connection.
8	**NC**	-	-	**No Connect.** No internal connection.
9	**LOCK**	O	DS2187	**Frequency Lock Indication.** High state indicates that the DS2187 is phase and frequency- locked to the incoming signal at RTIP and RRING.
10	**TAIS**	I	DS2186	**Transmit Alarm Indication Signal.** When strapped high, an unframed all ones signal is transmitted at TTIP and TRING at the TCLK rate.
11	**RCL192**	O	DS2187	**Receive Carrier Loss.** High state indicates that at least 192 consecutive zeros have been received at RTIP and RRING.
12	**AIS**	O	DS2187	**Receive Alarm Indication Signal.** High state indicates that the receive data stream at RTIP and RRING contains less than three zeros over two full frames of incoming data.
13 14 15	**LEN0 (2280)** **LEN1 (2280)** **LEN2 (2280)**	I	DS2186	**Line Length Select.** State of these three pins determines the output T1 waveform shape. See Table 3.
13 14 15	**NC (2281)** **NC (2281)** **NC (2281)**	-	-	**No Connect.** No internal connection.

16 17	**RPOS** **RNEG**	O	DS2187	**Receive Positive and Negative Data.** Data extracted from the T1 or CEPT line by the DS2187.
18	**VDD**	-	-	**Positive Supply.** Connect to 5.0V.
19	**VSS**	-	-	**Ground.** Connect to 0.0V.
20	**NC**	-	-	**No Connect.** No internal connection.
21 22	**TRING** **TTIP**	O	DS2186	**Transmit Tip and Ring.** Connects directly to the transmit T1 twisted pair or CEPT line.
23	**NC**	-	-	**No Connect.** No internal connection.
24	**LB**	I	DS2186	**Line Loopback.** When strapped high, clock and data received at RTIP and RRING is looped back to TTIP and TRING.
25	**TSER**	I	DS2180A DS2181	**Transmit Serial Data.** NRZ data input, sampled on the falling edge of TCLK.
26	**TMO**	O	DS2180A DS2181	**Transmit Multiframe Out.** Output of the internal multiframe counter; indicates multiframe boundaries.
27	**TSIGSEL (2280)**	O	DS2180A	**Transmit Signaling Select.** A .667KHz clock which identifies signaling frames A and C in 193E framing; a 1.33KHz clock in 193S framing.
	TXD (2281)	I	DS2181	**Transmit Extra Data.** Sampled on falling edge of TCLK during bit times 5, 7, and 8 of timeslot 16 in frame 0 when CAS is enabled.
28	**LF**	O	DS2186	**Line Fault.** Open collector; active low output. Held low during an output driver fault or failure; 3-stated otherwise.
29	**TSIGFR (2280)**	O	DS2180A	**Transmit Signaling Frame.** High during signaling frames, low otherwise.
	TSTS (2281)	O	DS2181	**Transmit Signaling Timeslot.** High during time slot 16 of every frame, low otherwise.

7

30	**TABCD (2280)**	I	DS2180A	**Transmit ABCD Signaling Data.** When enabled via TCR.4 in the DS2180A, the LSB time of each channel will be sampled in signaling frames on falling edge of TCLK.
	TSD (2281)	I	DS2181	**Transmit Signaling Data.** CAS signaling data input; sampled on falling edge of TCLK for insertion into outgoing time slot 16 when enabled.
31	**TLINK (2280)**	I	DS2180A	**Transmit Link Data.** Sampled during the F-bit time on the falling edge of TCLK. Sampled in odd frames in 193E framing and in even frames for 193S if enabled via TCR.2 in the DS2180A.
	TIND (2281)	I	DS2181	**Transmit International and National Data.** Sampled on falling edge of TCLK during bit 1 of timeslot 0 of every frame (international) and/or during bit times 4 through 8 of time-slot 0 during non-align frames (national) when enabled.
32	**TLCLK (2280)**	O	DS2180A	**Transmit Link Clock.** A 4KHz demand clock for the TLINK input.
	TAF (2281)	O	DS2181	**Transmit Alignment Frame.** High during frames containing the frame alignment signal, low otherwise.
33	**INT**	O	DS2180A DS2181	**Receive Alarm Interrupt.** Flags host controller during alarm conditions. Active low, open drain output.
34	**SDI**	I	DS2180A DS2181	**Serial Data In.** Data for onboard registers. Sampled on the rising edge of SCLK.
35	**TCHCLK**	O	DS2180A	**Transmit Channel Clock.** 192KHz or 256KHz clock DS2181 which identifies time-slot (channel) boundaries.
36	**TCLK**	I	DS2186 DS2180A DS2181	**Transmit Clock.** A 1.544MHz or 2.048MHz clock with the proper accuracy and jitter characteristics should be applied here.

37	**TFSYNC**	I	DS2180A DS2181	**Transmit Frame Sync.** Rising edge identifies frame boundary; may be pulsed every frame to reinforce internal frame counter, or tied low, allowing TMSYNC to establish multiframe and frame alignment.
38	**TMSYNC**	I	DS2180A DS2181	**Transmit Multiframe Sync.** May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows the internal multiframe counter to run free.
39	**RLOS**	O	DS2180A DS2181	**Receive Loss of Sync.** Indicates sync status; high when a resync is in progress, low otherwise.
40	**RFER**	O	DS2180A DS2181	**Receive Frame Error.** Transitions high when either a frame or CRC or CAS multiframe error event occurs.
41	**RBV**	O	DS2180A DS2181	**Receive Bipolar Violation.** Transitions high when a bipolar violation is detected.
42	**RCL32**	O	DS2180A	**Receive Carrier Loss.** High state indicates that at least 32 consecutive zeros have been received at RTIP and RRING.
43	**SDO**	O	DS2180A DS2181	**Serial Data Out.** Control and status information from the onboard registers. Updated on falling edge of SCLK, 3-stated during serial port write or when CS\ is high.
44	**CS**	I	DS2180A DS2181	**Chip Select.** Must be low to write to or read from the serial port.
45	**SCLK**	I	DS2180A DS2181	**Serial Data Clock.** Used to read or write serial port registers.
46	**SPS**	I	DS2180A DS2181	**Serial Port Select.** Tie to VDD to select the serial port (software mode). Tie to VSS to select the hardware mode.

47	**RST**	I	DS2180A DS2181	**Reset.** A high-low transition clears all internal registers and resets the receive side counters. A high-low-high transition will initiate a resync.
48	**RYEL (2280)**	O	DS2180A	**Receive Yellow Alarm.** High state indicates that a yellow alarm has been detected in the T1 data stream received at RTIP and RRING.
	RRA (2281)	O	DS2181	**Receive Remote Alarm.** Transitions high when alarm detected, low when alarm cleared.
49	**RLINK (2280)**	O	DS2180A	**Receive Link Data.** In 193E framing mode, updated with extracted FDL data one RCLK before the start of odd frames and held until the next update. In 193S framing mode, updated with extracted S-bit data one RCLK before the start of even frames and held until the next update.
	RDMA (2281)	O	DS2181	**Receive Distant Multiframe Alarm.** Transitions high when alarm detected, low when alarm cleared.
50	**RSIGSEL (2280)**	O	DS2180A	**Receive Signaling Select.** A .667KHz clock which identifies signaling frames A and C in 193E framing; a 1.33KHz clock in 193S framing.
	RCSYNC (2281)	O	DS2181	**Receive CRC4 Sync.** Low-high transition indicates start of CRC4 multiframe, held high during CRC4 frames 0 through 7 and low during frames 8 through 15.
51	**RLCLK (2280)**	O	DS2180A	**Receive Link Clock.** A 4KHz demand clock for RLINK.
	RAF (2281)	O	DS2181	**Receive Alignment Frame.** High during frames containing the frame alignment signal, low otherwise.

52	**RCLK**	O	DS2187	**Receive Clock.** A 1.544MHz or 2.048MHz clock that is recovered from the incoming data stream at RTIP and RRING by the DS2187. Fed to all the other devices on the DS2280 and DS2281.
53	**RABCD (2280)**	O	DS2180A	**Receive ABCD Signaling.** Extracted signaling data output, valid for each channel time in signaling frames. In non-signaling frames, RABCD outputs the LSB of each channel word.
	RSD (2281)	O	DS2181	**Receive Signaling Data.** Extracted time slot 16 data.
54	**RCHCLK**	O	DS2180A DS2181	**Receive Channel Clock.** 192KHz or 256KHz clock which identifies timeslot (channel) boundaries.
55	**RFSYNC**	O	DS2180A DS2181	**Receive Frame Sync.** Extracted 8KHz signal that indicates the beginning of each frame.
56	**RSIGFR (2280)**	O	DS2180A	**Receive Signaling Frame.** High during signaling frames, low during resync and non-signaling frames.
	RSTS (2281)	O	DS2181	**Receive Signaling Timeslot.** High during timeslot 16 of every frame, low otherwise.
57	**ALN**	I	DS2175	**Align.** When forced low, ALN\ recenters the buffer on the next system side frame sync boundary as determined by SFSYNC.
58	**SLIP**	O	DS2175	**Frame Slip.** Held low for 65 SYSCLK cycles when a slip occurs. Active low, open drain output.
59	**FSD**	O	DS2175	**Frame Slip Direction.** State indicates direction of the last slip; latched on a slip occurrence. Low state indicates that the buffer is empty and a frame was repeated. High state indicates that the buffer is full and a frame was deleted.

60	**RMSYNC**	O	DS2180A DS2181	**Receive Multiframe Sync.** Extracted multiframe sync; rising edge indicates the start of a multiframe.
61	**RSER**	O	DS2180A DS2181	**Receive Serial Data.** Received NRZ serial data, updated on the rising edge of RCLK.
62	**SYSCLK**	I	DS2175	**System Clock.** A 1.544MHz or 2.048MHz data clock.
63	**SSER**	O	DS2175	**System Serial Data.** Updated on the rising edge of SYSCLK.
64	**SMSYNC**	O	DS2175	**System Multiframe Sync.** Slip-compensated multiframe output; used with RMSYNC to monitor depth of the DS2175 buffer real time.
65	**SCLKSEL**	I	DS2175	**System Clock Select.** Tie to VSS for 1.544MHz backplane applications; tie to VDD for 2.048MHz backplane applications.
66	**S/P**	I	DS2175	**Serial/Parallel Select.** Tie to VSS for parallel backplane applications; tie to VDD for serial backplane applications.
67	**SCHCLK**	O	DS2175	**System Channel Clock.** Transitions high on channel boundaries.
68	**SFSYNC**	I	DS2175	**System Frame Sync.** Rising edge establishes system side frame boundaries.

T1 TRANSMIT LINE LENGHT SELECTION Table 3

LEN2	LEN1	LEN0	WAVEFORM SELECTED
0	0	0	Do not use
0	0	1	Do not use
0	1	0	Do not use
0	1	1	DSX-1 Crossconnect; 0 to 133 feet
1	0	0	DSX-1 Crossconnect; 133 to 266 feet
1	0	1	DSX-1 Crossconnect; 266 to 399 feet
1	1	0	DSX-1 Crossconnect; 399 to 533 feet
1	1	1	DSX-1 Crossconnect; 533 to 655 feet

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	VIH	2.0		Vcc+0.3	V	1
Logic 0	VIL	-0.3		+0.8	V	1
Supply	VDD	4.75		5.25	V	

CAPACITANCE

(tA=25C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		20		pF	1
Output Capacitance	COUT		40		pF	1

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D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C; VDD=5V+/-5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	IDD		70	90	mA	2
Input Leakage	II	-1.0		+1.0	uA	3,5
Output Leakage	IO	-1.0		+1.0	uA	4
Output Current (2.4V)	IOH	-1.0			mA	6
Output Current (0.4V)	IOL	+4.0			mA	6

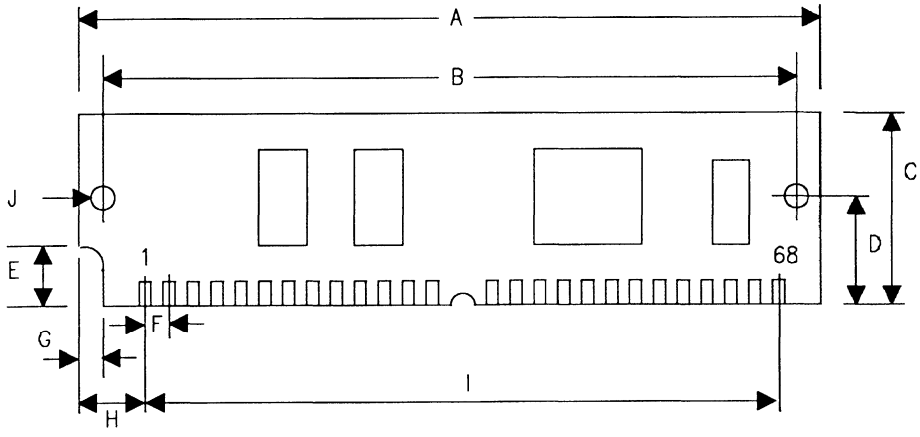
NOTES:

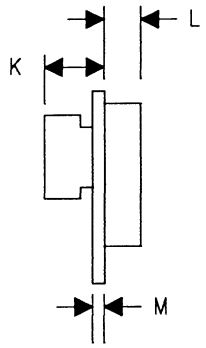
1. Does not apply to RTIP, RRING, TTIP, or TRING.
2. VDD = 5.25V and TCLK = 2.048MHz.
3. VSS < VIN < VDD.
4. Applies to open collector outputs (LF\, SLIP\, INT\).
5. All inputs except RTIP and RRING.
6. All outputs except TTIP and TRING.

NOTE:

All AC Electrical Parametrics can be found in the individual data sheets on the DS2187, DS2186, DS2180A, DS2181, and DS2175.

DS2280
T1 LINE CARD Stik
DS2281
CEPT LINE CARD Stik





DIMENSION	INCHES
A	4.050
B	3.784
C	0.850
D	0.400
E	0.250
F	0.050
G	0.080
H	0.250
I	3.550
J	0.125 DIA
K	0.300
L	0.173
M	0.050

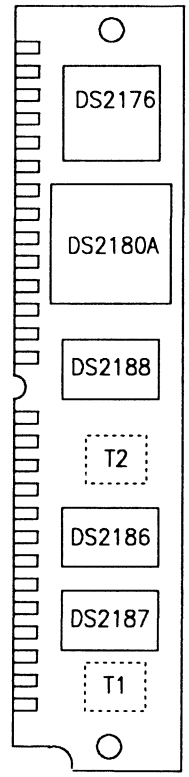
DALLAS SEMICONDUCTOR

DS2283
ENHANCED T1 LINE CARD
Stik™

FEATURES

- Pretested, snap-In T1 line card
- Consumes only 2 square inches of board space
- Performs six functions:
  - line interface
  - clock and data dejittering
  - framing
  - monitoring
  - buffering
  - robbed-bit signaling extraction
- Includes line interface transformers and termination resistors
- Three separate loopback modes: payload, line, and local
- Connects to both 1.544MHz and 2.048MHz backplanes
- Fully CMOS for low power consumption
- Operates off a single +5V supply

Stik LAYOUT



Actual Size

DESCRIPTION

The DS2283 is a T1 line card that consumes only two square inches of printed circuit board space. The card is designed to plug into standard 68-pin Single In-Line connectors. It has been arranged for maximum flexibility and contains all the necessary hardware to connect directly to T1 DSX-1 twisted pair lines. The line interface function is performed by the DS2187 and DS2186. The dejittering of the clock and data is performed by the DS2188. The monitoring and framing functions are performed by the DS2180A. The buffering and robbed-bit signaling extraction functions are handled by the DS2176. The DS2283 provides all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). It also provides indication of frame errors, CRC-6 errors, and bipolar violations. Please contact the factory for more information on this product.

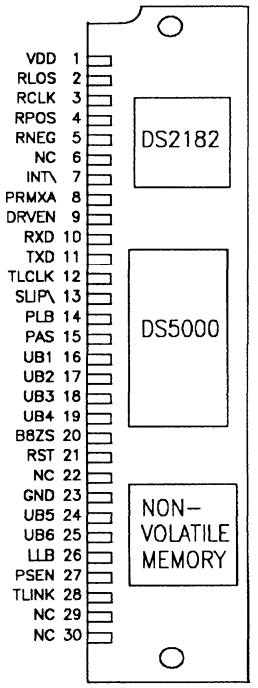
DALLAS SEMICONDUCTOR

DS2282
T1 FDL CONTROLLER/ MONITOR Stik™

FEATURES

- Fully implements the FDL message format as described in TR-TSY-000194 and T1.403-1989
- Supports both Scheduled Performance Report Messages and Unscheduled Messages
- Software implementation allows adaptation to evolving standards
- Provides high-level monitor counts, namely:
  - Errored Seconds
  - Severely Errored Seconds
  - Unavailable Seconds
- Important counts are stored in nonvolatile memory
- Works in conjunction with the DS2280T1 Line Card Stik or DS2180A T1 Transceiver
- Simple serial port used to retrieve information and control operation
- Can be used without an external controller
- Connects to a standard 30-pin Single In-Line connector
- Single +5V supply

Stik LAYOUT



(actual size)

DESCRIPTION

The DS2282 completely controls the Facility Data Link (FDL) as described in the Bellcore document TR-TSY-000194 (Extended Superframe Format Interface Specification - December 1987) and the ANSI document T1.403-1989 (Carrier to Carrier Installation - DS1 Metallic Interface). It also provides a number of important performance parameters involved in monitoring T1 lines. Since the DS2282 is implemented using the DS5000 Soft Microcontroller, it easily adapts to evolving T1 standards and can be customized to meet the user's needs. For example, the DS2282 could be modified to implement the TABS protocol as described in the AT&T Communications document PUB 54016.

OVERVIEW

The DS2282 has two main functions: it controls the Facility Data Link (FDL) for Performance Report Messages (PRM) and unscheduled messages as described in TR-TSY-000194, and it also provides monitoring data as outlined in TA-TSY-000147 and similar documents. (See Figure 1.) Recovered data off of a T1 line is clocked into the DS2282 via the RPOS and RNEG pins with the RCLK signal. The DS2282 synchronizes to the incoming data stream and extracts the FDL. Once the FDL has been extracted, it is examined for both PRMs and for unscheduled messages. Incoming PRMs are reported in a set four registers labeled PRMR0 to PRMR3. Incoming unscheduled messages are reported via the RUMR register. The DS2282 also calculates Errored Seconds (ES) and Severely Errored Seconds (SES) off of the incoming PRMs and reports the count in the PRMESR and PRMSESR registers.

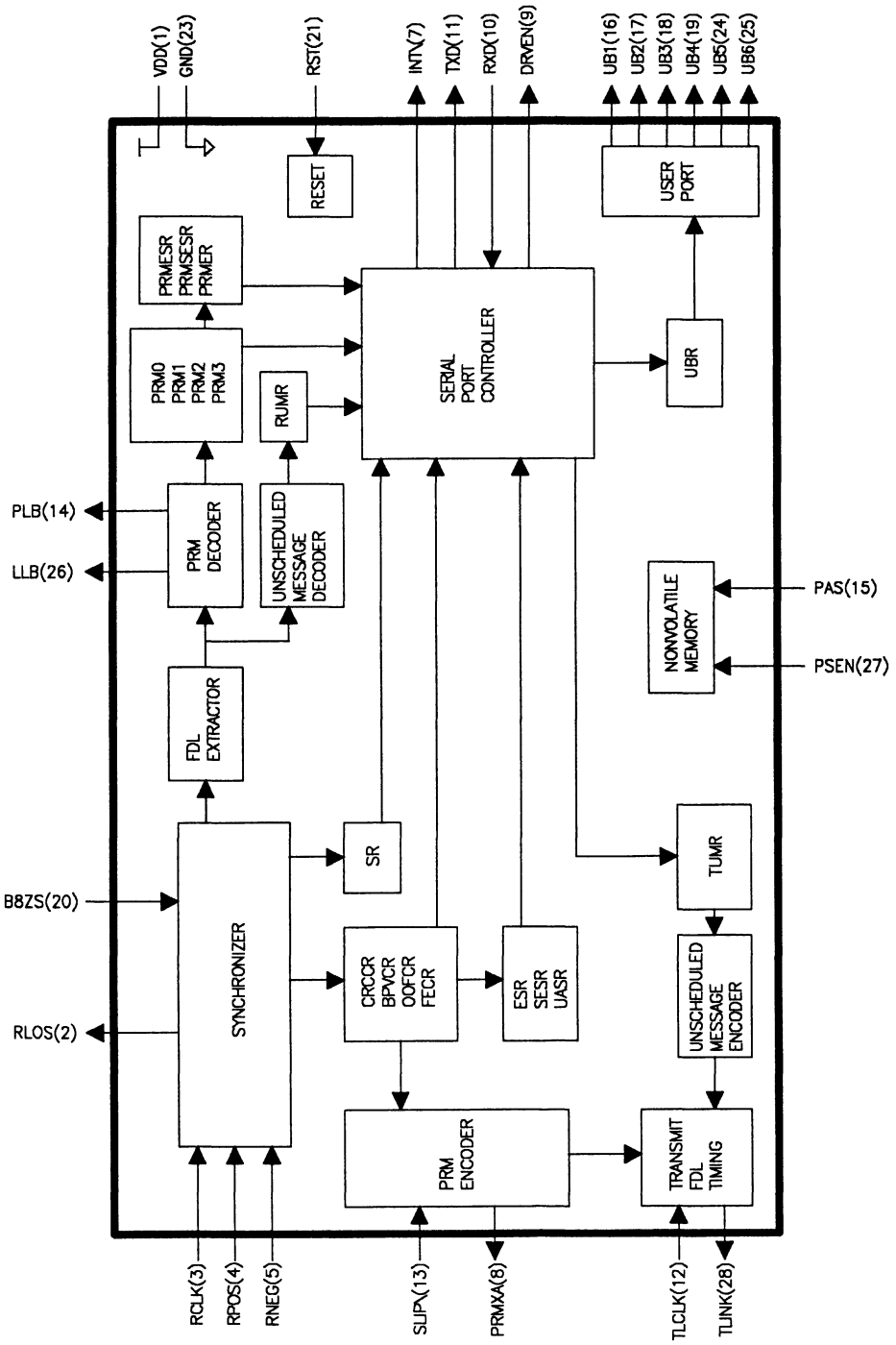
The DS2282 also monitors the incoming data stream for bipolar violations, CRC errors, out of frame error events, and frame error events. Counts of these error events are recorded in the BPVCR, CRCCR, OOFCR, and FECR registers respectively. The DS2282 combines the information in these registers along with the indication of local slips via the SLIP\ signal, to create PRMs that are transmitted once a second via the TLINK signal. The DS2282 also uses these registers to count ES, SES, as well as Unavailable Seconds (UAS). Counts for ES, SES, and UAS are reported in the ESR, SESR, and UASR registers, respectively. Unscheduled messages can be transmitted by placing the proper code in the TUMR register. There is also a register available for the user's customized purposes. Pins UB1 to UB6 can be set either high or low by programming the appropriate bit in the USR register.

An asynchronous serial port is used to control the DS2282 and to retrieve data from it. The port is operated at 19.2 Kbps. Access to all eighteen onboard registers is achieved via the serial port. An address can be assigned to this serial port. This allows a single external controller to communicate over a single bus to as many as 32 separate DS2282s. Each DS2282 will listen for its address and only respond when it is asked to do so.

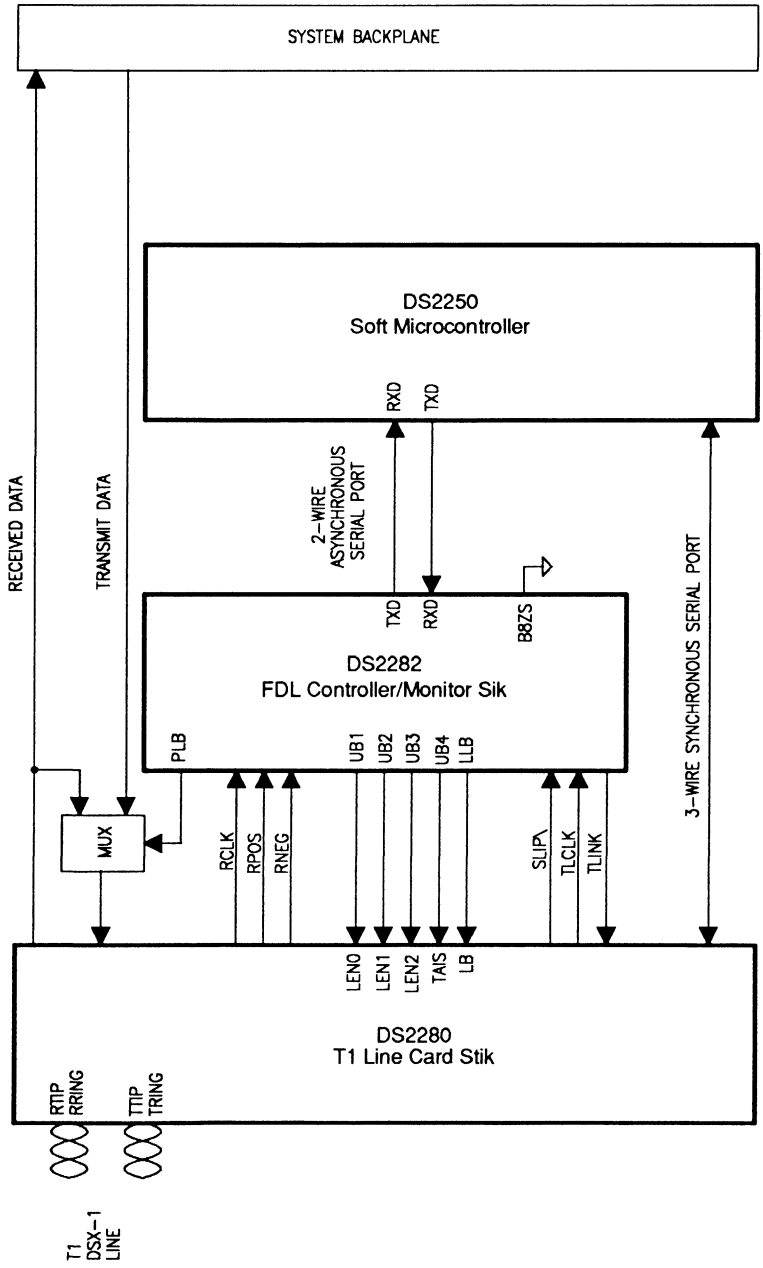
All of the registers in the DS2282 that either count error events or errored time intervals are recorded in onboard, nonvolatile memory. Hence, in case of a local loss of power, these registers will maintain their counts.

A typical application of the DS2282 is shown in Figure 2. In this application, the DS2282 is completely controlling the FDL as well as monitoring the T1 line. The DS2250 Soft Micro Stik is used to configure the DS2282 and to extract any performance data that may be required. In this application, the DS2250 is also being used to control the DS2280 T1 Line Card Stik. The mux is necessary to perform payload loopback.

DS2282 BLOCK DIAGRAM Figure 1



TYPICAL SYSTEM APPLICATION Figure 2



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PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	**VDD**	-	**Positive Supply.** 5.0 Volts.
2	**RLOS**	O	**Receive Loss Of Sync.** Indicates sync status; high when internal resync is in progress, low otherwise.
3	**RCLK**	I	**Receive Clock.** 1.544MHz clock input. All internal time intervals are derived from this clock.
4 5	**RPOS** **RNEG**	I	**Receive Bipolar Data.** Sampled on falling edge of RCLK. Can be tied together to receive NRZ data and disable BPV and B8ZS detection circuitry.
6	**NC**	-	**No Connect.** Do not connect any signal to this pin.
7	**INT**	O	**Interrupt.** Transitions low when bits in the Status Register (SR) change state or when an unscheduled message is received.
8	**PRMXA**	O	**PRM Transmit Active.** Transitions high when a Performance Report Message is being sent via TLINK.
9	**DRVEN**	O	**Serial Port Drive Enable.** Driven high when the DS2282 is transmitting data. Can be used to enable an external line driver.
10	**RXD**	I	**Serial Port Receive.** Serial data input; data is inputted asynchronously at 19.2Kbps.
11	**TXD**	O	**Serial Port Transmit.** Serial data output; data is outputted asynchronously at 19.2Kbps.
12	**TLCLK**	I	**Transmit Link Clock.** 4KHz demand clock for the FDL data.
13	**SLIP**	I	**Slip Occurrence Event.** This pin should be held low for at least 10us when a slip occurs locally. If local slip indications are not available, this pin should be tied high.
14	**PLB**	O	**Payload Loopback.** Transitions high when the code word for payload loopback activate has been received; transitions low when the code word for payload loopback deactivate has been received.
15	**PAS**	I	**Program Address Select.** Used to program the serial port address; active high.

16 17 18 19 24 25	**UB1** **UB2** **UB3** **UB4** **UB5** **UB6**	O	**User Bits 1 to 6.** Each user bit can be independently configured either high or low via the UBR register.
20	**B8ZS**	I	**B8ZS Enable.** Tie low to disable B8ZS; tie high to enable B8ZS. Logically OR'ed with the B8ZS bit in the UBR register; tie low if the B8ZS bit is to be used to select B8ZS mode.
21	**RST**	I	**Reset.** Active high level will initiate a reset. Contains an internal pull-down resister.
22	**NC**	-	**No Connect.** Do not connect any signal to this pin.
23	**GND**	-	**Ground.** 0.0 Volts.
26	**LLB**	O	**Line Loopback.** Transitions high when the code word for line loopback activate has been received; transitions low when the code word for line loopback deactivate has been received.
27	**PSEN**	-	**Program Store Enable.** Used in conjunction with the RST pin to program the onboard nonvolatile memory. In normal applications, do not connect any signal to this pin.
28	**TLINK**	O	**Transmit Link Data.** FDL data to be transmitted; updated on the falling edge of TLCLK.
29	**NC**	-	**No Connect.** Do not connect any signal to this pin.
30	**NC**	-	**No Connect.** Do not connect any signal to this pin.

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SERIAL PORT OPERATION

There are 18 control and information registers in the DS2282. All but two of the registers are read only; USR and TUMR are write only. See Tables 2 through 4. Registers on the DS2282 are read from or written to one at time. Communication over the serial port to one of the registers always consists of either three, four, or five bytes. The first byte is always written to the DS2282 and is called the Address Byte. The Address Byte is actually a byte plus one extra bit. The extra bit is always set to one and is next to the MSB. Hence the Address Byte is actually nine bits long. How to set the serial port address on the DS2282 is described later.

Address Byte

(MSB)								(LSB)
EB	A4	A3	A2	A1	A0	0	0	0

EB	Extra Bit. Should always be set to one.
A4	Address Bit 4. The MSB of the serial port address.
A3	Address Bit 3.
A2	Address Bit 2.
A1	Address Bit 1.
A0	Address Bit 0. The LSB of the serial port address.

The second byte is also always written to the DS2282 and is called the Register Byte. The Register Byte contains the address of the register that is to be either read from or written to. The MSB in the Register Byte is the Clear Bit. The Clear Bit is used to clear a register after it has been read; hence it can only be used in association with read registers. Furthermore, only certain read registers are clearable. See Tables 1 and 2. Typically, the only registers that can be cleared after reading are registers that count events and/or errors.

Register Byte

(MSB)							(LSB)
CB	0	0	A4	A3	A2	A1	A0

CB	Clear Bit. Set to a one if register is to be cleared after reading.
A4	Address Bit 4. The MSB of the register address.
A3	Address Bit 3.
A2	Address Bit 2.
A1	Address Bit 1.
A0	Address Bit 0. The LSB of the register address.

The third byte in the communication over the serial port may be either read from or written to the DS2282. Bytes four and five are always read from the DS2282 since there are no write registers longer than one byte.

Data is read from and written to the DS2282, least significant bit first. Also in multiple byte registers, the least significant byte is read first and the most significant byte is read last.

As an example, if a DS2282 had been programmed for a serial port address of five (decimal) and the user wished to retrieve and clear the count in the BPVCR, then the following transaction would occur:

1. The Address Byte with the Extra Bit set to one and the proper serial port address <100101000> would be written to the DS2282, least significant bit first.
2. The Register Byte with the proper register address for the BPVCR selected and the Clear Bit set to one <10001001> would be written to the DS2282, least significant bit first.
3. The current value in the 24-bit (3-byte) BPVCR is read from the DS2282; the least significant bit in the least significant byte is read first and the most significant bit in the most significant byte is read last.
4. The BPVCR will automatically be reset to zero.

The serial port communication on the DS2282 is handled by the onboard DS5000 Soft Microcontroller. The DS5000 is based on an 8051 type architecture. The DS2282 utilizes the asynchronous Mode 2 operation of a 8051-like microcontroller. Hence, each byte written to the DS2282 must be preceded by a start bit (0) and followed with a stop bit (1). The DS2282 will append start and stop bits to the bytes that it transmits back to an external controller via the TXD pin. More information on Mode 2 operation can be found in the DS5000 User's Guide.

MONITOR REGISTER SUMMARY Table 2

Name	Addr	R/W	Clearable	Description
CRCCR*	01000	R	Yes	**CRC Count Register.** A 16-bit register that counts CRC-6 error events.
BPVCR*	01001	R	Yes	**BPV Count Register.** A 24-bit register that counts bipolar violations.
OOFCR*	01010	R	Yes	**OOF Count Register.** A 16-bit register that counts OOF error events.
FECR*	01011	R	Yes	**Frame Error Count Register.** A 16-bit register that counts errors in the FPS framing pattern.
ESR*	01100	R	Yes	**Errored Second Register.** A 16-bit register that counts ES.
SESR*	01101	R	Yes	**Severely Errored Second Register.** A 16-bit register that counts SES.
UASR*	01110	R	Yes	**Unavailable Seconds Register.** A 16-bit register that counts UAS.
SR	00100	R	Yes	**Status Register.** An 8-bit register that reports alarm conditions.

NOTE: All registers marked with an asterisk are nonvolatile.

FDL REGISTER SUMMARY Table 3

Name	Addr	R/W	Clearable	Description
PRMR0 **PRMR1** **PRMR2** **PRMR3**	10000 10001 10010 10011	R R R R	No No No No	**Performance Report Message Registers.** Four 8-bit registers that contain the PRMs that were received in the FDL in the last four seconds.
RUMR	11000	R	No	**Receive Unscheduled Message Register.** An 8-bit register that reports unscheduled messages as they are received.
TUMR	11001	W	No	**Transmit Unscheduled Message Register.** An 8-bit register that is used to send unscheduled messages.
PRMESR*	11100	R	Yes	**PRM Errored Second Register.** A 16-bit register that counts ES as reported in the PRM.
PRMSESR*	11101	R	Yes	**PRM Severely Errored Second Register.** A 16-bit register that counts SES as reported in the PRM.
PRMER*	11110	R	Yes	**PRM Error Register.** An 8-bit register that counts PRMs that are received in error.

NOTE: All registers marked with an asterisk are nonvolatile.

USER REGISTER SUMMARY Table 4

Name	Addr	R/W	Clearable	Description
UBR	10100	W	No	**User Bit Register.** A 8-bit register that sets the position of the six available user bits.

NOTE: All of the registers in the DS2282 that count events will saturate at their maximum possible count; they do not roll over. For example, all the 16-bit registers stop at a count of 65,535. They do not roll over to zero and continue counting.

MONITOR REGISTERS

There are two sets of monitor registers. The first set helps support some of the monitoring requirements on T1 lines as spelled out in documents such as TA-TSY-000147 (DS1 Rate Digital Service Monitoring Unit Functional Specifications - October 1987), TR 62411 (Accunet* T1.5 Service Description and Interface Specifications - December 1988), and the CCITT recommendation G.821. This set consists of three registers, the Errored Second Register (ESR), the Severely Errored Second Register (SESR), and the Unavailable Seconds Register (UASR). Unlike the first set of monitor registers which provide a count of conditioned data, the second set of monitor registers just provide raw data counts of events such as CRC-6 errors, bipolar violations, frame errors, and out of frame errors. The second set of monitor registers consists of four registers, the CRC Count Register (CRCCR), the Bipolar Violation Count Register (BPVCR), the Frame Error Count Register (FECR), and the Out Of Frame Count Register (OOFCR). All of the monitor registers are described below.

ESR: Errored Second Register

A 16-bit register that counts Errored Seconds (ES). An ES is any one-second time interval with either a frame bit error or CRC-6 error.

SESR: Severely Errored Second Register

A 16-bit register that counts Severely Errored Seconds (SES). A SES is any one-second time interval with an OOF error event and/or more than 320 CRC-6 errors in it.

UASR: Unavailable Seconds Register

A 16-bit register that counts Unavailable Seconds (UAS). A UAS is the number of seconds between 10 consecutive SES events (inclusive) and 10 consecutive non-SES events (exclusive). The DS2282 starts counting SES events when it receives the first one. If it counts ten SESs in a row, then it increments the UASR by ten and decrements the ES and SES by ten. Counts in the ESR and SESR are inhibited during unavailable seconds. Once the DS2282 has begun counting unavailable seconds, it begins counting non-SES events. At the first non-SES event, it begins counting Errored Seconds in a separate register that is not available to the user. If the DS2282 fails to count ten non-SES events in a row, it clears both the non-SES count and the register counting Errored Seconds during unavailable seconds. If it counts ten non-SES events in a row, it will decrement the UASR by ten and will increment the ESR by the count in the register counting Errored Seconds during unavailable seconds. Also, when the DS2282 detects either an incoming Alarm Indication Signal (AIS) or Receive Carrier Loss (RCL), it will increment the UASR for each second during which either of these conditions exists.

CRCCR: CRC-6 Error Count Register.

A 16-bit register that records CRC-6 error events. The DS2282 calculates CRC-6 on the incoming data. Each time the calculation does not match the CRC-6 code word in the incoming ESF data stream, the CRCCR is incremented by one.

BPVCR: Bipolar Violation Count Register

A 24-bit register that records bipolar violations (line code violations). Bipolar violations are counted whether the synchronizer in the DS2282 is in sync (the RLOS signal is low) or not. If the DS2282 is set up to receive B8ZS code words, B8ZS code words are not counted as bipolar violations.

FECR: Frame Error Count Register

A 16-bit register that records errors in the Framing Pattern Sequence (FPS). All individual bit errors in the FPS pattern (001011) are recorded in the FECR.

OOFCR: Out Of Frame Count Register

A 16-bit register that records Out Of Frame (OOF) error events. An OOF error event occurs whenever two or more framing bits of out six in the FPS are incorrect. An OOF error event will cause the DS2282 to resynchronize to the incoming data stream.

Alarm and Event Indication

The Status Register (SR) reports alarms and events. The SR is always cleared when it is read by an external controller, hence the Clear Bit in the Register Byte does not need to be set. All of the bits in the SR operate in a "latched" fashion. That is, once an event or alarm has occured, the appropriate bit in the SR will remain set until the SR is read. All of the bits in the SR will be cleared when read unless the alarm condition still exists. Also, the INT\ pin will be asserted (transitions low) indicating to an external controller that a bit in the SR has changed status. The INT\ pin will return high as soon as the serial port is accessed.

SR: Status Register

(MSB)							(LSB)
PLB	LLB	16ZD	RCL	RYEL	RLOS	B8ZSD	AIS

PLB	**Payload Loopback.** Set when payload loopback is active.
LLB	**Line Loopback.** Set when line loopback is active.
16ZD	**Sixteen Zero Detect.** Set when 16 consecutive zeros are received. An indication of a pulse density violation.
RCL	**Receive Carrier Loss.** Set when 192 consecutive zeros have been received.
RYEL	**Receive Yellow Alarm.** Set when 16 consecutive 00FF Hex codes have been received in the FDL.
RLOS	**Receive Loss of Sync.** Set when the DS2282 loses synchronization.
B8ZSD	**B8ZS Detect.** Set when a B8ZS code word is received; operates whether the DS2282 is set up for B8ZS or not.
AIS	**Alarm Indication Signal.** Set when less than 3 zeros over two consecutive frames have been received (F-bits are not tested).

FDL REGISTERS

RECEIVE PRM OPERATION

The DS2282 decodes the incoming FDL for scheduled Performance Report Messages (PRM). It automatically detects opening flags, deletes any stuffed zero bits that may be present, and it calculates CRC-16 on all the data between the opening and closing flags. The DS2282 normally only decodes the current second's data (octets 5 and 6). Data from the previous three seconds is bumped from PRMR0 to PRMR1 to PRMR2 to PRMR3 and finally out of available recall range. If the PRM is received in error (CRC check sum is incorrect), the message will be ignored. The DS2282 will keep track of errored PRMs and properly place the unerrored message when it is received. For example, if a PRM is received that does not correspond to its CRC check sum, then PRMR0 will be set to all zeros indicating that an invalid message was received. If the next scheduled message is received correctly, then the data missed in the last scheduled message will be updated to PRMR1. NOTE: PRMR0 to PRMR3 are only updated if PRMs are received.

PRMR0: PRM Register 0
PRMR1: PRM Register 1
PRMR2: PRM Register 2
PRMR3: PRM Register 3

(MSB)							(LSB)
PLB	SL	LV	SE	FE	CRC2	CRC1	CRC0

PLB	Payload Loopback Activated
SL	Controlled Slip (slip >= 1)
LV	Line Violation (BPV >= 1)
SE	Severely Errored Framing Event (2 of 6 OOF >= 1)
FE	Frame Sync Bit Error Event
CRC2	See Table Below
CRC1	See Table Below
CRC0	See Table Below

CRC2	CRC1	CRC0	Event
0	0	0	Invalid
0	0	1	CRC = 0
0	1	0	CRC = 1 (G1)
0	1	1	1 < CRC <= 5 (G2)
1	0	0	5 < CRC <= 10 (G3)
1	0	1	10 < CRC <= 100 (G4)
1	1	0	100 < CRC <= 319 (G5)
1	1	1	CRC >= 320 (G6)

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PRM HISTORY REGISTERS

There are three registers that keep track of the scheduled PRM and collect data on the receive performance of the remote end. The first two of these registers (PRMESR and PRMSESR) mock the monitor registers in the type of data that they report. ES and SES are calculated off of the received PRM data. The PRM data is pulled from PRMR3 since it has the highest probability of containing valid data. If PRMR3 does not contain valid data, then ES and SES are not calculated. The third register (PRMER) keeps a count of how many PRMs have been received in error.

PRMESR: PRM Errored Second Register

A 16-bit register that counts Errored Seconds (ES). An ES is any one-second time interval with either a frame bit error (FE or SE = 1) or CRC-6 error (G1 to G6 = 1).

PRMSESR: PRM Severely Errored Second Register

A 16-bit register that counts Severely Errored Seconds (SES). A SES is any one-second time interval with an OOF error event (SE = 1) or more than 320 CRC-6 error events (G6 = 1).

PRMER: PRM Error Register

A 8-bit register that records the number of PRMs that have been received in error. A PRM is considered to be received in error when the calculated CRC does not match the incoming CRC word.

TRANSMIT PRM OPERATION

The DS2282 will automatically generate PRMs once a second to be included into the FDL for transmission to the remote end. It automatically pulls together all the necessary data to create a PRM from both the monitor registers and from the SLIP\ signal. It creates the opening and

closing flags as well as the address and control bytes. Once the PRM packet has been assembled, the DS2282 will generate CRC-16 and include it at the end of the PRM. And finally, before the PRM is sent, zeros are inserted to ensure that none of the PRM data appears as a flag.

RECEIVE UNSCHEDULED MESSAGE OPERATION

The DS2282 decodes incoming unscheduled messages as they are received. The DS2282 will report the received unscheduled message via the RUMR when the message has been received on 10 consecutive occasions. The RUMR is cleared when read via the serial port. Also, the INT\ pin will be asserted (transitions low) indicating to an external controller that an unscheduled message has been received. The INT\ pin will return high as soon as the serial port is accessed.

Two output signals on the DS2282 will respond to certain unscheduled messages. The PLB (Payload Loopback) signal will transition high if the code word for payload loopback activate (001010) is received ten times. It will remain high until the DS2282 has received the payload loopback deactivate code word (011001) ten times. The LLB (Line Loopback) signal operates similarly. The LLB signal will transition high when the DS2282 has received the code word for line loopback activate (000111) ten times. It will remain high until the DS2282 has received the code word for line loopback deactivate (011100) ten times.

RUMR: Receive Unscheduled Message Register

(MSB)							(LSB)
NA	NA	CW5	CW4	CW3	CW2	CW1	CW0

NA	Not Assigned. Could be any value when read.
NA	Not Assigned. Could be any value when read.
CW5	MSB of the Receive Unscheduled Message Codeword.
CW0	LSB of the Receive Unscheduled Message Codeword.

TRANSMIT UNSCHEDULED MESSAGE OPERATION

The DS2282 will transmit outgoing unscheduled messages. The DS2282 will continuously transmit the unscheduled message described in TUMR if enabled via the TUM bit in the TUMR. If unscheduled messages are being transmitted, all PRMs are superseded.

TUMR: Transmit Unscheduled Message Register

(MSB)							(LSB)
TUM	0	CW5	CW4	CW3	CW2	CW1	CW0

TUM	Transmit Unscheduled Message Enable.
CW5	MSB of the Transmit Unscheduled Message Codeword.
CW0	LSB of the Transmit Unscheduled Message Codeword.

USER REGISTER

The DS2282 contains a 6-bit user port. An external controller can independently set or clear these user bits via the User Bit Register (UBR).

UBR: User Bit Register

(MSB)							(LSB)
B8ZS	0	UB6	UB5	UB4	UB3	UB2	UB1

B8ZS	B8ZS Select. Logically OR'ed with the B8ZS signal.
UB6	User Bit 6. Sets or clears the UB6 pin.
UB5	User Bit 6. Sets or clears the UB5 pin.
UB4	User Bit 6. Sets or clears the UB4 pin.
UB3	User Bit 6. Sets or clears the UB3 pin.
UB2	User Bit 6. Sets or clears the UB2 pin.
UB1	User Bit 6. Sets or clears the UB1 pin.

INITIALIZING THE ADDRESS OF THE SERIAL PORT

The serial port on the DS2282 can be assigned an address from 0 to 30 decimal. Address location 31 decimal is reserved and should not be used. The default address is 0 decimal. The DS2282 is shipped from the factory with the default value in place. The address can be programmed in the following manner:

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1. Power down the DS2282.
2. Pull the Program Address Select pin high.
3. Configure the User Bits 1 to 5 with the desired address; UB1 is the LSB, UB5 is the MSB.
4. Leave all other pins open.
5. Apply power to the DS2282 for at least 1 second.
6. Power down the DS2282.

At this point, the DS2282 will be programmed to the proper value. Assigning a new address value can performed with the same procedure. The address value is stored in nonvolatile memory.

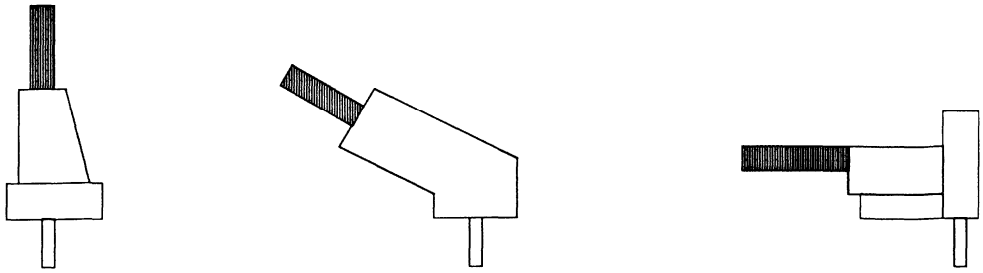
NONVOLATILE STORAGE

The DS2282 can retain its onboard program and the contents of the nonvolatile registers for at least ten years in the absence of power.

SINGLE IN-LINE CONNECTOR

The DS2282 is designed to connect directly into a 30-position Single In-Line connector. These connectors are available from a number of vendors in a variety of different configurations. There are vertical, inclined, and right angle connectors. See Figure 3. Table 5 lists the various vendors and the associated part numbers.

SINGLE IN-LINE CONNECTOR SCHEMES Figure 3



SINGLE IN-LINE CONNECTOR VENDORS Table 5

Connector	AMP	MOLEX	DALLAS
30-position vertical	821828-2	15-46-0780	DS9071-30V
30-position inclined	821876-2	15-46-0380	DS9071-30I
30-position right angle	NA	15-46-0450	NA

APPLICATION NOTE: FDL MESSAGE OVERVIEW

The Facility Data Link (FDL) on all Extended SuperFrame (ESF) channels must support two distinct message formats as per Section 4.3 in the Bellcore Document TR-TSY-000194 published December 1987. The first is a Scheduled Performance Report Message (PRM) that is to be sent once a second using a subset of the standard LAPD protocol. The PRM contains information on the receiving performance of the terminal that is sending the DS1 signal. The second message format is an Unscheduled Message which consists of a group of repeated 16-bit codewords. Unscheduled Messages contain information of the current status of the T1 line.

Performance Report Messages

The PRM must be sent once a second through the FDL. The transmission of the PRM does not have to be synchronous with any particular event but it must be on regular, precise intervals of one second. The PRM contains range indicators for CRC-6 error events and yes/no indications of the following:

- activated payload loopback
- frame synchronization bit error event
- out of frame (OOF) error event
- bipolar violation (BPV) error event
- controlled slip

The format of the PRM conforms to the Link Access Procedure for the D channel (LAPD) as described in the CCITT document Q.921. The PRM conforms to the unnumbered, unacknowledged format of this protocol. Each PRM contains performance information for the last four consecutive seconds. The format of the PRM is shown in Figure A1.

PRM FORMAT Figure A1

Octet Number		Bit Number 8	7	6	5	4	3	2	1
1	(opening flag)	0	1	1	1	1	1	1	0
2	(address)	0	0	1	1	1	0	C/R	0
3	(address)	0	0	0	0	0	0	0	1
4	(control byte)	0	0	0	0	0	0	1	1
5	(ASB for	G3	LV	G4	U1	U2	G5	SL	G6
6	time t0)	FE	SE	LB	G1	R	G2	Nm	NI
7	(ASB for	G3	LV	G4	U1	U2	G5	SL	G6
8	time t0 - 1)	FE	SE	LB	G1	R	G2	Nm	NI
9	(ASB for	G3	LV	G4	U1	U2	G5	SL	G6
10	time t0 - 2)	FE	SE	LB	G1	R	G2	Nm	NI
11	(ASB for	G3	LV	G4	U1	U2	G5	SL	G6
12	time t0 - 3)	FE	SE	LB	G1	R	G2	Nm	NI
13	(CRC-16 frame								msb
14	check sum)	lsb							
15	(closing flag)	0	1	1	1	1	1	1	0

Bit 1 of Octet 1 is transmitted first and received first. Each PRM contains 120 bits (8 bits/octet times 15 octets) and will take at least 30ms to transmit (120 bits times 250 microseconds/bit). The C/R bit in octet 2 should be set to zero since the originating equipment is DTE. If the source had been a T1 carrier, the C/R bit would be set to a one. The Application Specific Bits (ASB) in octets 5 through 12 are described in Figure A2.

KEY FOR APPLICATION SPECIFIC BITS (ASB) Figure A2

G1 = 1	CRC Error Event = 1
G2 = 1	1 < CRC Error Event <= 5
G3 = 1	5 < CRC Error Event <= 10
G4 = 1	10 < CRC Error Event <=100
G5 = 1	100 < CRC Error Event <= 319
G6 = 1	CRC Error Event >= 320
SE = 1	Severly Errored Framing Event or OOF >= 1 (FE shall = 0)
FE = 1	Frame Synchronization Bit Error Event >= 1 (SE shall = 0)
LV = 1	Line Code Violation Event or BPV >= 1
SL = 1	Controlled Slip >= 1
LB = 1	Payload Loopback is currently activated
R = 0	Reserved (default value is 0)
Nm,Nl	Modulus 4 counter (00/01/10/11)
U1,U2 = 0	Undefined (should be set to 0)

Unscheduled Message

An Unscheduled (bit-oriented) Message is a repeating 16-bit pattern of the form:

0XXXXXX0 11111111

where the six X-bits create 64 unique codewords as shown in Figure A3. Only the codewords currently defined are listed in Figure A3. Priority messages must be repeated for a minimum of one second while Command and Response Messages need only be repeated a minimum of ten times.

UNSCHEDULED MESSAGE FORMAT Figure A3

Priority Messages	**Codeword**	
Yellow Alarm	0 000000 0	11111111
Reserved for network use	0 001110 0	11111111
Reserved for network use	0 010110 0	11111111
Reserved for network use	0 011010 0	11111111
Command and Response Messages		
Line Loopback Activate	0 000111 0	11111111
Line Loopback Deactivate	0 011100 0	11111111
Payload Loopback Activate	0 001010 0	11111111
Payload Loopback Deactivate	0 011001 0	11111111
Network Loopback Activate	0 001001 0	11111111
Network Loopback Deactivate	0 010010 0	11111111
Protection Switch Line 1	0 100001 0	11111111
Protection Switch Line 2	0 100010 0	11111111
Protection Switch Line 26	0 111010 0	11111111
Protection Switch Line 27	0 111011 0	11111111
Protection Switch Acknowledge	0 001100 0	11111111
Protection Switch Release	0 010011 0	11111111
Reserved for network use	0 001101 0	11111111
Reserved for network use	0 001011 0	11111111
Reserved for network use	0 001111 0	11111111
Reserved for network use	0 011101 0	11111111
Reserved for network use	0 010101 0	11111111

Message Priorities
Unscheduled Messages always take precedence over any other communications that may be taking place in the FDL, which includes PRMs. Unscheduled Messages will interrupt any PRM that may be currently in progress because the first eight bits of each codeword are all ones which is an abort signal in the LAPD protocol. When the FDL is not being used to transmit either Unscheduled Messages or PRMs, the 8-bit idle code 01111110 should be sent repeatedly.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	0°C to 70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	VIH	2.0		Vcc+0.3	V	3
Logic 1 for RST	VIH	3.5		Vcc+0.3	V	
Logic 0	VIL	-0.3		+0.8	V	
Supply	VDD	4.50		5.50	V	

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CAPACITANCE (tA=25C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN		30		pF	
Output Capacitance	COUT		50		pF	

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	IDD		30		mA	1
Static Input Leakage	II	-50		+50	uA	2,3
Output Voltage (80uA)	VOH	2.4	4.8		V	
Output Voltage (1.6mA)	VOL		.15	.45	V	
RST Pull-Down Resistance	RPD	40		125	Kohm	

NOTES:
1. RCLK = 1.544MHz; VDD = 5.50V; outputs open; inputs tied low.
2. Vin = .45 Volts.
3. Does not apply to RST.

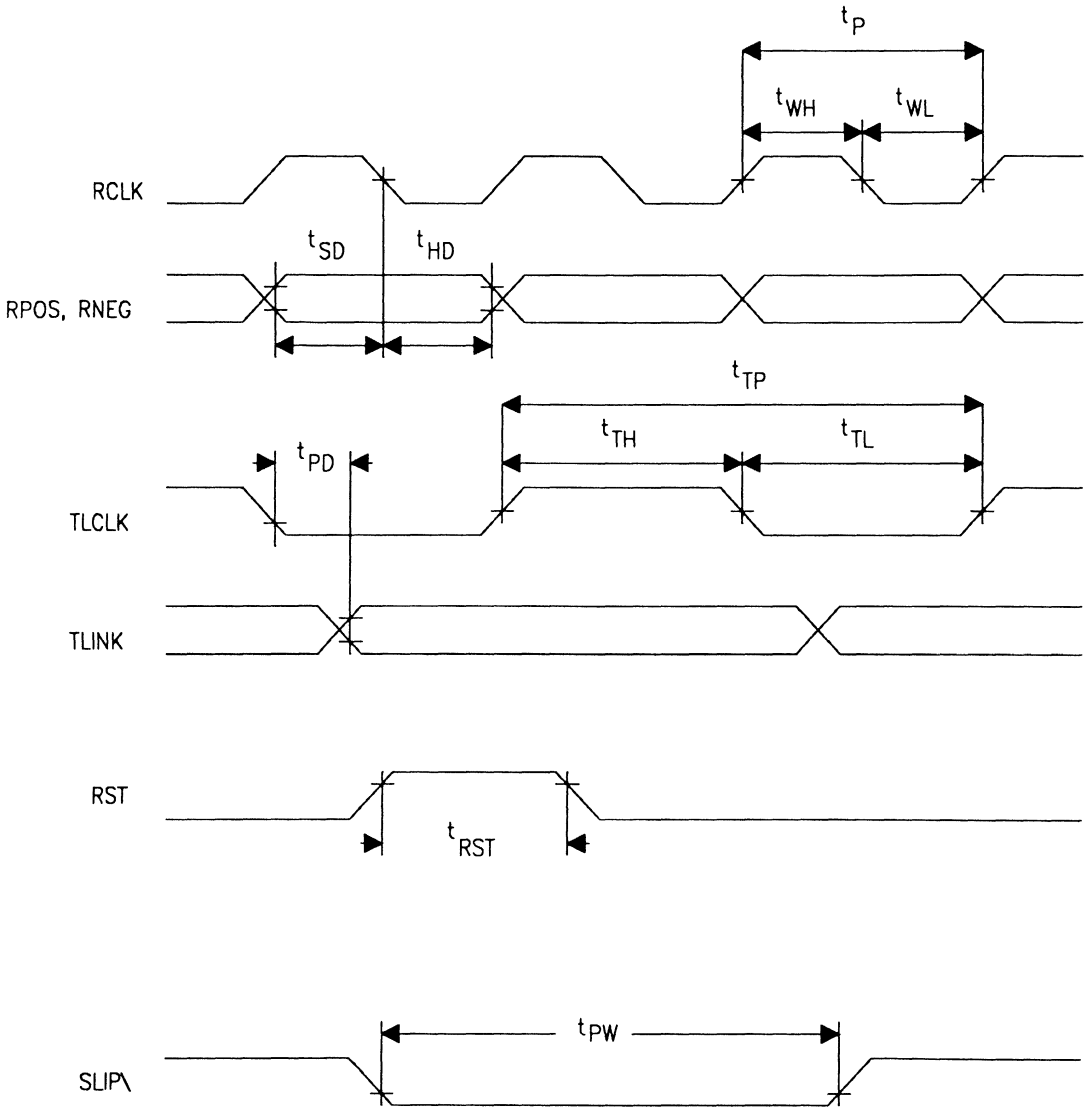
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{DD}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_P		648		ns	1
RCLK Pulse Width	t_{WH}, t_{WL}	100			ns	
RPOS, RNEG Setup to RCLK Falling	t_{SD}	50			ns	
RPOS, RNEG Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay From TLCLK Falling to TLINK Valid	t_{PD}			40	us	
TLCLK Period	t_{TP}		250		us	1
TLCLK Pulse Width	t_{TH}, t_{TL}	50			us	
RST Pulse Width	t_{RST}	10			us	
SLIP\ Pulse Width	t_{PW}	10			us	
Sync / Reframe Time				30	ms	2

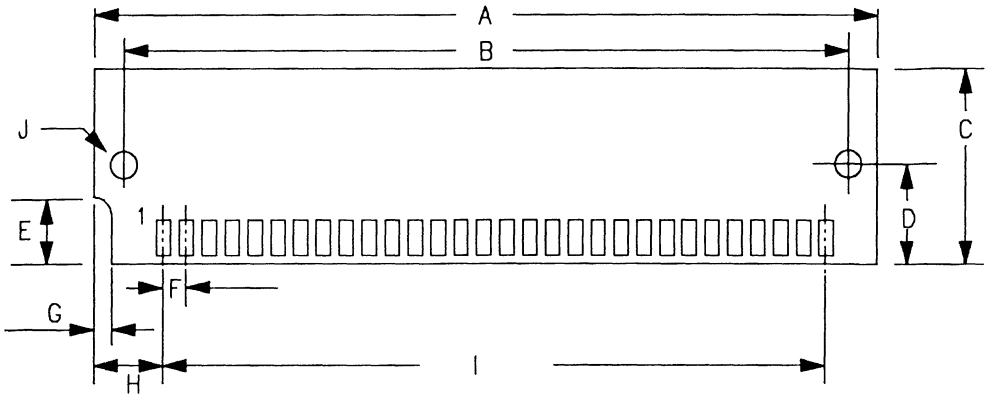
NOTES:

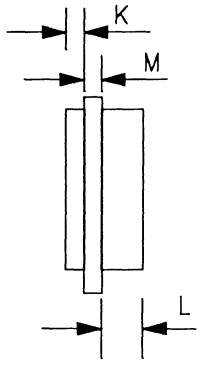
1. Must be accurate to +/-32ppm for precise one-second interval measurements.
2. Time necessary to sync to an error-free signal.

A.C. TIMING DIAGRAM Figure 4



DS2282
T1 FDL CONTROLLER/ MONITOR





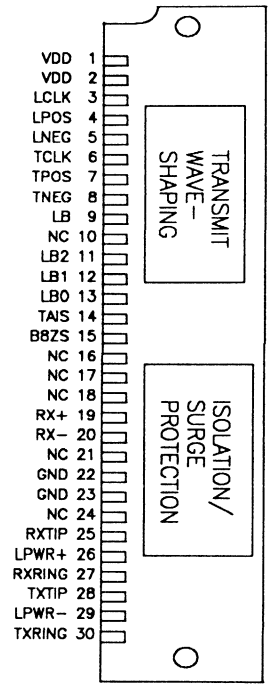
DIM	INCHES
A	3.500
B	3.234
C	0.850
D	0.400
E	0.250
F	0.100
G	0.080
H	0.300
I	2.900
J	0.125 DIA
K	0.150
L	0.175
M	0.050

DALLAS SEMICONDUCTOR

DS2290
T1 ISOLATION Stik™

FEATURES
- Protected interface for connecting equipment to T1 lines
- Provides 800 volts of surge protection and 1500 volts of isolation
- FCC Part 68 registered
- Meets TR 62411 and T1.403-1989 for transmit pulse characteristics
- Line Build Outs of 0dB, -7.5dB, and -15dB
- Companion to the DS2291 T1 Long Loop Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

Stik LAYOUT



(actual size)

DESCRIPTION
The DS2290 T1 Isolation Stik provides all the surge and isolation protection that is necessary in order to connect a piece of equipment to a T1 line. It offers a function similar to that provided by a Data Access Arrangement (DAA) when a modem is connected to a phone line. The DS2290 is FCC Part 68 pre-registered so the user can connect equipment to T1 lines without any further testing or qualification. It contains onboard waveshaping circuitry that will create transmit pulses that meet the latest T1 specifications including TR 62411 (Accunet* T1.5 Service Description and Interface Specifications - December 1988) and T1.403-1989 (Carrier to Carrier Installation - DS1 Metallic Interface). Applications include Channel Service Units and similar equipment that requires a fully protected interface.

OVERVIEW

The DS2290 contains all the isolation and surge protection required to connect equipment to T1 lines. The Isolation Stik has a receive and a transmit section. (See Figure 1.) In the receive section, inputs RXTIP and RXRING are connected directly to the receive T1 twisted pair. These inputs are terminated at 100 ohms. The T1 signal received at RXTIP and RXRING is coupled through a 2:1 transformer and presented at the RX+ and RX- outputs. See Figure 2. There is a full 1500 volts of isolation between the Network Side pins and the Customer Side pins.

In the transmit section, data that is to be transmitted is sourced from either the TPOS and TNEG inputs or the LPOS and LNEG inputs. The Data Mux will transmit data at the TCLK rate from the TPOS and TNEG inputs if the LB pin is either tied low or left open. It will transmit data at the LCLK rate from the LPOS and LNEG inputs if the LB pin is tied high. In order to comply with the latest T1 standards, the clock presented at either TCLK or LCLK must be at a 1.544MHz rate (+/- 32ppm) and must not jitter beyond 0.05 unit intervals peak-to-peak (UIpp). TPOS and TNEG can be tied together if the source of the transmit data is in a NRZ format. The DS2290 will automatically sense that these inputs are tied together and will create a bipolar data stream from them. The same holds true for the LPOS and LNEG inputs.

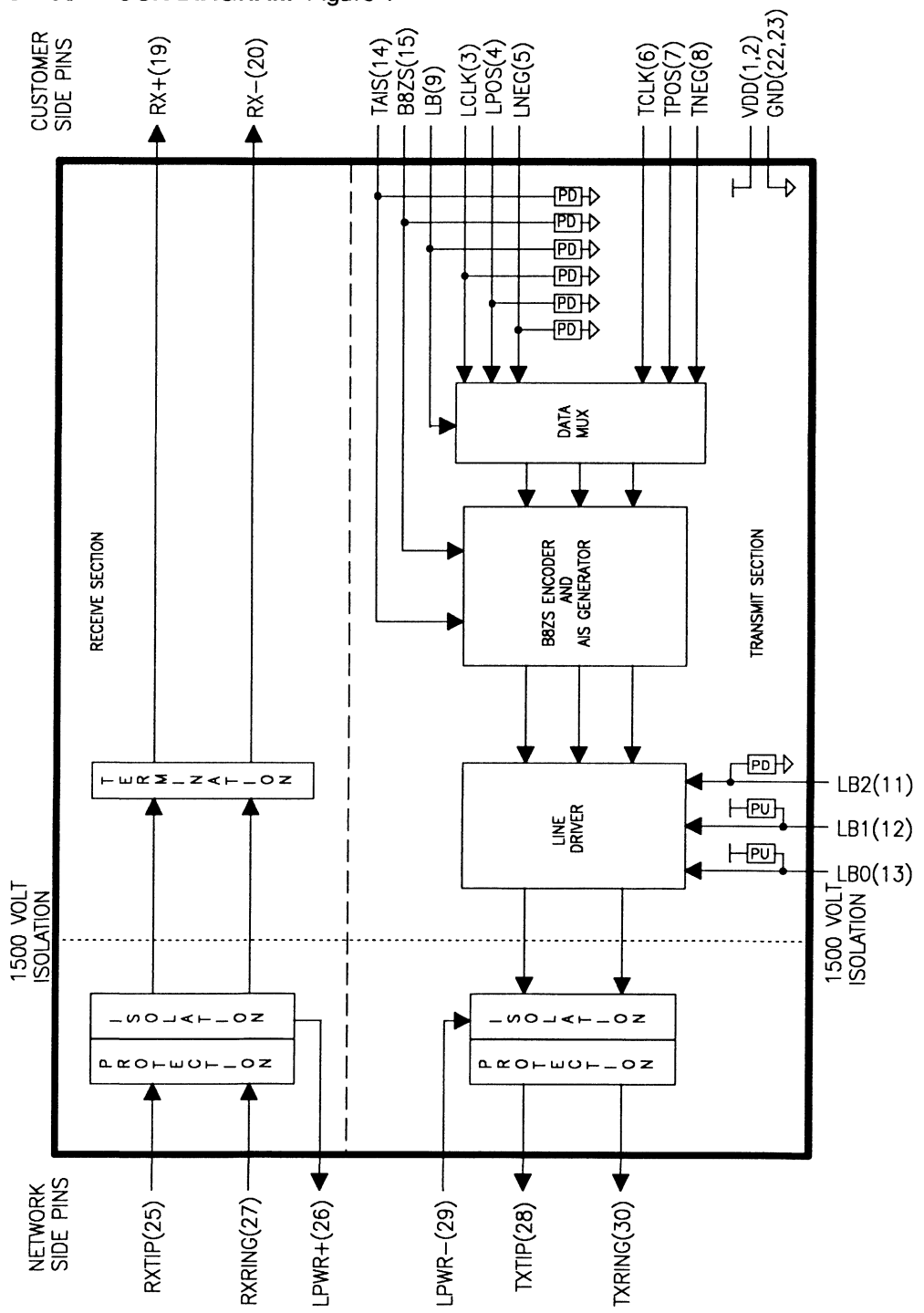
Data out of the Data Mux is passed to a B8ZS encoder and AIS generator. If the B8ZS pin is tied high, then the DS2290 will properly encode the transmit data stream for the B8ZS zero code suppression scheme. If the B8ZS pin is tied low or left open, the DS2290 will not encode the transmit data for B8ZS. Also, the DS2290 can be configured to transmit an AIS (Alarm Indication Signal). If the TAIS pin is tied high, the DS2290 will transmit an unframed, all ones signal at either the TCLK (LB = 0) or LCLK (LB = 1) rate.

The data to be transmitted is fed to the line driver. The line driver creates the T1 pulse that will be transmitted. The line build out pins LB0 to LB2 select whether the output pulse level will be 0dB, -7.5dB, or -15dB. If 0dB of build out is selected, the output pulse will conform to the shape described in Figure 2. This pulse shape is congruent with the latest T1 specifications such as TR 62411 and T1.403-1989. If the -7.5dB or -15dB line build outs are selected, then the pulse shown in Figure 3 will be attenuated according to the transfer function as described in FCC Part 68, Subpart D. Once the T1 pulse has been created, it is then transmitted onto the transmit T1 twisted pair via the TTIP and TRING outputs.

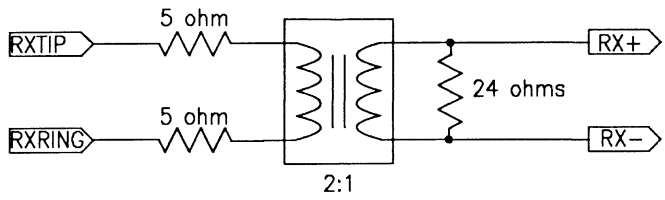
The DS2290 contains provisions for line powering. If the DS2290 is to be powered from the T1 line using a DC simplex power arrangement, then an external DC-to-DC converter can connected to the LPWR+ and LPWR- pins. Requirements for line powering are currently being relaxed and will be totally removed in the future. If the DS2290 is not line powered, the LPWR+ and LPWR- pins should be tied together.

Figure 4 shows a typical application using the DS2290. The transmit and receive T1 twisted pairs are connected directly to the DS2290. The DS2291 T1 Long Loop Stik recovers clock and data from the protected signal provided by the Isolation Stik. The DS2180A T1 Transceiver frames to the recovered data and interfaces to the system backplane. The DS2250 Soft Microcontroller Stik is used to control and monitor the status of the other devices.

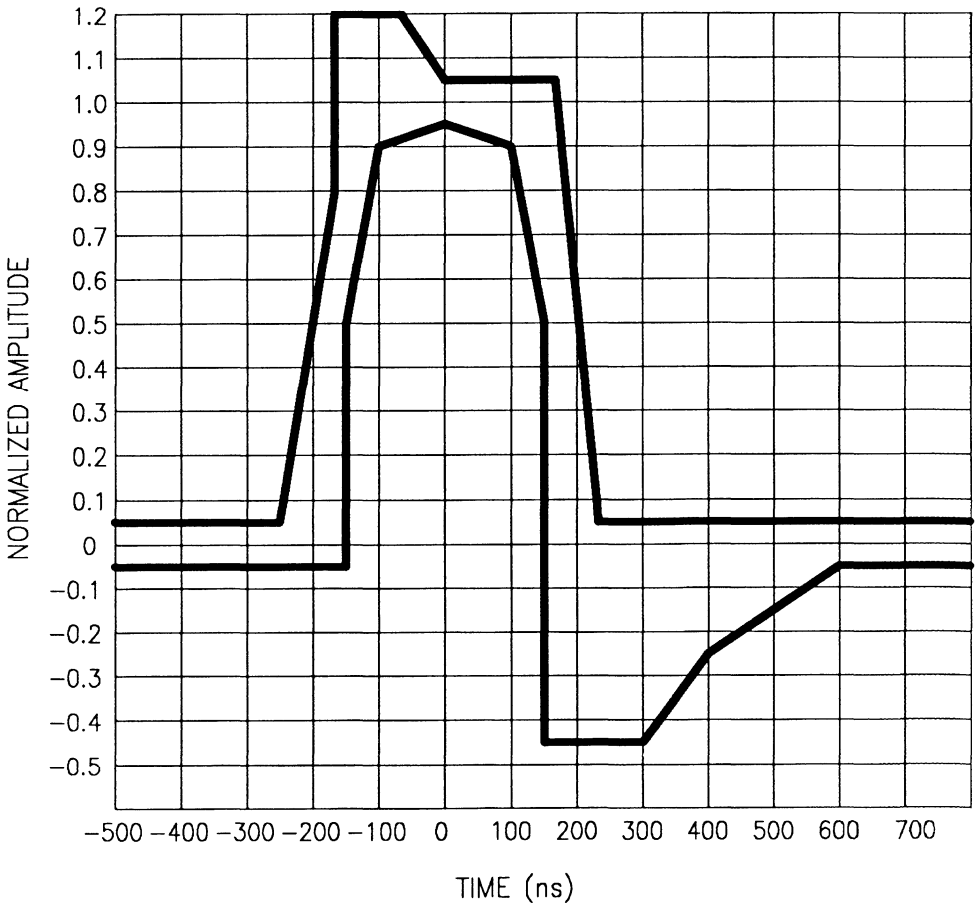
DS2290 BLOCK DIAGRAM Figure 1



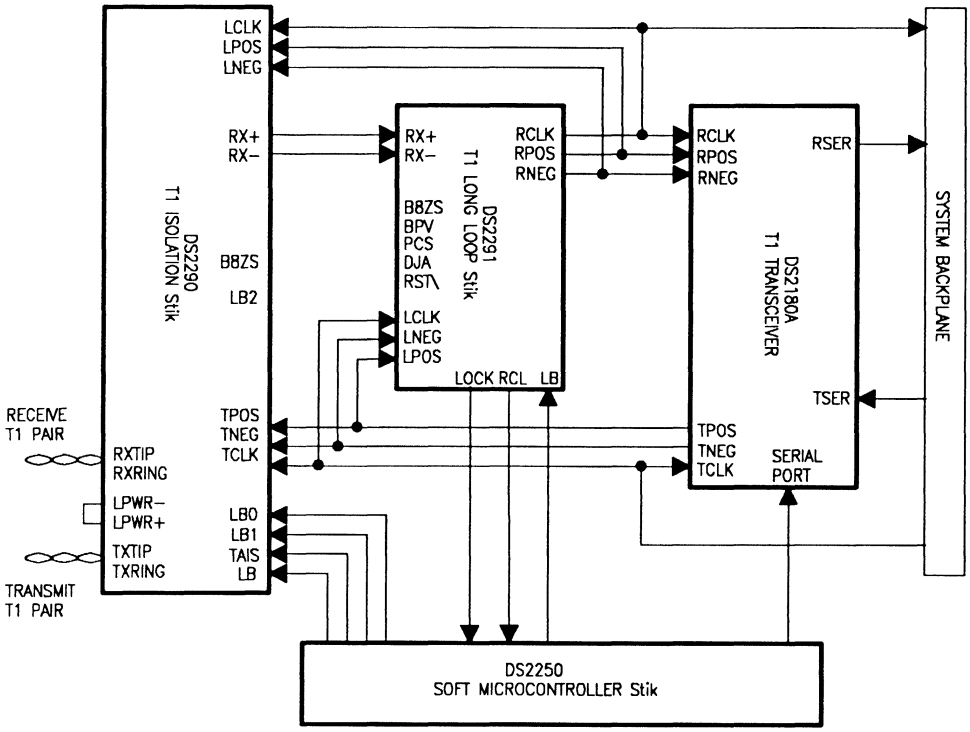
DS2290 RECEIVE SECTION CIRCUITRY Figure 2



OUTPUT PULSE TEMPLATE Figure 3



TYPICAL DS2290 APPLICATION Figure 4



NETWORK SIDE PIN DESCRIPTION Table 1

PIN	SYMBOL	I/O	DESCRIPTION
25 27	**RXTIP** **RXRING**	I	**Receive Tip and Ring Inputs.** Connects directly to the receive T1 twisted pair. These inputs are transformer coupled and terminated at 100 ohms. See Figure 2.
28 30	**TXTIP** **TXRING**	O	**Transmit Tip and Ring Outputs.** Connects directly to the transmit T1 twisted pair. Output signal level is programmable via the LB0 to LB2 pins.
26 29	**LPWR+** **LPWR-**	-	**Loop Power Connections.** These pins connect to the internal center-taps of the transmit and receive transformers. They provide access to the DC power on the T1 line (may not be provided by carriers in the future). Tie together if no simplex power arrangement is needed.

CUSTOMER SIDE PIN DESCRIPTION Table 2

PIN	SYMBOL	I/O	DESCRIPTION
1,2	**VDD**	-	**Positive Supply.** 5.0 Volts.
3	**LCLK**	I	**Loopback Clock.** Clock for loopback data. Internally pulled low by 100K ohm.
4 5	**LPOS** **LNEG**	I	**Loopback Bipolar Data.** Sampled on the falling edge of LCLK if LB is tied high. Internally pulled low by 100K ohm.
6	**TCLK**	I	**Transmit Clock.** Apply a 1.544MHz (+/- 32ppm) clock here.
7 8	**TPOS** **TNEG**	I	**Transmit Bipolar Data.** Data that is to be transmitted. Sampled on the falling edge of TCLK when LB is tied low or left open. TPOS and TNEG can be tied together for an NRZ data input.
9	**LB**	I	**Loopback Enable.** Tie high to transmit data from LPOS and LNEG; tie low or leave open to transmit data from TPOS and TNEG. Internally pulled low by 100K ohm.
11 12 13	**LB2** **LB1** **LB0**	I	**Line Build Out Select.** State determines whether the transmitted signal has 0dB, -7.5dB, or -15dB of line build out. See Table 3. LB0 and LB1 are internally pulled high by 100K ohm; LB2 is pulled low by 100K ohm. If all three build out pins are left open, the default state is 0dB.
14	**TAIS**	I	**Transmit Alarm Indication Signal.** Tie high to transmit an unframed all ones signal at either the TCLK (LB = 0) or LCLK (LB = 1) rate. Internally pulled low by 100K ohm.
15	**B8ZS**	I	**B8ZS Enable.** Tie high to enable B8ZS encoding; tie low or leave open to disable B8ZS encoding. Internally pulled low by 100K ohm.
19 20	**RX+** **RX-**	O	**Receive Analog Output.** Protected differential T1 signal outputed here.
22,23	**GND**	-	**Ground.** 0.0 Volts.

NOTE: Do not connect any signal to pins 10, 16, 17, 18, 21, and 24.

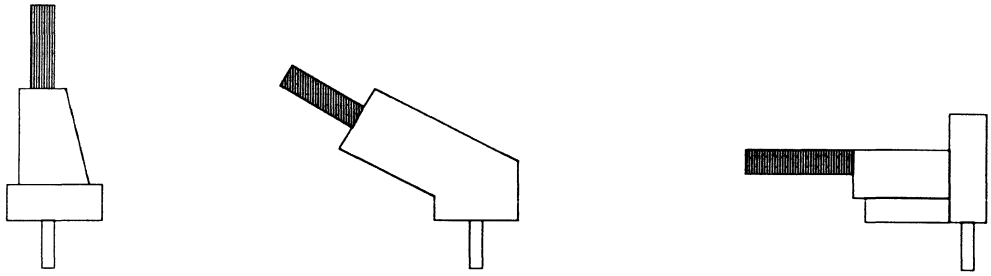
LINE BUILD OUT SELECTS Table 3

Line Build Out Selected	LB0	LB1	LB2
0dB	1	1	0
-7.5dB	1	0	0
-15dB	0	1	0

SINGLE IN-LINE CONNECTOR

The DS2290 is designed to connect directly into a 30-position single in-line connector. These connectors are available from a number of vendors in a variety of configurations. There are vertical, inclined, and right angle connectors. (See Figure 5.) Table 4 lists the various vendors and the associated part numbers.

SINGLE IN-LINE CONNECTOR SCHEMES Figure 5



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SINGLE IN-LINE CONNECTOR VENDORS Table 4

Connector	AMP	MOLEX	DALLAS
30-position vertical	821828-2	15-46-0780	DS9071-30V
30-position inclined	821876-2	15-46-0380	DS9071-30I
30-position right angle	NA	15-46-0450	NA

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground (Customer Side pins only)	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55C to +125C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	VIH	2.0		Vcc+0.3	V	3
Logic 0	VIL	-0.3		+0.8	V	3
Supply	VDD	4.75		5.25	V	

CAPACITANCE (tA=25C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Onput Capacitance	CIN		30		pF	3
Output Capacitance	COUT		50		pF	3

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{DD}=5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	IDD		40	50	mA	1
Input Leakage	II	-100		+100	uA	2,3
Output Current (2.4V)	IOH	-1.0			mA	3
Output Current (0.4V)	IOL	+4.0			mA	3

NOTES:

1. TCLK = 1.544MHz; VDD = 5.25V; outputs open; driving all ones into 6000 feet of 22 AWG.
2. VSS < Vin < VDD.
3. Does not apply to any of the network side pins nor RX+ or RX-.

ANALOG ELECTRICAL CHARACTERISTICS (0°C to 70°C; VDD=5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Impedance at RXTIP & RXRING at 772KHz	I_Z	95	100	105	ohms	1
Transmit Jitter Generation	J_{GEN}			0.03	UIpp	2
Transmit Pulse Amplitude	P_{AMP}	2.8	3.0	3.2	Vpk	3,4,5
Pulse Width Balance @ 50%	PW_{BAL}		1	10	ns	3,6
Pulse Amplitude Balance	PA_{BAL}		10	100	mV	3,6
Power Level at 772KHz	P_{LVL}	12		19	dBm	7

7

NOTES:

1. RX+ and RX- left open circuited.
2. Jitter present at TXTIP and TXRING with no jitter at TCLK (LB = 0) or LCLK (LB = 1).
3. Measured with 100 ohm (+/- 5%) termination at TXTIP and TXRING.
4. Measured directly at TXTIP and TXRING with 0dB of line build out.
5. Pulse shape meets template in Figure 3 over temperature and voltage.
6. Measured over 17 consecutive pulses.
7. Measured in a 2KHz to 3KHz band about 772KHz; power level in a 2 to 3 KHz band at 1.544MHz is at least 25dB lower.

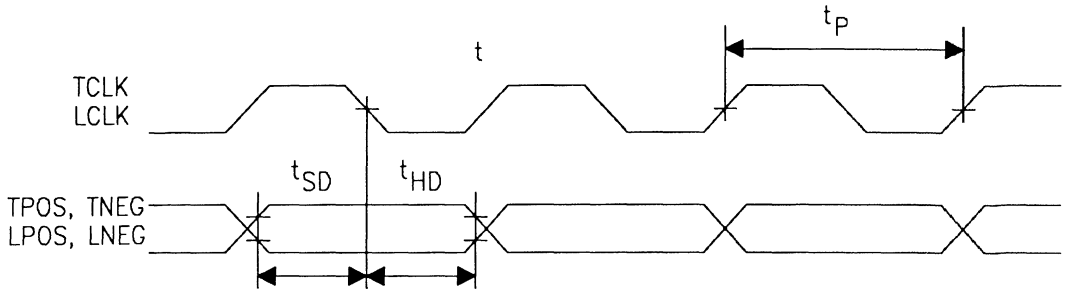
DIGITAL ELECTRICAL CHARACTERISTICS (0°C to 70°C; VDD=5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_P			+/-32	ppm	1
TPOS, TNEG or LPOS, LNEG Setup Time to TCLK or LCLK falling	t_{SD}	50			ns	
TPOS, TNEG or LPOS, LNEG Hold Time from TCLK or LCLK Falling	t_{HD}	50			ns	

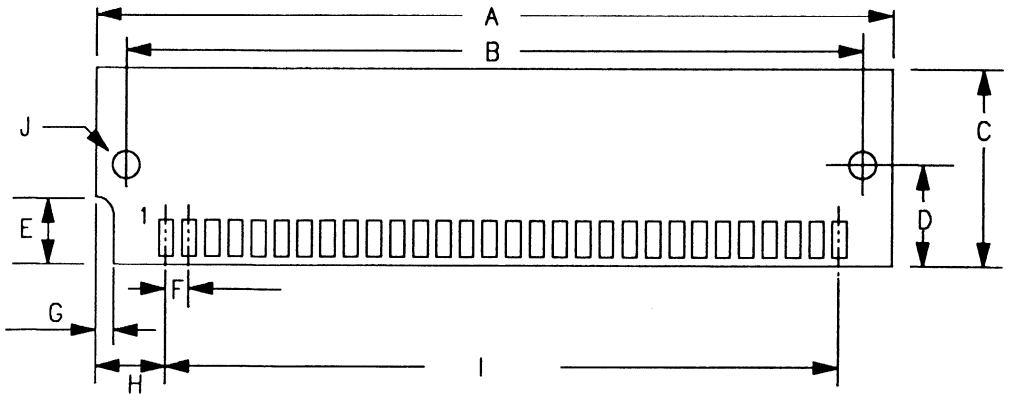
NOTES:

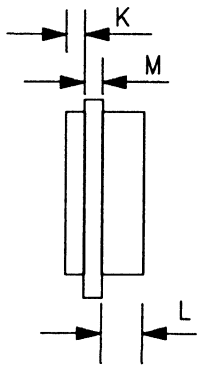
1. Necessary to meet current carrier and FCC specifications.

AC TIMING DIAGRAM Figure 6



DS2290
T1 ISOLATION Stik





DIM	INCHES
A	3.500
B	3.234
C	0.850
D	0.400
E	0.250
F	0.100
G	0.080
H	0.300
I	2.900
J	0.125 DIA
K	0.110
L	0.250
M	0.050

7

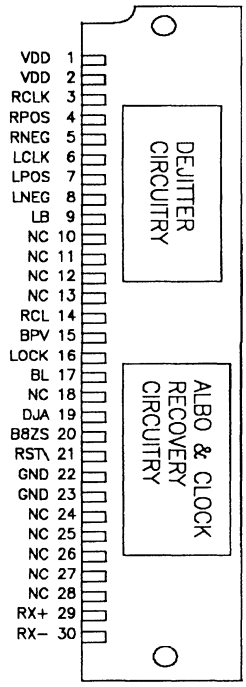
DALLAS SEMICONDUCTOR

DS2291
T1 LONG LOOP Stik™

FEATURES

- Recovers clock and data off of T1 lines from 0 to 6000 feet in length
- +0 to -30dBSX receive sensitivity
- Built-in Automatic Line Build Out (ALBO) circuitry; no tuning or external components required
- Dejitters the recovered clock and data
- Meets TR 62411 for jitter tolerance and attenuation
- Companion to the DS2290 T1 Isolation Stik
- Connects to a standard 30-pin single in-line connector
- Single +5V supply

Stik LAYOUT



(actual size)

DESCRIPTION

The DS2291 T1 Long Loop Stik contains all the circuitry necessary to recover clock and data off a T1 line. The DS2291 contains an Automatic Line Build Out (ALBO) circuit that allows it to adapt to T1 lines varying in length from 0 to 6000 feet. It also will dejitter the recovered clock and data according the jitter attenuation curves outlined in AT&T Communications Document TR 62411 (Accunet* T1.5 Service Description and Interface Specification - December 1988). Applications areas include Channel Service Units (CSU), T1 monitoring equipment, and T1 test equipment.

OVERVIEW

The DS2291 contains onboard ALBO circuitry that allows it to recover clock and data from T1 lines up to 6000 feet in length. (See Figure 1.) Unlike alternative methods of clock and data recovery from T1 lines, the DS2291 does not require any tuning, nor does it need any additional external circuitry. T1 signals applied at RX+ and RX- are equalized by the ALBO circuit before they are presented to the clock and data recovery circuitry. The state of the LOCK pin indicates whether the DS2291 has been able to phase and frequency lock to the incoming T1 signal. If the LOCK pin is high, the DS2291 is properly locked onto the incoming signal. The DS2291 meets the latest T1 specifications for jitter tolerance. The jitter tolerance curve in Figure 2 is applicable over the full dynamic input range of the DS2291.

Once the Long Loop Stik has recovered data off of the T1 line, it can decode B8ZS code words and it checks for bipolar violations and carrier loss. If the B8ZS pin is tied high, the DS2291 will automatically replace incoming B8ZS code words with eight zeros. If the B8ZS pin is tied low or left open, no replacement occurs. Bipolar violations are reported via the BPV pin. The BPV pin will transition high for a full T1 bit period (648ns) each time a violation is detected. Bipolar violations inherent in B8ZS code words are not reported if the B8ZS pin is tied high. The DS2291 also checks for carrier loss. The RCL pin will transition high when the DS2291 detects 192 consecutive zeros at RX+ and RX-.

The recovered clock and data is passed to the dejitter circuitry. If the DJA is tied low or left open, the DS2291 will attenuate the jitter present at RX+ and RX- according the curves outlined in Figure 3. These curves meet the latest T1 specifications. If the DJA pin is tied high, the DS2291 will not attenuate jitter. Hence, all the jitter inherent in the signal at RX+ and RX- will be passed to RCLK, RPOS, and RNEG. If the recovered clock at RCLK is used to transmit data onto T1 lines, it is recommended that the dejitter circuitry be enabled (DJA = 0). The dejitter circuitry contains a 128-bit buffer. This buffer can be recentered on command via the RST\ pin. In normal applications, the RST\ is left open or tied high. The Buffer Limit (BL) output will transition high when the DS2291 is receiving more than 120 unit intervals peak-to-peak (UIpp) of jitter at RX+ and RX-. As long as the incoming jitter is less than 120UIpp, the BL pin will remain low.

The DS2291 contains a data mux that allows data to be routed from either the T1 recovery circuitry or from a local source. The mux is helpful is locating faults in a system. For example, it could be used to implement a "local" loopback.

Two typical applications with the DS2291 are shown in Figures 4 and 5. In both applications, the DS2291 is used to recover data off of T1 lines up to 6000 feet in length. The application in Figure 4 is with an unprotected interface; it might be used in T1 test equipment. The application in Figure 5 is with the DS2290 T1 Isolation Stik, which provides all the necessary protection as required by FCC Part 68. This could be used in a Channel Serivce Unit (CSU) or in similar types of equipment in which full surge and isolation protection is required.

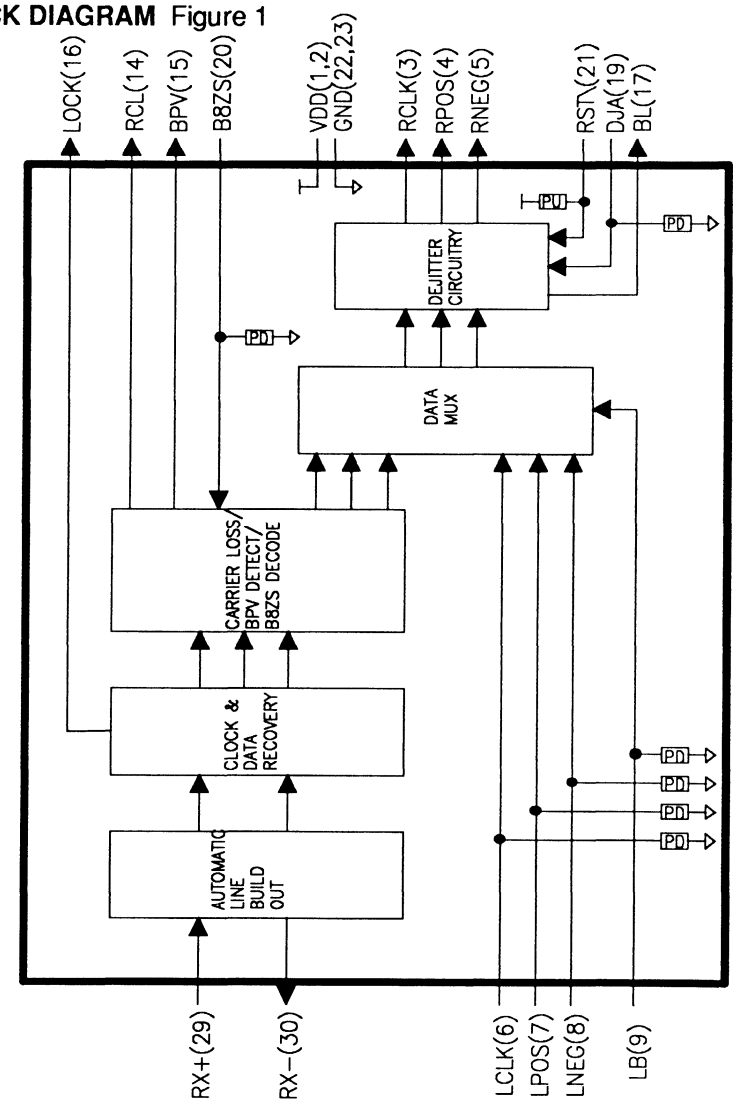
PIN DESCRIPTION Table 1

PIN	SYMBOL	I/O	DESCRIPTION
1,2	**VDD**	-	**Positive Supply.** 5.0 Volts.
3	**RCLK**	O	**Receive Clock.** Recovered 1.544MHz clock.
4 5	**RPOS** **RNEG**	O	**Receive Bipolar Data.** Recovered bipolar data; updated on the rising edge of RCLK. Bipolar violations are not corrected.
6	**LCLK**	I	**Loopback Clock.** Clock for loopback data. Internally pulled low by 100K ohm.
7 8	**LPOS** **LNEG**	I	**Loopback Bipolar Data.** Sampled on the falling edge of LCLK if LB is tied high. Internally pulled low by 100K ohm.
9	**LB**	I	**Loopback Enable.** Tie high to loopback data from the LPOS and LNEG inputs to RPOS and RNEG; tie low or leave open to obtain recovered data out of the ALBO circuitry at RPOS and RNEG. Internally pulled low by 100K ohm.
14	**RCL**	O	**Receive Carrier Loss.** Transitions high when 192 consecutive zeros have been received at RX+ and RX-; reset on the next ones occurrence.
15	**BPV**	O	**Receive Bipolar Violation.** Transistions high for a full bit period when a bipolar violation appears at RX+ and RX-. B8ZS code words are not reported if B8ZS is tied high.
16	**LOCK**	O	**Lock Indication.** High state indicates that the recovery circuit is phase-and frequency-locked to the signal at RX+ and RX-.
17	**BL**	O	**Buffer Limit.** Transitions high when the incoming jitter at RX+ and RX- is greater than 120UIpp.
19	**DJA**	I	**Disable Jitter Attenuation.** Tie high to disable the jitter attenuation circuitry; tie low to enable the jitter attenuation circuitry. Internally pulled low by 100K ohm.
20	**B8ZS**	I	**B8ZS Enable.** If tied high, incoming B8ZS code words are decoded and replaced with eight zeros. If tied low, B8ZS code words are not decoded. Internally pulled low by 100K ohm.

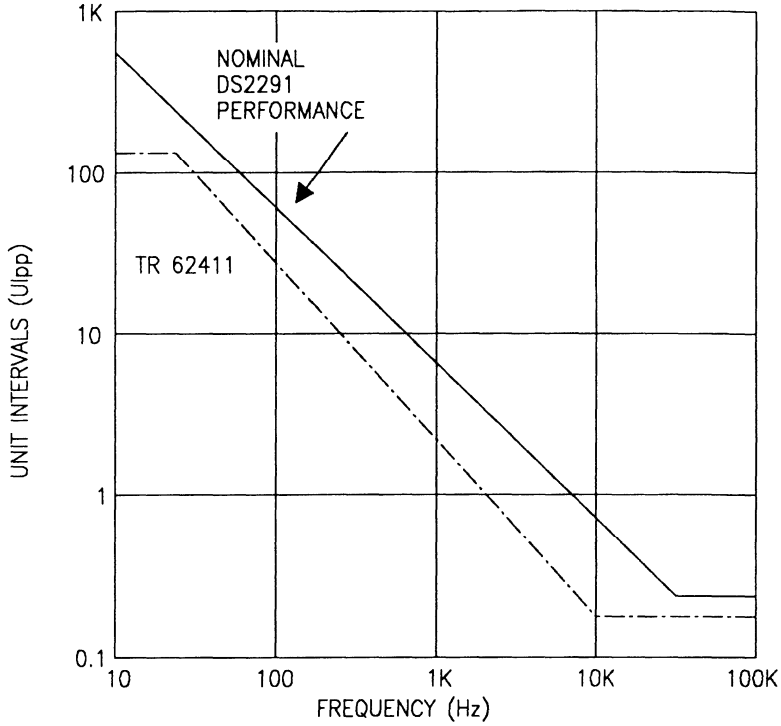
21	**RST**	I	**Reset.** Active low; a high-low-high transition will recenter the dejitter buffer. Internally pulled high by 100K ohm.
22,23	**GND**	-	**Ground.** 0.0 Volts.
29 30	**RX+** **RX-**	I O	**Receive Analog Input.** Connects to T1 line through a 2:1 transformer. See Figure 4.

NOTE:
Do not connect any signal to pins 10, 11, 12, 13, 18, 24, 25, 26, 27, or 28.

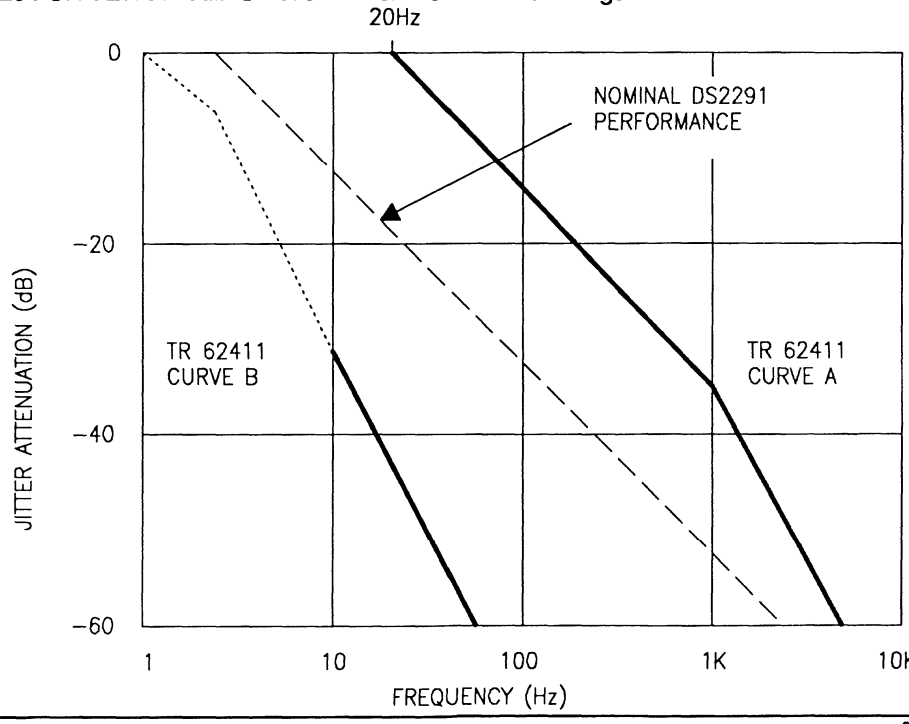
DS2291 BLOCK DIAGRAM Figure 1



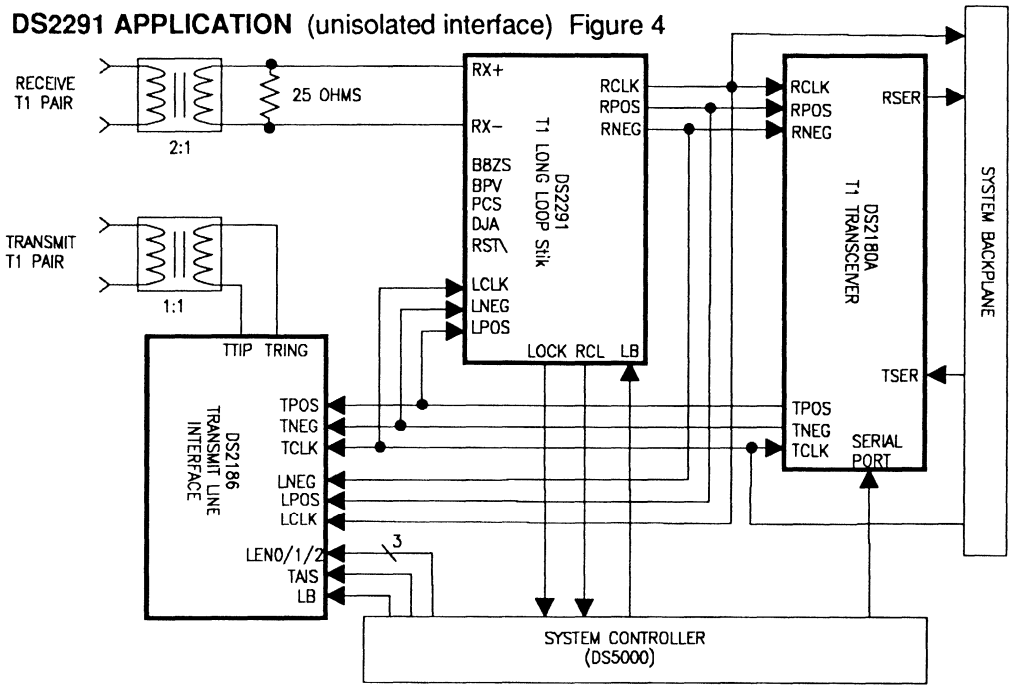
DS2291 JITTER TOLERANCE Figure 2



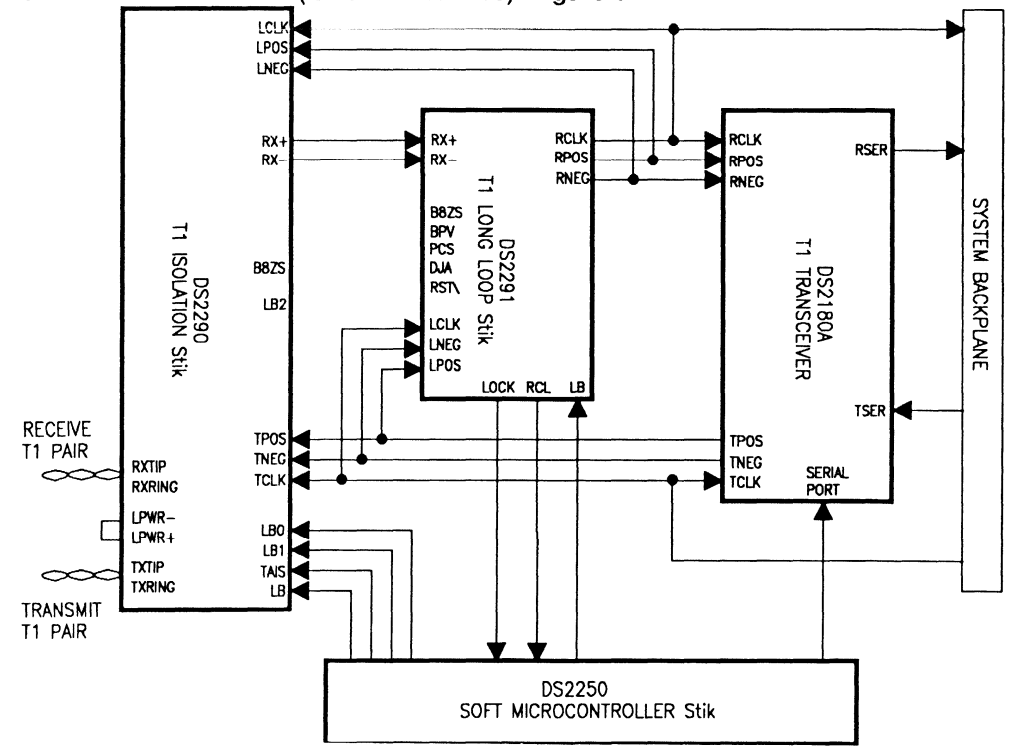
DS2291 JITTER ATTENUATION PERFORMANCE Figure 3



DS2291 APPLICATION (unisolated interface) Figure 4



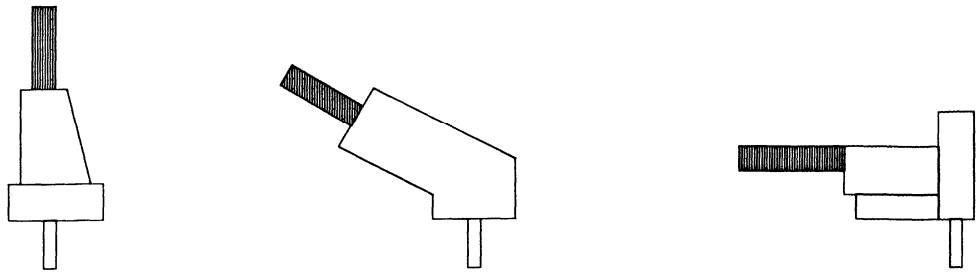
DS2291 APPLICATION (isolated interface) Figure 5



SINGLE IN-LINE CONNECTOR

The DS2291 is designed to connect directly into a 30-position single in-line connector. These connectors are available from a number of vendors in a variety of configurations. There are vertical, inclined, and right angle connectors. (See Figure 6.) Table 2 lists the various vendors and the associated part numbers.

SINGLE IN-LINE CONNECTOR SCHEMES Figure 6



SINGLE IN-LINE CONNECTOR VENDORS Table 2

Connector	AMP	MOLEX	DALLAS
30-position vertical	821828-2	15-46-0780	DS9071-30V
30-position inclined	821876-2	15-46-0380	DS9071-30I
30-position right angle	NA	15-46-0450	NA

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55C to +125C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	VIH	2.0		Vcc+0.3	V	3
Logic 0	VIL	-0.3		+0.8	V	3
Supply	VDD	4.75		5.25	V	

CAPACITANCE

(tA=25C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	CIN			30	pF	3
Output Capacitance	COUT			50	pF	3

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DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	IDD		40		mA	1
Input Leakage	II	-100		+100	uA	2,3
Output Current (2.4V)	IOH	-1.0			mA	3
Output Current (0.4V)	IOL	+4.0			mA	3

NOTES:

1. VDD = 5.25V; outputs open.
2. VSS < Vin < VDD.
3. Does not apply to RX+ and RX-.

DIGITAL ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
LPOS, LNEG Setup to LCLK Rising	t_{SD}	50			ns	
LPOS, LNEG Hold from LCLK Rising	t_{HD}	50			ns	
Propagation Delay from RRCLK to RRPOS, RRNEG Valid	t_{PD}			50	ns	
RCLK Period	t_P		648		ns	
RCLK Pulse Width	t_{WL},t_{WH}		324		ns	
RST\ Pulse Width	t_{RST}	1			us	

ANALOG ELECTRICAL CHARACTERISTICS

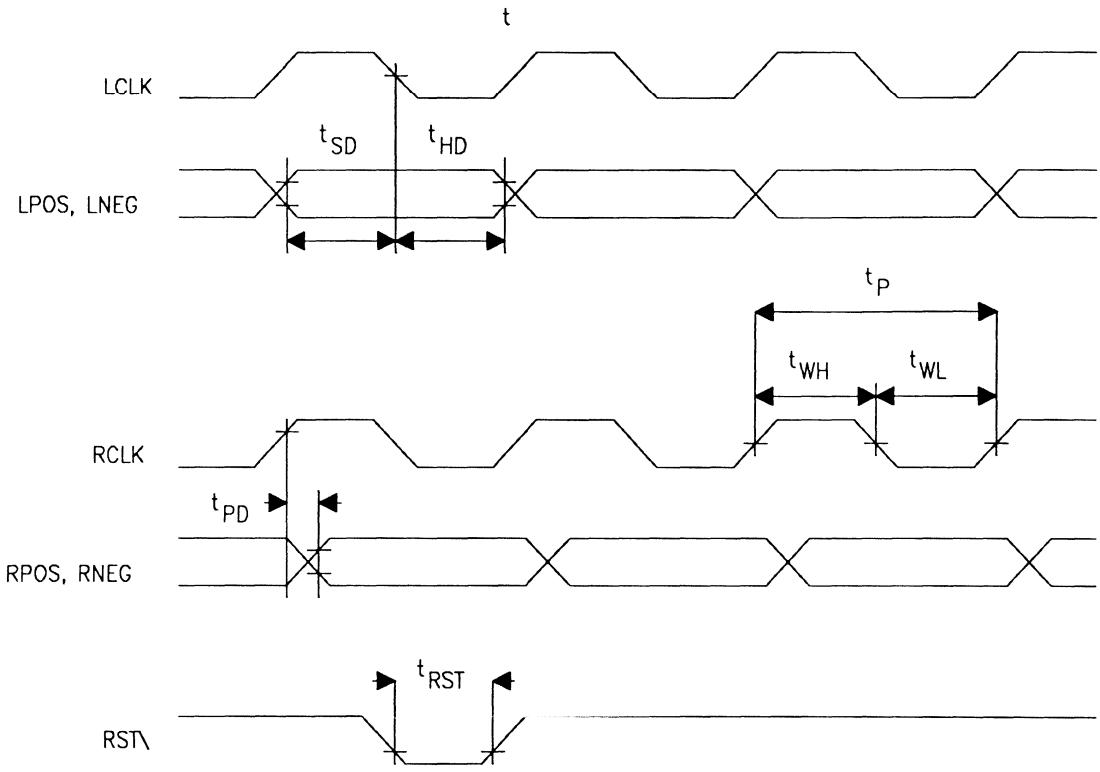
(0°C to 70°C; V_{DD}=5V +/- 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Signal Range	V_{IR}	-30		+0	dBSX	1
Input Impedance at 772KHz	I_Z	400		800	ohms	

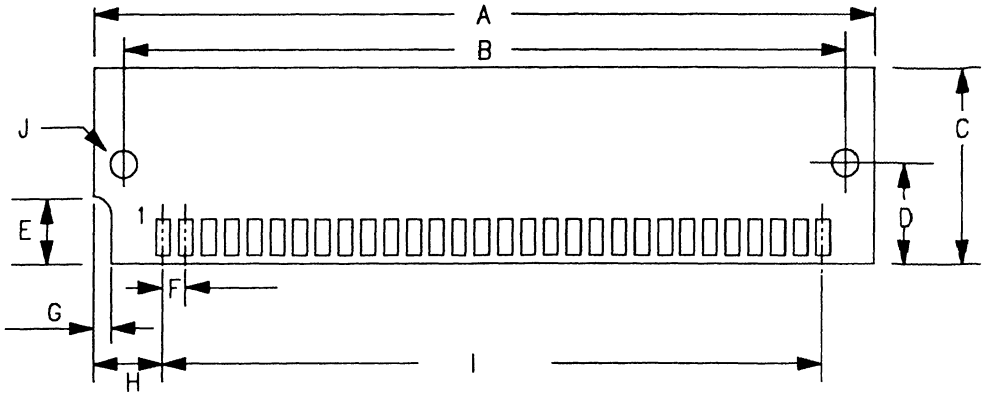
NOTES:

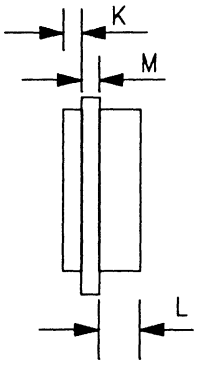
1. dBSX = 3Vpk; signal defined at the primary side of a 2:1 transformer with the secondary connected to RX+ and RX- (see Figure 4 for an example).

AC TIMING DIAGRAM Figure 7



DS2291
T1 LONG LOOP Stik





DIM	INCHES
A	3.500
B	3.234
C	0.850
D	0.400
E	0.250
F	0.100
G	0.080
H	0.300
I	2.900
J	0.125 DIA
K	0.100
L	0.250
M	0.050

DESIGN KITS

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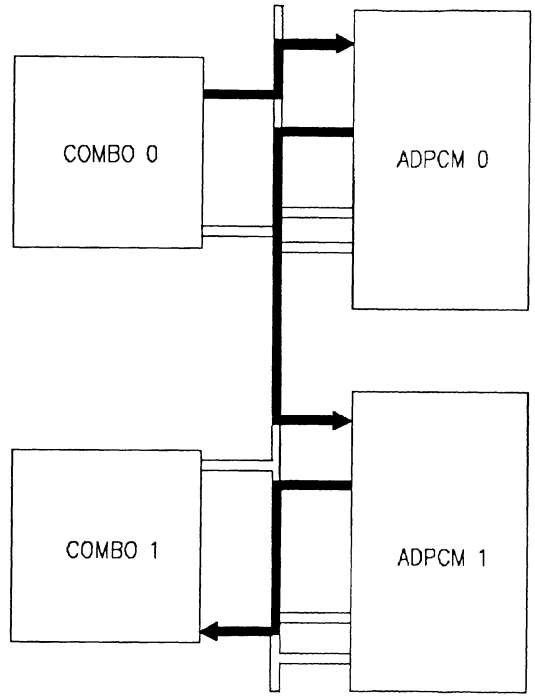
DALLAS SEMICONDUCTOR

DS2167K
ADPCM DESIGN KIT

FEATURES

- Emulates multi-channel applications such as T1 transcoders
- Expedites new designs by eliminating first-pass device prototyping
- Interfaces directly to IBM PC, XT, AT and compatibles
- High-level, graphic software demonstrates chip flexibility and feature set
- Kit components include:
  - DS2167 ADPCM processors (2)
  - Codec-combo devices (2)
  - Timeslot assigner circuit (TSAC) for combos
  - Support logic and clock generation circuitry
  - Printed circuit board
  - Interface cable for PC
  - Documentation and control software diskette



DESCRIPTION

The ADPCM design kit provides everything a user needs to evaluate the DS2167 ADPCM processors in an actual system environment. The evaluation board connects directly to transmission tests for performance monitoring of compressed or expanded channels. The board requires +/-5 volts. A system contro interface connects directly to the PC parallel printer port.

The kit's control software turns the PC into a powerful system controller. The program gives the user full control of system configuration, including timeslot placement, operating modes (compression, expansion, bypass or idle), data formats and algorithm reset. The controller program runs under MSDOS or IBM DOS version 2.0 or later. Color monitors are supported but not required.

1. INTRODUCTION

The DS2167 Evaluation Kit simplifies system level evaluation of the Dallas Semiconductor DS2167 ADPCM Processor. The DS2167 is a single CMOS integrated circuit which implements the recommended T1Y1 ADPCM 32K-bit speech compression/expansion algorithms for two independent channels. Not only does the DS2167 contain a high-speed DSP engine optimized for the ADPCM algorithms, but it also contains on-chip control and timing circuitry to minimize support logic for connection to serial PCM backplanes. A microcontroller compatible interface allows the DS2167 configuration to be defined by an external microcontroller. This kit allows performance evaluation of multiple-channel ADPCM processing systems. The kit includes an evaluation board and controller software.

The DS2168 Evaluation Kit is identical to the DS2167 Evaluation Kit, except that DS2168 ADPCM Processors are substituted for the DS2167. This device implements the older CCITT ADPCM algorithm. Except where noted, all information equally applies to both kits.

1.1 The Evaluation Board

The evaluation board is a self-contained, multi-channel speech compression/expansion system. A block diagram of the DS2167 Evaluation Board is shown in Figure 1. It contains two DS2167 ADPCM Processors and two CODEC/filter combos, all connected by a common PCM highway.

DS2167 access to the highway is controlled by on-chip channel time slot counters; combo access is controlled by a separate time slot assignment circuit (TSAC). A 1.544MHz data clock (BCLK) and 8KHz frame synchronization clock (SYNC) are generated on the Evaluation Board and routed to all synchronous elements. Four BNC connectors allow connections to the analog inputs and outputs of the two combos. Power-on reset for the DS2167s is provided by a DS1232 Micromonitor.

The board contains a configuration control port which connects directly to the parallel (printer) port of an IBM PC/XT/AT or compatible personal computer. If the computer has multiple printer

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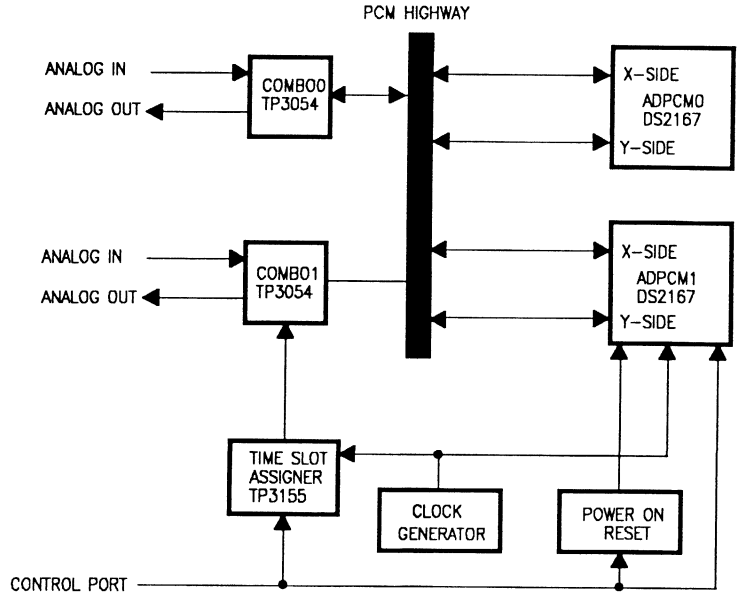
DS2167 EVALUATION BOARD BLOCK DIAGRAM Figure 1



ports, the evaluation board may be connected without interfering with normal printer operation.

Section two of this manual describes the evaluation board.

1.2 The Controller Software

The provided controller software turns an IBM PC (or compatible computer) into a system controller for the evaluation board. The program communicates with the evaluation board through a parallel (printer) port. The controller displays a system configuration. First, the user makes any configuration changes he or she desires. The display will be updated to reflect these changes. When all the changes have been made, the user directs the controller program to write the displayed configuration to the evaluation board.

The controller software runs under MSDOS or IBM DOS. It takes advantage of color monitors (both standard CGA and EGA color video adapters), but monochrome adapters may also be used. Several predefined configuration data files are included as examples. Section three of this manual describes the controller software, including setup instructions.

2. THE EVALUATION BOARD

This section discusses the DS2167 Evaluation Board hardware. First, the data paths through the board, including the PCM highway, are reviewed. Next the miscellaneous clocking and reset circuits are discussed. Finally, the configuration control port is presented.

2.1 The PCM Highway

All PCM data and ADPCM data travel along a common PCM highway. The combos and DS2167s are assigned time slots to place data onto and take data away from the highway. The DS2167 accomplishes this function with no external circuitry—it contains on-chip time slot counters. The combos require an external TSAC to control highway access.

Each combo has a pair of BNC connectors—one for its analog input and one for its analog output. The input signal is converted to PCM data and placed onto the highway during the combo's transmit time slot. The output signal is generated from the PCM data on the highway during the combo's receive time slot.

Data on the highway is grouped into frames of 193 bits. One bit occurs during the frame sync—the remaining 192 bits are divided into time slots. For PCM data, there are 24 8-bit time slots numbered 0 through 23. For ADPCM data, there are 48 4-bit time slots numbered 0 through 47. Time slot assignments are illustrated in figure two. Note that PCM and ADPCM data is carried over the same bus. Therefore it is undesirable, for example, to have one device transmitting PCM data during time slot 2 and another transmitting ADPCM data during time slot 5.

Each combo is assigned two time slots—one for transmit data and one for receive data. Each DS2167 is assigned four time slots—a transmit/receive pair for the X-side and another pair for the Y-side. Time slot values range from 0 to 63. Note that a device can be assigned a time slot which does not occur, which effectively disables the device. This is because the frame sync signal resets the TSAC and DS2167 time slot counters to zero, and the frame sync occurs after time slot 23. For example, if a combo is assigned a transmit time slot greater than 23, then the combo will never transmit data.

2.2 Clocking and Reset Circuitry

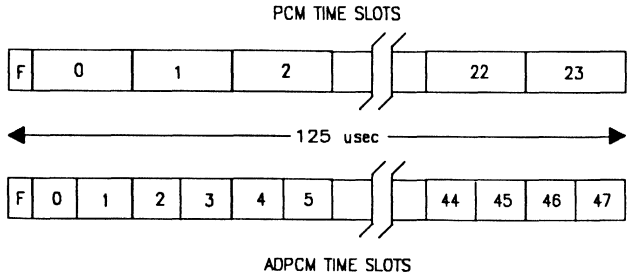
The DS2167 Evaluation Board contains a 1.544MHz data clock (BLCK) which runs to all synchronous elements. This clock is divided by 193 to obtain an 8KHz frame sync (SYNC) which is connected to both DS2167s and the TSAC. The TSAC generates the sync pulses which control combo processing. The TSAC supplied with the evaluation kit is the TP3155.

Power on reset for the DS2167s is provided by a DS1232 Micromonitor. The DS2167s may also be reset through the control port. The TSAC powers up with all sync pulses inhibited. A sync pulse is enabled (and only that sync pulse is enabled) when programmed through the control port.

2.3 Configuration Control

This section describes how the Evaluation Board control port works. It provides sufficient detail to construct controller hardware and software for the board. Note that the provided software alleviates the need to know these details, so most users may skip this section.

TIME SLOT ASSIGNMENTS Figure 2



The DS2167 contains a serial port which allows an external controller to define the device configuration. The configuration parameters include the input (receive) time slot, the output (transmit) time slot, the data format (*u*-Law or A-Law), the device mode (compress, expand, 4-bit bypass, 8-bit bypass, or idle), and algorithm reset control. This information is defined independently for the X and Y channels. Please refer to the DS2167 data sheet for information on these parameters and the serial port interface protocol.

The TSAC generates the sync pulses which control the combo's transmit and receive time slots. It contains a serial port for specifying time slot numbers and three control lines (CH0, CH1, and CH2) for associating the time slot number with a specific sync signal. Serial data is driven on the DC line and latched on the falling edge of the CLKC line. The configuration sequence is enabled by driving the CS line low. The protocol for the TSAC is shown in Figure 3. The T5 through T0 bits specify the time slot number. The X and R bits are both high to disable the associated channel (by suppressing that channel's sync pulse); any other value enables the sync pulse. Please refer to the TP3155 data sheet for further information.

The user can access both the DS2167 and TSAC through the Evaluation Board's control port. Figure 4 shows the connector pin assignments. For reference, the table shows the standard PC parallel port signal designations along with the Evaluation Board signal definitions. The input/output information is specified with respect to the DS2167 Evaluation Board.

The various signals are used as follows:

2.3.1 SCLK The serial data clocking signal for both the DS2167s and the TSAC. Note that the DS2167 latches serial data on the rising clock edge, while the TSAC latches data on the falling edge.

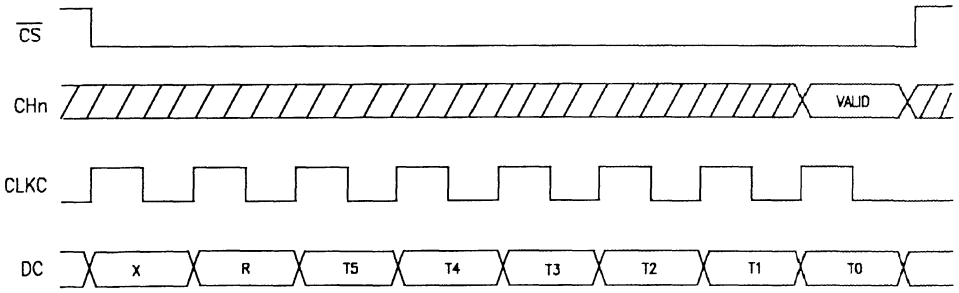
2.3.2 SDATA The serial data for both the DS2167s and the TSAC. Note that the DS2167 data bytes are written to the port least significant bit first, while TSAC data is written most significant bit first.

2.3.3 CSADPCM/ Chip select for both DS2167s. This signal should be low when either DS2167 serial port is being written, otherwise it should remain high.

2.3.4 CSTSAC/ Chip select for the TSAC. This signal should be low when the TSAC serial port is being written, otherwise it should remain high.

2.3.5 TSACCHAN This signal specifies the combo for which the time slot assignment is being made; it is the TSAC's "CH0" input. It should

TSAC CONTROL INTERFACE Figure 3



CONTROL PORT CONNECTIONS Figure 4

Header Pin	Signal Dir.	Board Signal	Port Signal	DB-25 Pin
1	input	SCLK	STROBE/	1
3	input	SDATA	BIT0	2
5	input	CSADPCM/	BIT1	3
7	input	CSTSAC/	BIT2	4
9	input	TSACCHAN	BIT3	5
11	input	TSACSIDE	BIT4	6
13	input	- -	BIT5	7
15	input	- -	BIT6	8
17	input	- -	BIT7	9
19	output	wired low	ACK/	10
21	output	wired low	BUSY	11
23	output	wired low	PEND	12
25	output	wired high	SELECT	13
2	input	- -	AUTOFEED/	14
4	output	wired high	ERROR/	15
6	input	RESET/	INIT/	16
8	input	- -	SELINP/	17
10-24	- -	ground	ground	18-25
26	- -	no connect	- -	- -

be low when assigning a combo 0 time slot and high when assigning a combo 1 time slot. It is latched by the TSAC at the same time as the T0 serial data bit.

2.3.6 TSACSIDE This signal specifies whether the time slot assignment is for a combo transmit or receive side; it is the TSAC's "CH2" input. It should be low when assigning a transmit time slot and high when assigning a receive time slot. It is latched by the TSAC at the same time as the "T0" serial data bit.

2.3.7 RESET/ Active low signal which generates a reset for the DS2167s. Please refer to the DS1232 Micromonitor data sheet for details on the timing of the reset signals.

2.3.8 Outputs The five output pins are hardwired to form a board "signature." This signature may be used to determine if the board is present on a particular printer port. If the board is connected to a PC with the provided cable, the signature may be checked by reading the parallel adapter's STATUS port and looking for a binary pattern "10011XXX."

3. CONTROLLER SOFTWARE

The DS2167 Evaluation Board Controller program allows the user to control the Evaluation Board configuration. A high level, graphic interface simplifies this task. In addition, several "canned configuration" data files are included to demonstrate some different board configurations.

3.1 Requirements and Setup

The ADPCM.EXE controller program is shipped on a DOS-compatible floppy disk. The program will run under MSDOS or IBM DOS on an IBM/PC, IBM/AT, or compatible personal computer. While the program takes advantage of color graphics, a monochrome display adapter may be used. A parallel printer port must be available on the PC for connecting the evaluation board. The procedure is as follows:

1. Make sure that the controller program can be accessed by either copying "ADPCM.EXE" from the floppy disk to the hard disk, or place the floppy disk in the drive and make that drive the current drive.
2. Connect the evaluation board to any parallel printer port on the PC with the provided interface cable.
3. Connect transmission test set or other equipment to the evaluation board's BNC connectors.
4. Connect power (+5 volts, −5 volts, ground) to the evaluation board, and turn the power supply on.
5. Start the controller program by typing "ADPCM".

NOTE—It is important that the board is powered up before the controller program is started. This is so that the program can find the board.

When the program is invoked, it automatically determines your system configuration. Specifically, it determines whether you are using a color monitor or a monochrome monitor, and it determines if the Evaluation Board is connected to the LPT1 or LPT2 port (or not connected at all).

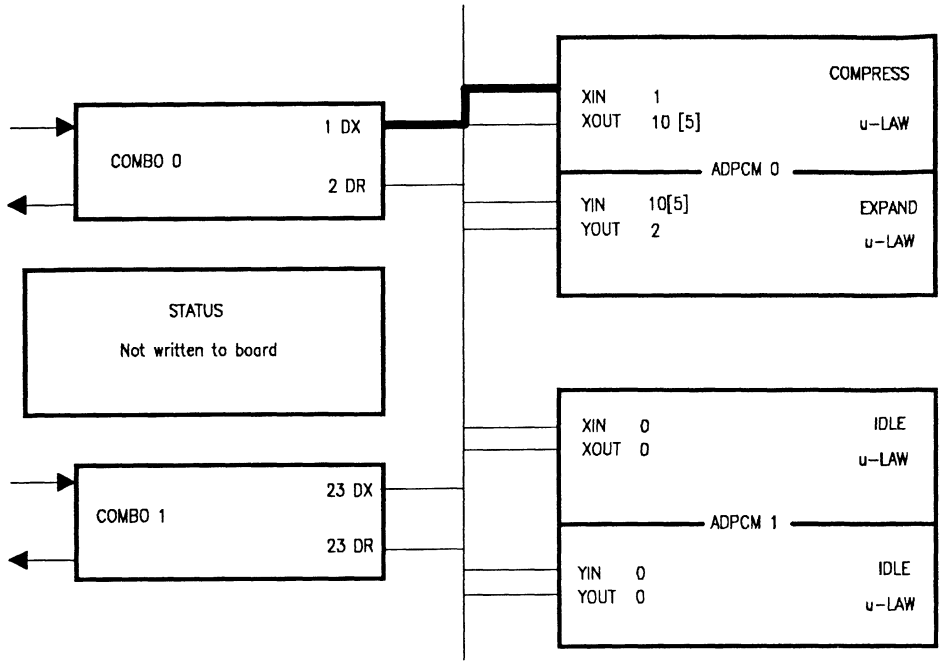
3.2 Screen Display

When invoked, a representation of the Evaluation Board configuration is drawn on the screen. This configuration may be edited and then written to the Evaluation Board. Figure 5 shows an example screen display. The following discussion will frequently reference this example to illustrate how the program works. The display shows four devices connected to the highway: COMBO0, COMBO1, ADPCM0, and ADPCM1. These represent the two combos and DS2167s, respectively.

In the following discussion, the terms *connection* and *link* will be used. A connection is any point which may access the highway, such as the ADPCM0 XIN pin. There are twelve possible connections on the Evaluation Board. A link consists of one or more connections which access the highway at the same time, either transmitting data or receiving data.

3.2.1 Time Slots The controller program shows connections at the combos and DS2167s leading to the PCM highway. Next to each connection is the time slot number associated with that connection. For example, figure five shows that COMBO0 will transmit during time slot 1 and receive during time slot 2.

CONTROLLER DISPLAY EXAMPLE Figure 5



Recall that 8-bit PCM and 4-bit ADPCM use different time slot numbering conventions, but they are transmitted together on the highway. For this reason, any connection which is transmitting or receiving ADPCM shows a number in brackets next to the time slot number. This bracketed number is the 8-bit PCM time slot which occurs at the same time as the programmed 4-bit time slot. The example shows that ADPCM0 will be transmitting 4-bit data on XOUT during time slot 10. ADPCM time slot 10 occurs at the same time as PCM time slot 5, so "5" is shown in brackets.

3.2.3 Formats and Modes The data format and operating mode of the DS2167s are also shown. The two possible data formats are *A-Law* and *u-Law*. The X-side of ADPCM0 is processing *u*-Law data in the example. The possible operating modes are *compress, expand, bypass-4, bypass-8,* and *idle*. The X-side of ADPCM0 is compressing 8-bit PCM data to 4-bit ADPCM data in the example.

The mode and format may be programmed only for the DS2167s—the combos are fixed. The combos shipped with the DS2167 Evaluation Kit process *u*-Law data, which is why the DS2167s are initially defined to *u*-Law format. If desired, you may replace the combos with TP3057 A-Law combos and reconfigure the DS2167s for A-Law data.

3.2.3 Connection Selection One connection on the screen is always considered the "selected connection." The selected connection is indicated by a highlighted time slot number. In the example it is the transmit connection of COMBO0, and if any configuration changes are made they will affect this connection. A different connection is selected with the cursor movement keys.

3.2.4 Links The link containing the selected connection is highlighted. This makes it easy to follow data flow through the Evaluation Board. The example shows that a link exists between

the COMBO0 DX connection and the ADPCM0 XIN connection. That is because the former is transmitting data during time slot 1 and the latter is receiving data during the same time slot. If the COMBO0 DX time slot was changed, then there would no longer be a link between it and ADPCM0 XIN, so the highlighted link would be removed. If the new transmit time slot linked COMBO0 to another device, then the new link would be highlighted.

Sometimes there can be problems in the links—you can create conflicting connections or mismatched connections. Conflicting connections occur when two connections try to transmit data onto the highway at the same time creating bus contention. Mismatched connections occur when two connections access the highway at the same time, but access it for different types of data. For example, if one device transmits PCM data and another device picks up half of it as ADPCM data, then these connections are mismatched.

When a color display is used, normal links are shown in blue, conflicting connections are shown in red, and mismatched connections are shown in pink (magenta). When a monochrome display is used, normal links are emboldened, conflicting connections blink in bold intensity, and mismatched connections blink in normal intensity. Even though the controller program locates problems between connections, the user is still free to program any configuration he or she desires.

3.2.5 Status Messages The "status" box may contain one of the following status messages:

- board not present
- not written to board

The "board not present" message indicates that the program doesn't see a DS2167 Evaluation Board connected to a parallel port. If the program can't find a board, then it will disable the commands which talk to the board. If you receive this message, verify that the evaluation board is properly connected to the PC and it is powered up. You can also verify the system configuration with the "F2" setup command discussed shortly.

The "not written to board" message indicates that the configuration shown on the screen has not been written to the Evaluation Board. The configuration is only written upon request from the user. This message will be displayed when the program first starts (unless no board is present), and any time changes are made. This message is removed when the configuration is written to the Evaluation Board.

3.3 Connection Selection Commands As mentioned, configuration commands only affect the selected connection—which is indicated by a highlighted time slot number. The cursor movement keys may be used to select a different connection. The recognized keys are:

- cursor up
- cursor down
- cursor left
- cursor right
- home
- end
- page up
- page down

The first four keys work much as expected—they move in the indicated direction. In the example, pressing the "cursor down" key will select the COMBO0 DR connection. In this case, the time slot value of "2" would be highlighted, and the link to ADPCM0 YOUT would be highlighted. Moving off the end of the screen wraps around to the other side. In the example, pressing the "cursor up" key will select the COMBO1 DR connection.

The "home" key moves to the top-left connection on the screen (COMBO0 DX). The "end" key moves to the bottom-right connection on the screen (ADPCM1 YOUT).

The last two cursor movement keys provide ways of quickly accessing other connections in a link. The "page up" key moves up the screen to the next connection which is linked to the selected connection. If there are no other connections linked to the selected connection then no changes are made. The "page down" key works similarly but it moves down the screen to the next connection in the link.

3.4 Keyboard Entry Many of the remaining commands require keyboard entry from the user (e.g. a file name, a device mode, etc.). As the user types, the characters are displayed at the

bottom of the screen. Editing is performed with the "backspace" key (delete last character) and the "escape" or "control/U" keys (delete line).

3.5 Configuration Commands Once a connection has been selected (with the aforementioned cursor movement keys), several commands are available for changing that device's configuration, specifically the time slot, data format, and operating mode. Press the "ENTER" key after the command is typed. Commands may be in either upper case or lower case. Only the first character of the command is required. For example, "bypass," "BYPASS", "ByPaSs", "b", and "byp" all mean the same thing.

3.5.1 Time Slot Selection When a number between 0 and 63 is entered, the time slot for the selected connection is changed to that number.

3.5.2 Data Format Selection The DS2167s may process either *u*-Law or A-Law data. The data format is specified independently for each side. To change the data format on one side of a DS2167, select either connection on that side and enter one of the following commands:

- *u*-Law
- A-Law

The hyphen need not be typed, so "U-LAW", "ULAW", and "U" all accomplish the same thing.

3.5.3 Operating Mode Selection The ADPCM operating mode is specified by selecting either connection on a side and specifying:

- Compress
- Expand
- Bypass
- Idle

Note that there are two different bypass modes: "bypass-4" which processes 4-bit ADPCM data and "bypass-8" which processes 8-bit PCM data. Each entry of the "bypass" command toggles between these two modes.

3.6 Function Key Commands
Some commands use the special function keys. They include:

F1 - Help
F2 - Change Program Setup
F3 - Write Configuration
F4 - Reset Board
F5 - Reset ADPCM Algorithm
F6 - Change ADPCM Address
F7 - Load from File
F8 - Save to File
F9 - DOS Escape
F10 - Exit Program

Some of these commands require information (such as a file name) to be entered. The user should type in the required information and then press the appropriate function key. The "ENTER" key should not be used.

3.6.1 F1—Help The "F1" help key displays a summary of the controller program commands.

3.6.2 F2—Setup When the controller program is started, it automatically determines the monitor type and where the Evaluation Board is connected. The "F2" key allows you to examine and modify the setup.

3.6.3 F3—Write Configuration Once a board configuration has been entered, the "F3" write configuration key sends the configuration to the board. Note that the board isn't updated as configuration changes are made—the "F3" key must be used to write out the configuration.

3.6.4 F4—Reset Board The "F4" reset key issues a reset to the DS2167s on the Evaluation Board. Once the devices are reset, you will need to use "F3" to program them again. The reset does not affect the combos or TSAC. A reset is automatically performed when the controller program is started.

3.6.5 F5—Reset Algorithm The "F5" key sends an algorithm reset request to the selected ADPCM. This request causes the DS2167 to reset the algorithm coefficients to their initial conditions. Note that this command does not change the device's configuration, and it only affects one side ('X' or 'Y') of a device. For example, if the "ADPCM0 XIN" connection is selected, then "F5" will reset the algorithm registers for the X-side of ADPCM0.

3.6.6 F6—Change Address The ADPCM0 and ADPCM1 pins A0 through A5 are hardwired on the Evaluation Board to addresses 0 and 1 respectively. The controller program normally uses these addresses. If hardware modifications are made to the board, the "F6" change address key may be used to select different device addresses. Use this command by entering a valid ADPCM device address (between 0 and 63) and then press "F6". The first time you try this, the controller program will ask if you want to allow changes to the device addresses. If you answer "Y" (for yes), then the display will be updated to show the ADPCM device address in brackets immediately following the device number. Unless the user modifies the evaluation board, he or she will probably not want to use this command.

3.6.7 F7—Load Configuration The "F7" load configuration command is used to load an evaluation board configuration from a file. This might be one of the "canned configuration" files included with the ADPCM Evaluation Kit, or a file created with the "F8" save configuration command. To use this command, enter a file name and then press "F7". Be sure that you enter the full file name. For example, if you want to load the "FULLDUP.DAT" file, then specify that, not just "FULLDUP". This command does not actually change the board configuration—you will need to use the "F3" write configuration key to do that.

3.6.8 F8—Save Configuration The "F8" save configuration command is used to save the configuration shown on the screen to a file. This configuration may be recalled at a later time with the "F7" load configuration command. To use this command, enter a file name and then press "F8".

3.6.9 F9—DOS Escape The "F9" key allows access to DOS without terminating the controller program. If a command is typed (e.g. "dir") and then "F9" is pressed, then that command will be run. If no command is typed, then pressing "F9" will pause execution of the controller program and pass control to DOS. When you are ready to return to the controller program, type "exit". In order for "F9" to work properly, you need to ensure that the controller program will be able to find "COMMAND.COM". If "F9" fails to work properly, ensure that the DOS "COMSPEC" parameter is properly set. If a DOS parameter called "SHELL" is defined then it will be used for DOS escapes instead of "COMMAND.COM" This command does not change the evaluation board status—it will continue to operate while the controller program is suspended.

3.6.10 F10—Exit Program The "F10" key terminates execution of the controller program. Note that exiting the program does not change the evaluation board status—it will continue to operate in the most recently defined configuration.

3.7 Additional Commands Two additional commands are:

- Control/L
- Control/C

"Control/L" redraws the display. "Control/C" terminates the program, and is equivalent to the "F10" function key.

3.8 Canned Configurations Four "canned configurations" are provided with the DS2167 Evaluation Kit. They are stored in the files "INITIAL.DAT", "EXAMPLE.DAT", "COMPARE.DAT" and "FULLDUP.DAT".

The "INITIAL.DAT" file contains the same configuration as when the program is first invoked. This file may be loaded to "start over from the beginning."

The "EXAMPLE.DAT" file contains the configuration shown in Figure 5 which has been used as an example throughout this document.

The "COMPARE.DAT" configuration allows the impact of compression/expansion to be compared. The analog input from COMBO0 is compressed, then expanded, and then output through COMBO0. The COMBO1 output is taken from the COMBO0 input, so the two combo outputs can be compared to see the effects of ADPCM processing. COMBO1 does no transmission in this configuration; only the receive side is used.

The "FULLDUP.DAT" configuration sets up a full duplex connection between the two combos. The input from COMBO0 is compressed, then expanded, and then output through COMBO1.

The COMBO1 input is compressed, expanded, and output through COMBO0.

4. CONCLUSION

The DS2167 Evaluation Kit demonstrates multiple ADPCM Processors operating in a single system. Due to the on-chip time slot counters and serial control port, this is accomplished with ease. No "glue" circuitry was required to do this—the Evaluation Board used but a few pull-up resistors and a port buffer for the DS2167s. The techniques demonstrated here extend to systems with as many as 64 DS2167s sharing common data and control lines. For applications which do not require this degree of flexibility, the DS2167's hardware mode alleviates the need for serial communication while maintaining the demonstrated performance.

Controller Program Command Summary

Connection Selection Commands

cursor up	Select connection above.
cursor down	Select connection below.
cursor left	Select connection to the left.
cursor right	Select connection to the right.
home	Select top-left connection.
end	Select bottom-right connection.
page up	Search up for another connection in this link.
page down	search down for another connection in this link.

Device Configuration Commands

number	Set connection time slot to **number**.
u-Law	Select *u*-Law data format.
A-LaW	Select A-Law data format.
Compress	Select PCM-to-ADPCM compression mode.
Expand	Select ADPCM-to-PCM expansion mode.
Bypass	Select or toggle bypass mode.
Idle	Select device standby state.

Function Key Commands

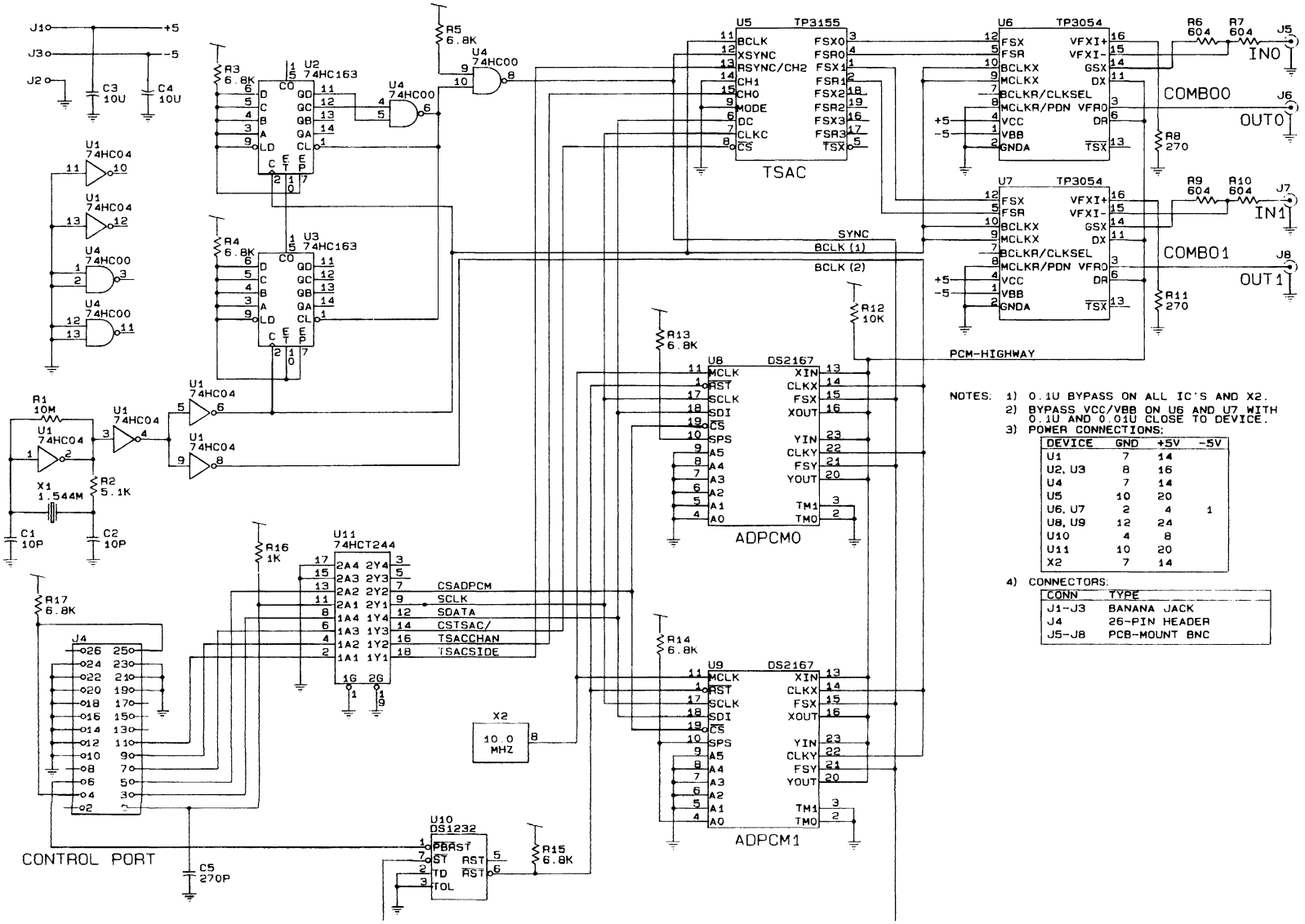
F1	Give help summary.
F2	Change display or port setup.
F3	Write configuration to board.
F4	Reset ADPCMs.
F5	Reset ADPCM algorithm for selected connection.
F6	Change ADPCM device address.
F7	Load configuration from file.
F8	Save configuration to file.
F9	DOS escape.
F10	Exit program.

Other Commands

Control/L	Redraw screen.
Control/C	Exit program.

Evaluation Board Parts List	
U1	74HC04 Hex Inverter
U2-U3	74HC163 Binary Counter
U4	74HC00 Quad Two-Input NAND
U5	TP3155 Time Slot Assignment Circuit
U6-U7	TP3054 *u*-Law CODEC/Filter Combo
U8-U9	DS2167 (or DS2168) ADPCM Processor
U10	DS1232 Micromonitor
U11	74HCT244 Octal Buffer
C1-C2	10pF Capacitor
C3-C4	10*u*F Capacitor
C5	270pF Capacitor
(4)	0.01*u*F Capacitors (U6, U7 decoupling)
(14)	0.1*u*F Capacitors (U1-U11, X2 decoupling)
R1	10Mohm, ¼W, 5% Resistor
R2	5.1Kohm, ¼W, 5% Resistor
R3-R5, R13-R15	6.8Kohm, ¼W, 5% Resistor
R6, R7, R9, R10	604ohm, ¼W, 1% Resistor
R8, R11	270ohm, ¼W, 5% Resistor
R12	10Kohm, ¼W, 5% Resistor
R16	1Kohm, ¼W, 5% Resistor
J1-J3	Banana Jack
J4	26-pin Header Connector
J5-J8	BNC Connector
X1	1.544MHz Crystal
X2	10MHz Crystal Clock Oscillator

ADPCM EVALUATION BOARD



NOTES:
1) 0.1U BYPASS ON ALL IC'S AND X2.
2) BYPASS VCC/VBB ON U6 AND U7 WITH 0.1U AND 0.01U CLOSE TO DEVICE.
3) POWER CONNECTIONS:

DEVICE	GND	+5V	-5V
U1	7	14	
U2, U3	8	16	
U4	7	14	
U5	10	20	
U6, U7	2	4	1
U8, U9	12	24	
U10	4	8	
U11	10	20	
X2	7	14	

4) CONNECTORS:

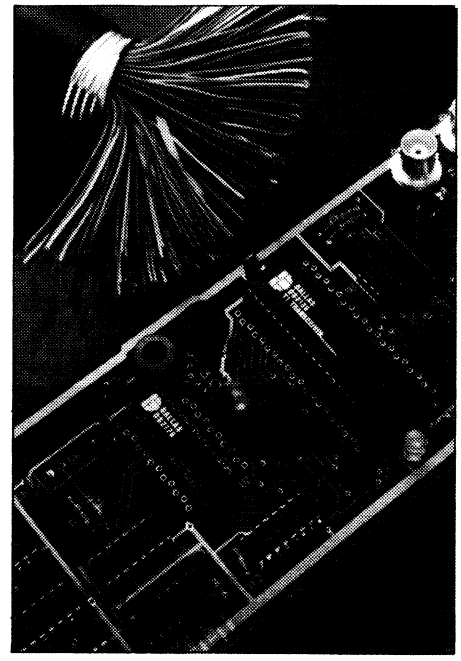
CONN	TYPE
J1-J3	BANANA JACK
J4	26-PIN HEADER
J5-J8	PCB-MOUNT BNC

DALLAS SEMICONDUCTOR

DS2180K
T1 DESIGN KIT

FEATURES

- Demonstrates key "hardware mode" attributes of the DS2180/DS2176 pair, such as:
  - Framing/synchronization
  - Link supervision and control
  - Signaling supervision
  - Rate adaption to equipment backplanes
- Expedites new designs by eliminating first-pass device prototyping
- Easily interfaced to user host controller for "software mode" evaluation
- User-supplied line interface allows direct connection to T1 lines
- Kit components include:
  - DS2180 T1 Transceiver
  - DS2176 T1 Receive Buffer
  - Printed circuit board
  - Support logic and clock generation circuitry
  - Applications and assembly information



DESCRIPTION

The DS2180K allows the user to evaluate the performance of the DS2180 T1 Transceiver and DS2176 T1 Receive Buffer in an actual system environment. The evaluation board requires +5 volts; board inputs and outputs are TTL-compatible. Test points and control options on the board simplify selection of device feature sets required by the system designer.

Kit assembly requires approximately 1 hour. Although designed for hardware mode operation, a small wire-wrap area is provided for user-supplied host processor interface.

See Application Note for further information.

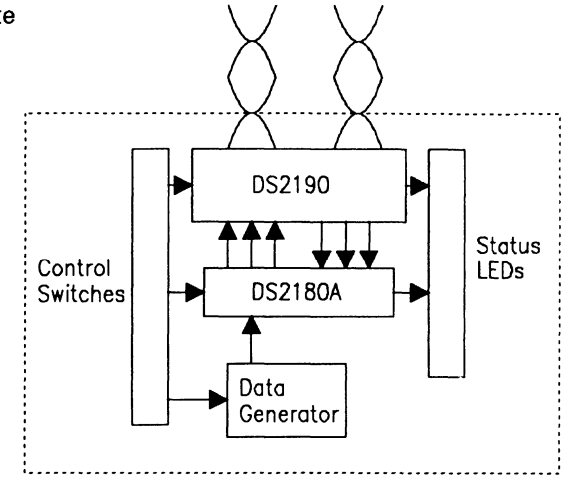
DALLAS SEMICONDUCTOR

DS2190DK
T1 Network Interface Unit Design Kit

FEATURES

- Self-contained system designed to evaluate the DS2190 T1 Network Interface Unit
- Includes the following:
  - DS2190 Network Interface Unit
  - DS2180A Primary Rate Transceiver
  - Transmit clock and frame sync Circuitry:
  - Status LEDs
  - Control DIP switches
  - Bantam jacks
  - Documentation
- Kit comes completely assembled
- Easily accessible test points
- Onboard data generator capable of QRSS generation and channel data insertion
- Prototyping wire-wrap area for user customization
- Powered by a single +5V supply

DESIGN KIT LAYOUT



DESCRIPTION

The DS2190DK contains all of the necessary support logic to completely evaluate the DS2190 Network Interface Unit. The DS2190DK can be connected to T1 test equipment, a simulated T1 line, or back onto itself. The board is organized for simplicity of operation. It is controlled through DIP switches, and real-time status can be monitored through a set of LEDs. The DS2190DK allows users to customize the kit to fit their needs. There is a prototyping wire-wrap area and all key signals are brought out to test points. An optional computer interface to control the DS2180A transceiver in the software mode is also available.

OVERVIEW

A functional block diagram of the DS2190DK is shown in Figure 1; a general layout of the kit is shown in Figure 2. Much of the operation of the DS2190DK revolves around the operation of its two main components, the DS2190 Network Interface Unit (NIU) and the DS2180A Primary Rate Transceiver. Partial descriptions of the functions of these two devices are given in this data sheet but more detailed information can be found in their individual data sheets. It's recommended that users of the DS2190DK familiarize themselves with these devices (especially the NIU) before beginning use of the DS2190DK.

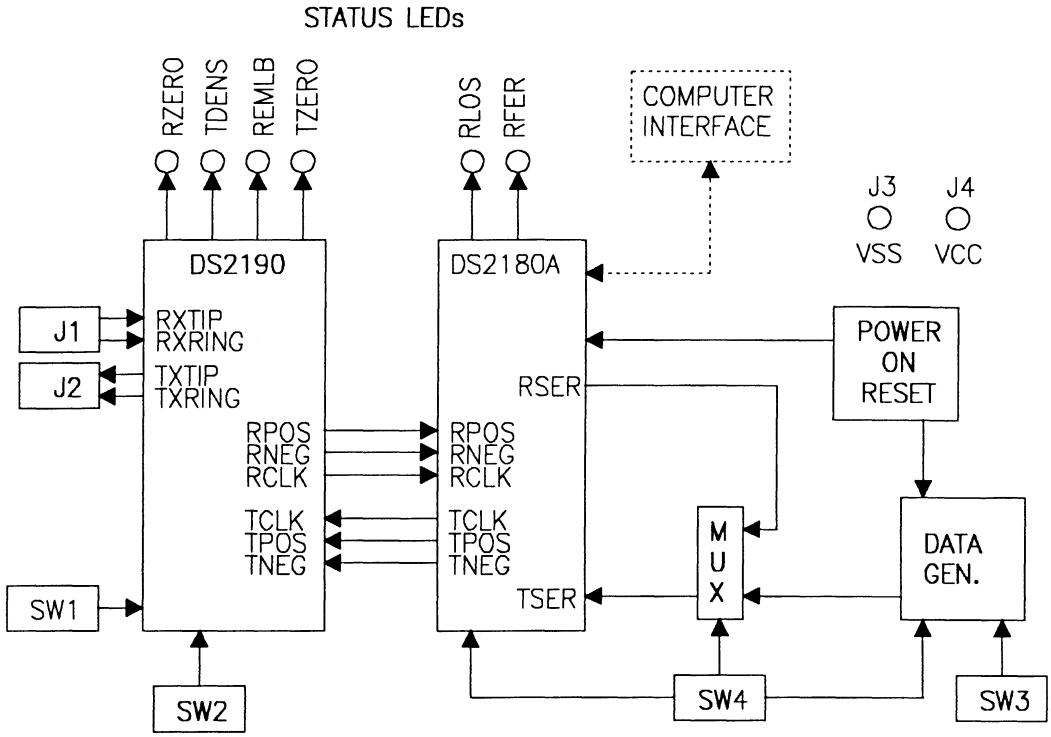
The DS2190DK can be connected to test equipment or a simulated T1 line through the Bantam jacks J1 and J2 on the board. J1 is the receive side (RX) jack and it connects directly to the receive input circuitry of the NIU. T1 signals in the range of 0dBSX to -30dBSX can be applied here. J2 is the transmit side (TX) jack and it connects directly to the transmit output circuitry of the NIU. Power must be supplied to the board through the banana jacks J3 and J4. J3 is marked "VSS" on the board and should be connected to the ground of a DC power supply. J4 is marked "VCC" and should be connected to an external +5V DC power supply. (CAUTION: reversing the J3 and J4 connections can cause serious damage to the DS2190DK.) The DS2190DK contains a power monitor circuit (DS1231 - U4) that automatically resets the board if power drops below 4.5V. Hence, the DS2190DK will not operate properly below 4.5V. J5 is an optional connector on the DS2190DK. It is not supplied with the kit. Its purpose will be covered in the computer interface section.

Control of the DS2190DK is accomplished through a set of four switches. Switch 1 is the only one which is not a DIP switch and it controls the amount of Line Build Out (LBO) that the NIU provides on the transmitted signal. Switch 2 controls only the NIU. Switch 3 provides data for the data generator (U2). Switch 4 controls the DS2180A and transmit data section of the board. One side of each of the DIP switches (SW2, SW3, SW4) is tied to ground while the other side is tied to a 100K ohm pullup resistor and to a specific point on the board. A complete functional description of each of these switches is given in this data sheet along with a quick reference summary in Appendix A.

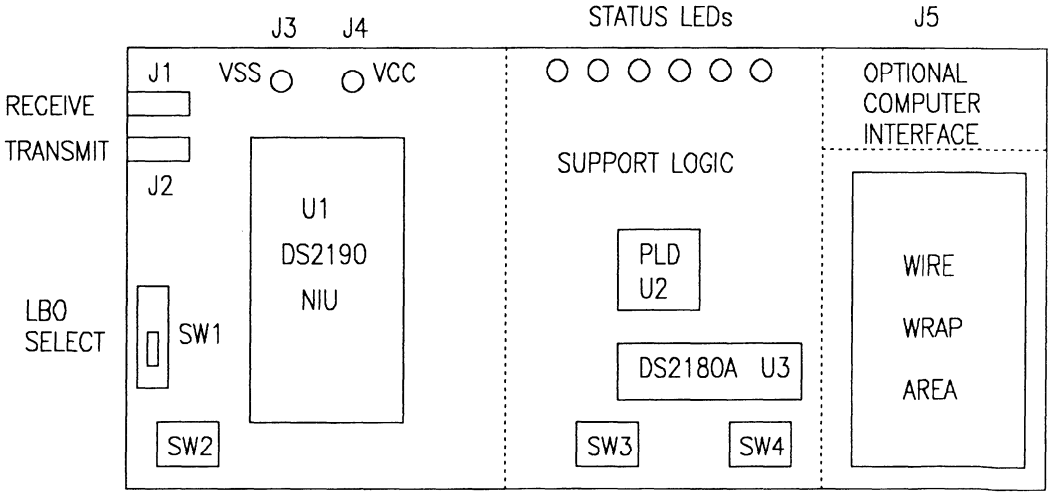
Real-time status of the board can be monitored through a set of six red LEDs at the top of the board. Four of the LEDs are tied to signals from the NIU and the other two are tied to signals from the transceiver. Two of the LEDs (TDENS and RFER) are timed by NE555 one-shots (U7 and U8) so that they can be readily seen. A complete functional description of the LEDs is given in this data sheet along with a quick reference summary in Appendix A.

An onboard multiplexor (U11) and data generator allow the user to set up the DS2190DK to transmit a number of different data streams. This enables the user to evaluate the DS2190 in a number of different configurations. The muliplexor will select clock, data, and frame sync information either from the receive side of the DS2180A (U3) transceiver or from the data generator. The data from the data generator can be one of two types, either a QRSS signal or an 8-bit byte that is inserted into all 24 T1 channels. Figures 3 and 4 represent two of the more common configurations of the DS2190DK. Figure 3 demonstrates how the DS2190DK might be used with a piece of T1 test equipment, while Figure 4 demonstrates how the kit can be used to evaluate the NIU without any additional T1 equipment.

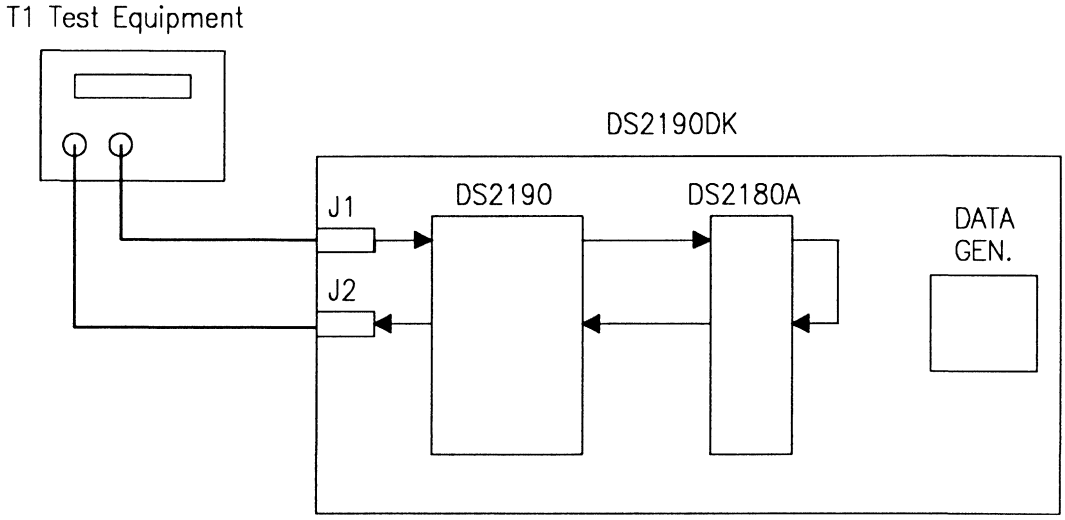
DS2190DK BLOCK DIAGRAM Figure 1



DS2190DK LAYOUT Figure 2



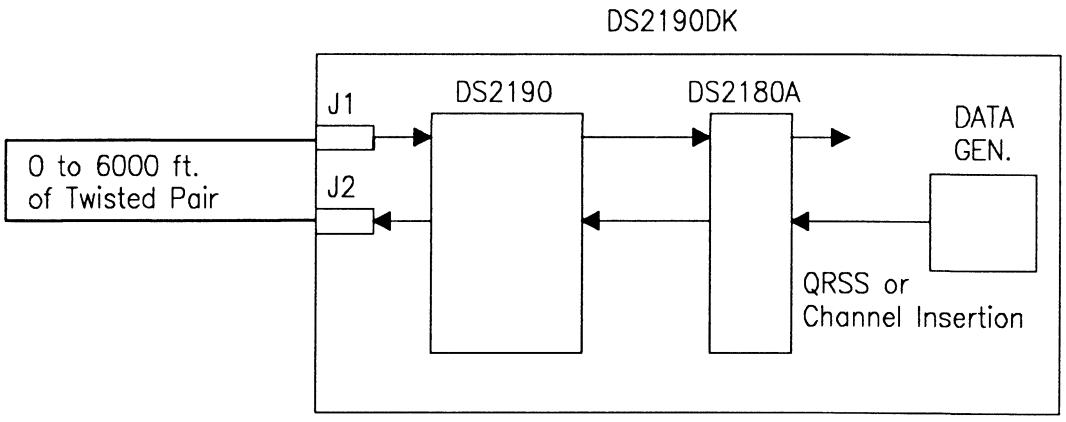
USE OF DS2190DK WITH T1 TEST EQUIPMENT Figure 3



NOTE:
1. Close the DGEN DIP switch (SW4 - 7).

8

USE OF DS2190DK WITHOUT T1 TEST EQUIPMENT Figure 4



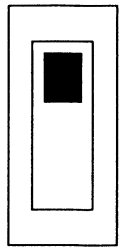
NOTES:
1. Open the DGEN DIP switch (SW4 - 7).
2. To select QRSS data, open the QRSS DIP switch (SW4 - 8).
3. To insert channel data, close the QRSS DIP switch (SW4 - 8).
4. The RFER (pin 38) and RBV (pin 37) pins of the DS2180A can be used to check data integrity.

STATUS LEDs Table 1

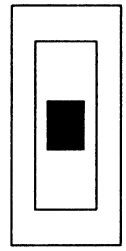
SYMBOL	DEVICE	DESCRIPTION
RZERO	**LED1**	**Receive Zeros.** When illuminated, the DS2190 has lost the receive T1 signal. It will light after 32 consecutive zeros have been received and will extinguish itself after a signal pulse off of the T1 line has been detected.
RLOS	**LED2**	**Receive Loss of Sync.** When illuminated, the DS2180A has lost the T1 framing pattern and is in the process of resynchronization. This lamp will extinguish itself when the DS2180A has synchronized to the incoming T1 data stream.
RFER	**LED3**	**Receive Frame Error.** When illuminated, the DS2180A has detected an error in the framing bits of the incoming T1 data stream. When the D4 framing modeis selected (SW4 - 2 is closed), both Ft and Fs errors are indicated. If the ESF framing mode is selected (SW4 - 2 is open), then both FPS and CRC errors will be indicated.
REMLB	**LED4**	**Remote Loopback Detect.** When illuminated, the DS2190 is in the remote loopback state. In this mode, the NIU will ignore the data at TPOS and TNEG, and instead transmit the received data back to the network without going through the DS2180A. The DS2190 enters this mode when it has received the loopback set code (a repeating "00001" pattern) for approximately 4.75 seconds. LED4 will extinguish itself when the DS2190 has received the reset code (a repeating "001" pattern) for approximately 4.75 seconds or if the RSTRLB switch is enabled (SW2 -2 is opened).
TZERO	**LED5**	**Transmit Zeros Detect.** When illuminated, the DS2190 has not detected any clock transitions at the TCLK input (pin 23) for 150ms. In this state, the NIU is transmiting an AIS signal (unframed all ones) to the network. LED5 will extinguish itself when a transition at the TCLK input is detected by the DS2190.
TDENS	**LED6**	**Transmit Density Detect.** When illuminated, the DS2190 has detected a pulse density violation in the transmitted data. If the INHDEN is not enabled (SW2 - 1 is closed), the NIU will insert a one into the data stream to correct the violation.

SWITCH 1 : TRANSMIT LINE BUILD OUT CONTROL

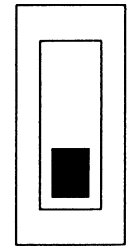
Switch 1 is a three-position slide switch that selects the transmit output level of the DS2190. The available settings are 0dBSX, -7.5dBSX, and -15dBSX. 0dBSX represents a signal of 3 volts peak into a 100 ohm termination. The settings of switch 1 are shown below:



0dBSX



-7.5dBSX



-15dBSX

DIP SWITCH 2 : DS2190 CONTROL Table 2

SYMBOL	DEVICE	DESCRIPTION
INHDEN	**SW2 - 1**	**Inhibit Density Monitor.** When enabled (opened), the DS2190 will not correct pulse density violations in the data to be transmitted. When disabled (closed), the NIU will alter the transmitted data to correct for the density violations. The TDENS (LED6) indicator operates independently of the INHDEN switch.
RSTRLB	**SW2 - 2**	**Reset Remote Loopback State.** When enabled (opened), the DS2190 will be forced to return from the remote loopback state to the normal operating state. If this switch is left enabled, the NIU will be inhibited from entering the remote loopback state. When disabled (closed), the DS2190 reacts normally to the remote loopback codes.
TSCOD	**SW2 - 3**	**Transmit Set Code.** When enabled (opened), the DS2190 will transmit the remote set code (a repeating "00001" pattern). When disabled (closed), the NIU will transmit the data as presented at TPOS and TNEG.
TRCOD	**SW2 - 4**	**Transmit Reset Code.** When enabled (opened), the DS2190 will transmit the remote set code (a repeating "001" pattern). When disabled (closed), the NIU will transmit the data as presented at TPOS and TNEG.

LOCLB	**SW2 - 5**	**Local Loopback Enable.** When enabled (opened), the DS2190 will ignore the incoming data off of the T1 line and instead loop the transmit signal back to the receive side where clock and data will be recovered by the receive side circuitry and presented at RPOS and RNEG. When disabled (closed), the NIU will process the data received at the RXTIP and RXRING inputs.
CLKSEL	**SW2 - 6**	**Clock Select.** When enabled (opened), the DS2190 will switch to an internal 1.544MHz clock when a RZERO condition (LED1 is lit) occurs. When disabled (closed), the RCLK output will go to a static high state when a RZERO condition occurs.
DELSEL	**SW2 - 7**	**Delay Select.** When enabled (opened), the DS2190 assumes a 10 clock delay from the FRSYNC pulse to the framing data presented at TPOS and TNEG. When disabled (closed), the NIU assumes that the FRSYNC pulse occurs when the framing data is presented at TPOS and TNEG. (NOTE: the DELSEL input accounts for the data delay through the DS2180A. Unless the DS2190DK is modified, the DELSEL switch should be kept enabled.)
SPARE	**SW2 - 8**	**Unassigned Switch.** Can be assigned by the user for a customized purpose.

DIP SWITCH 3 : CHANNEL DATA PATTERN Table 3

SYMBOL	DEVICE	DESCRIPTION
D1	**SW3 - 1**	**Channel Data Bit 1.** MSB of an 8-bit pattern forced into all 24 channels.
D8	**SW3 - 8**	**Channel Data Bit 8.** LSB of an 8-bit pattern forced into all 24 channels.

NOTE:

DIP switch 3 specifies an 8-bit pattern that will be placed into all 24 channels of the T1 pattern that is to be transmitted if the DGEN switch is enabled (SW4 - 7 is open) and the QRSS switch is disabled (SW4 - 8 is closed). D1 is transmitted first and hence would be considered the MSB of the byte transmitted. A one will be placed in the data stream if SW3 is open and a zero will be placed if SW3 is closed.

DIP SWITCH 4 : SYSTEM CONTROL Table 4

SYMBOL	DEVICE	DESCRIPTION
193SI	SW4 - 1	**193S S-Bit Insertion.** When enabled (opened), Fs bits are sourced from the DS2180A TLINK input (pin 10). When disabled (closed), Fs bits are internally sourced by the transceiver. If the DS2180A is placed into the ESF mode (SW4 -2 is open), then the 193SI switch has no effect on the DS2180A or DS2190DK.
FM	SW4 - 2	**Frame Mode Select.** When enabled (opened), the DS2180A operates in the ESF (193E) framing mode. When disabled (closed), the DS2180A operates in the D4 (193S) framing mode. (NOTE: the ESF framing mode offers superior error checking over the D4 framing mode due to the inclusion of CRC bits in the framing field.)
TYEL	SW4 - 3	**Transmit Yellow Alarm.** When enabled (opened), the DS2180A will generate the proper yellow alarm in the data stream to be transmitted according to the frame mode (SW4 - 2) the transceiver is operating in. In ESF (SW4 - 2 is open),the transceiver will generate a repeating .00FF Hex pattern in the FDL. In D4, (SW4 - 2 is closed), a zero is placed in bit 2 of all channels.
B7	SW4 - 4	**Bit 7 Zero Suppression.** When enabled (opened), the DS2180A will force bit 7 to a one if a channel contains eight zeros. When disabled (closed), then no bit 7 stuffing will occur.
B8ZS	SW4 - 5	**Bipolar Eight Zero Substitution.** When enabled (opened), the DS2180A will transmit a B8ZS code word if eight consecutive zeros occur in the transmit data stream. Also, B8ZS code words in the incoming T1 data stream will be decoded by the transceiver. When disabled (closed), no B8ZS coding or decoding takes place.
SPS	SW4 - 6	**Serial Port Select.** When enabled (opened), the DS2180A is in the software mode. When disabled (closed), the DS2180A is in the hardware mode. Unless the transceiver is being controlled by the optional computer interface (see the Computer Interface section), SW4 - 6 should always be closed.

DGEN	**SW4 - 7**	**Data Generator Select.** When enabled (opened), the transmit multiplexor selects the clock, data, and frame sync information generated onboard the DS2190DK to be passed to the DS2190 and DS2180A. The data generated will be produced by U2. When disabled (closed), the transmit multiplexor selects the clock, data, and frame sync information from the receive side of the DS2180A to be transmitted.
QRSS	**SW4 - 8**	**QRSS Select.** When enabled (opened), the data generator (U2) produces a 20-bit QRSS pattern with 15-zero suppression as defined in Appendix A of PUB 62411 (Oct. 1985). When disabled (closed), the data generator produces a repeating 8-bit pattern that is determined by DIP SW3. This 8-bit pattern in placed in all 24 channels.

DATA GENERATOR

The DS2190DK contains an onboard data generator that was designed to help the user easily evaluate the performance of the DS2190. The generator consists of a programmable logic device (an Altera PLD - U2), a 3.088MHz oscillator (X1), and a frame sync generator (U10 and U11). In order for the data generator to become active in the system, the DGEN DIP switch (SW4 - 7) must be open. The data generator can create two different data streams depending on the state of the QRSS Select DIP switch (SW4 - 8). If the QRSS DIP switch is closed, then a repeating 8-bit pattern will be placed into all 24 channels of the T1 data stream. This 8-bit pattern is determined by DIP switch 3. If the QRSS DIP switch is open, then a Quasi Random Signal Source (QRSS) pattern is created. This QRSS pattern follows the format as outlined in Appendix A of PUB 62411 (ACCUNET T1.5 Service Description and Interface Specifications - October 1985). The QRSS pattern is generated by a 20-stage shift register with feedback taken from the 17th and 20th stages. As defined by PUB 62411, the data generator will suppress strings of 15 consecutive zeros by inserting a one. Hence the longest string of zeros produced by the data generator is 14 zeros long. If the data generator is creating the QRSS pattern, then the framing bits will be inserted into the QRSS data stream by the DS2180A. (In other words, the framing bits do not overwrite the pattern.) For a detailed schematic of the PLD, please see Appendix B.

NOTE:

If the user is trying to meet the QRSS specifications of PUB 62411, then all zero suppression schemes on the DS2180A must be disabled. Hence, both the B7 and B8ZS switches should be closed.

COMPUTER INTERFACE

The DS2190DK is equipped with an optional computer/controller interface. This interface allows the user to operate the DS2180A in the software mode instead of the hardware mode. The DS2180A has expanded capabilities in the software mode. It can be used be used to count frame or CRC errors, OOF events, and bipolar violations. Also, it can be used to mark data in both the transmit and receive paths. Under the software mode, the user has access to complete flexibility of the DS2180A. Please consult the DS2180A data sheet for complete details.

The computer interface has been designed to directly connect the DS2190DK to the parallel printer port of an IBM PC or compatible computer. This allows the user who is familiar with the DS2180A to develop controller programs for DS2190DK. For more information on how to go about writing such a program, please contact the factory.

The following components are recommended for the computer interface:

J5	26-pin right-angle header receptacle (example: 3M No. 3429)
U13	74HCT244 octal buffer
C4	100pf capacitor
R10	1K ohm resistor

The DS2190DK can be connected to the computer's parallel printer port by a cable which has a 26-pin header connector on one end and a DB-25 male connector on the other. The connections are:

DS2190DK Board	26-pin Header	DB-25 Connector	Parallel Port on the PC
SCLK	1	1	strobe\
-	2	14	auto feed\
SDI	3	2	D0
GND	4	15	error\
-	5	3	D1
-	6	16	init/
CS\	7	4	D2
-	8	17	select in\
-	9	5	D3
GND	10	18	ground
-	11	6	D4
GND	12	19	ground
-	13	7	D5
GND	14	20	ground
-	15	8	ground
GND	16	21	ground
-	17	9	D7
GND	18	22	ground
GND	19	10	ack\
GND	20	23	ground
INT\	21	11	busy
GND	22	24	ground
SDO	23	12	paper end
GND	24	25	ground
GND	25	13	select
-	26	-	-

To enable the computer interface, place switches 193SI, FM, TYEL, B7, B8ZS, and SPS in the open position. Failure to place these switches in the open position will cause the some of the outputs of the octal buffer (U13) to be shorted to ground.

APPENDIX A : DS2190DK QUICK REFERENCE

LED INDICATORS

RZERO	The DS2190 has lost the receive T1 signal.
RLOS	The DS2180A has lost frame synchronization.
RFER	The DS2180A has detected either a framing or CRC error.
REMLB	The DS2190 is in the remote loopback state.
TZERO	The DS2190 has lost the transmit clock signal.
TDENS	The DS2190 has detected a transmit pulse density violation.

DIP SWITCH 2 : DS2190 CONTROL

INHDEN	Open = do not correct pulse density violations in the transmit data. Closed = correct pulse density violations in the transmit data.
RSTRLB	Open = force the DS2190 to return to normal operation from a remote loopback state. Closed = allow the DS2190 to respond normally to remote loopback codes.
TSCOD	Open = transmit the remote loopback set code. Closed = do not transmit the remote loopback set code.
TRCOD	Open = transmit the remote loopback reset code. Closed = do not transmit the remote loopback reset code.
LOCLB	Open = internally loop transmit data back to the receive circuitry of the DS2190. Closed = do not internally loopback transmit data; receive circuitry senses RXTIP and RXRING.
CLKSEL	Open = switch to an internal 1.544MHz clock if the receive signal is lost. Closed = do not switch to the internal 1.544MHz clock if the receive signal is lost.
DELSEL	Open = framing bit appears at TPOS and TNEG 10 TCLKs after FRSYNC (see Note 1). Closed = FRSYNC defines when the framing bit appears at TPOS and TNEG.

DIP SWITCH 3 : CHANNEL DATA PATTERN

D1 MSB of the 8-bit pattern; open = one, closed = zero.

D8 LSB of the 8-bit pattern; open = one, closed = zero.

DIP SWITCH 4 : SYSTEM AND DS2180A CONTROL

193SI Open = in the D4 framing mode, Fs bits are sampled at the TLINK input of the DS2180A.
Closed = in the D4 framing mode, Fs bits are internally sourced by the DS2180A.

FM Open = ESF (193E) framing mode selected; superior error detection.
Closed = D4 (193S) framing mode selected.

TYEL Open = transmit yellow alarm; type of yellow alarm transmitted depends on framing mode.
Closed = do not transmit yellow alarm.

B7 Open = stuff bit 7 with a one if the channel contains eight zeros.
Closed = do not stuff bit 7 under any condition.

B8ZS Open = replace any eight consecutive zeros with a B8ZS code word.
Closed = do not inject B8ZS code words.

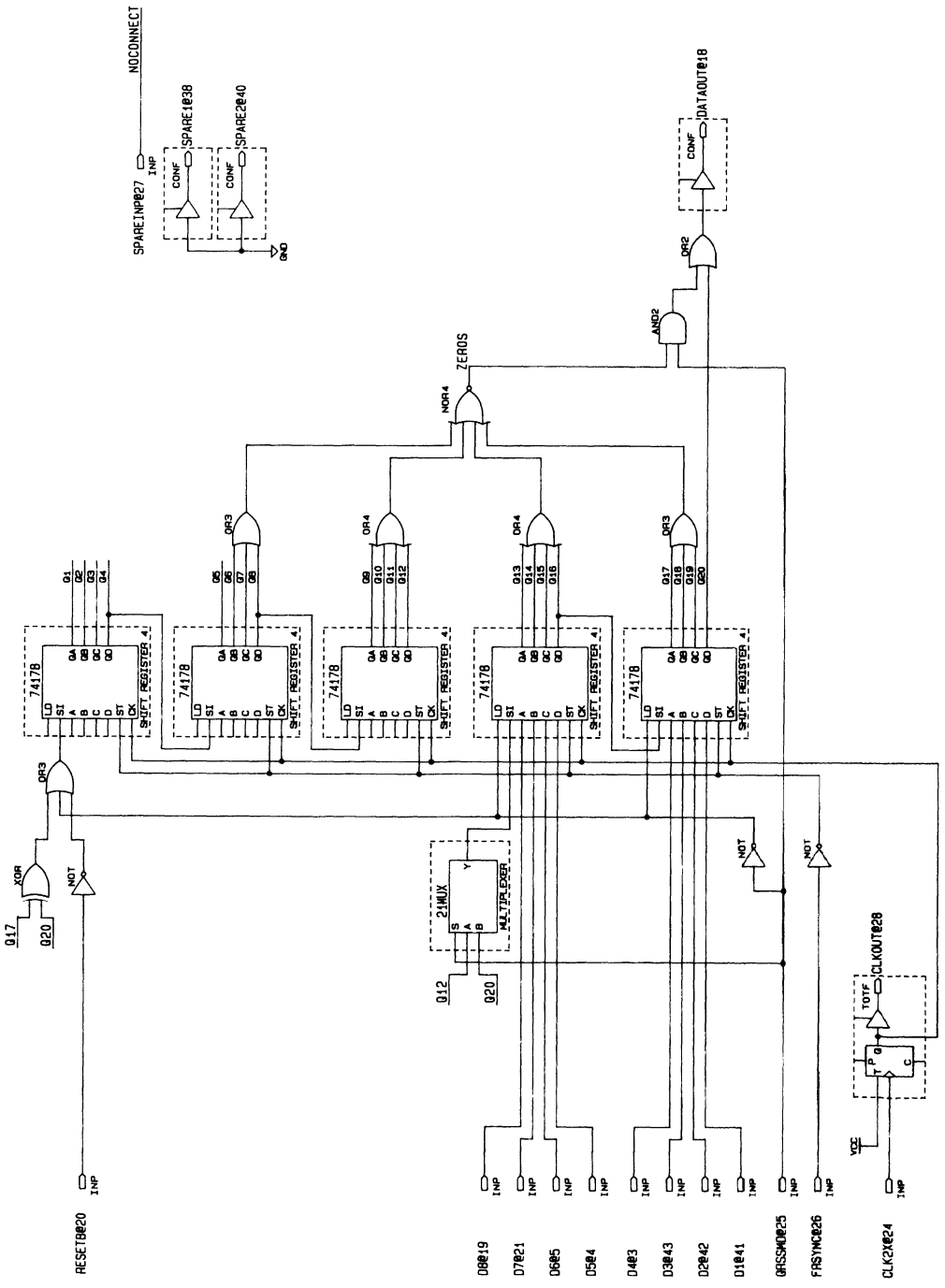
SPS Open = the DS2180A operates in the software mode.
Closed = the DS2180A operates in the hardware mode (see Note 1).

DGEN Open = onboard data generator creates the transmitted data stream.
Closed = transmitted data stream is obtained from the received data stream.

QRSS Open = onboard data generator creates a QRSS data stream.
Closed = onboard data generator inserts a data byte from DIP switch 3 into all 24 channels.

NOTE:
1. Unless the DS2190DK is modified, the DELSEL switch should be kept open and the SPS switch should be kept closed.

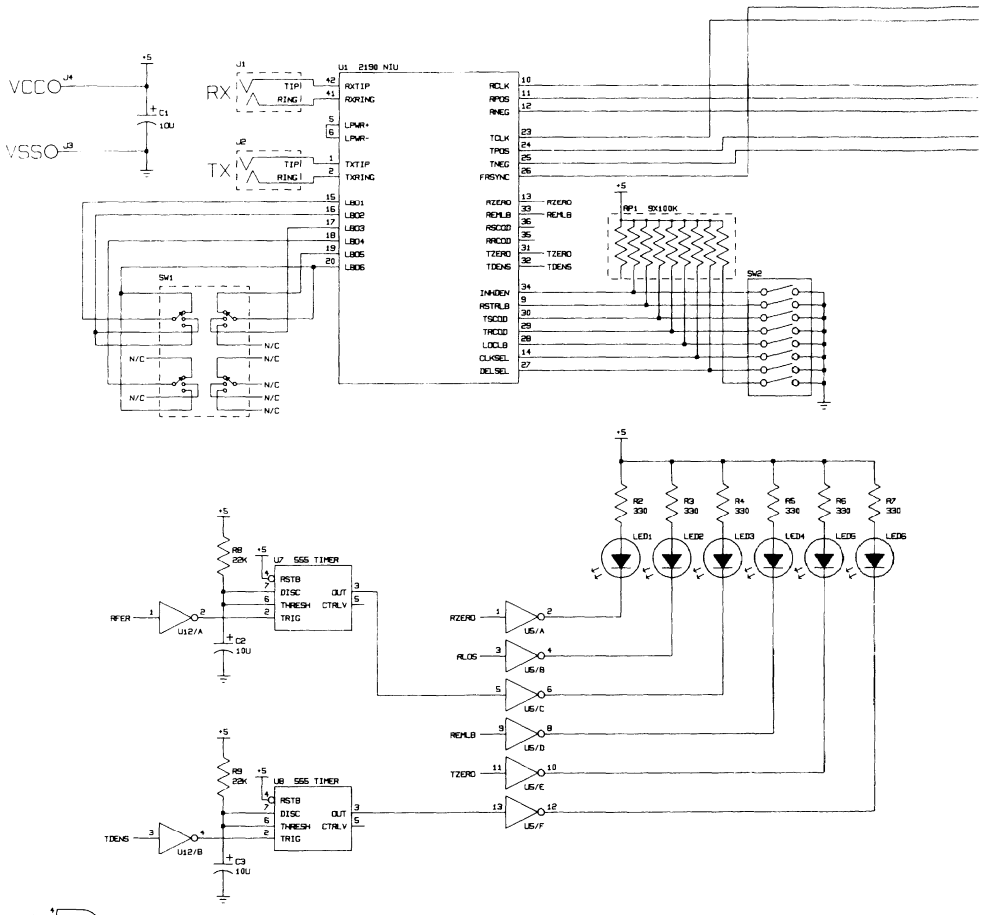
APPENDIX B : ALTERA PLD (U2) SCHEMATIC



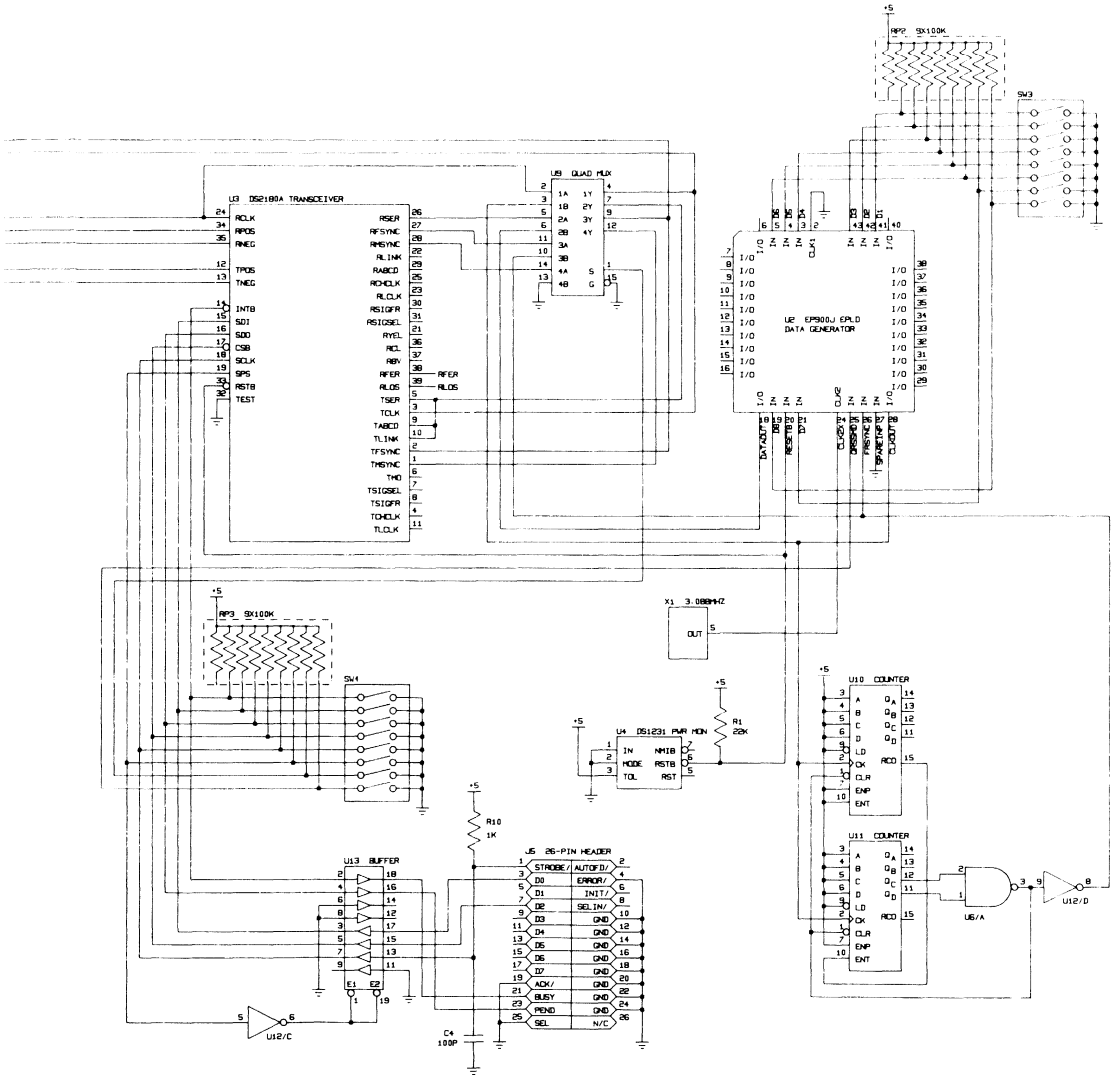
APPENDIX C : DS2190DK PARTS LIST

ITEM	PART #	DESCRIPTION	QTY
U1	DS2190	Network Interface Unit	1
U2	EP900J	Altera PLD	1
U3	DS2180A	T1 Transceiver	1
U4	DS1231	Power Monitor	1
U5, U12	74HC04	Hex Inverter	2
U6	74HC00	Quad NAND	1
U7, U8	LM555	Timer	2
U9	74HC157	Quad 2:1 Mux	1
U10, U11	74HC163	Binary Counter	2
X1		3.088MHz Oscillator	1
C1,C2,C3		10uF, 10V Tantalum Cap	3
R1,R8,R9		22K, 1/4W, 5% Resistor	3
R2 to R7		330, 1/4W, 5% Resistor	6
RP1 to RP3		100K Resistor Pack (9)	3
J1, J2		Bantam Jack	2
J3, J4		Banana Jack	2
SW1		4P3T Slide Switch	1
SW2 to SW4		8-Position DIP Switch	3
LED 1 to 6		Red LEDs	6
		0.1uF Bypass Capacitor	13

APPENDIX D : DS2190DK SCHEMATIC



REF	DEVICE	VDD	VSS
U1	DS2190 NETWORK INTERFACE UNIT	22	21
U2	EP900J PROGRAMMABLE LOGIC DEVICE	1,44	22,23
U3	DS2180A TRANSCEIVER	40	20
U4	DS1231 POWER MONITOR	8	4
U5,U12	74HC04 HEX INVERTER	14	7
U6	74HC00 QUAD NAND	14	7
U7,U8	555 TIMER	8	1
U9	74HC157 QUAD 2:1 MUX	16	8
U10,U11	74HC163 4-BIT BINARY COUNTER	16	8
U13	74HCT244 OCTAL BUFFER/TRANSCEIVER	20	10
X1	3.088MHZ CRYSTAL CLOCK OSCILLATOR	8	4



NOTES:

1. BYPASS U1-U13 AND X1 WITH 0.1UF.
2. SOCKET U1, U2, AND U3.
3. U13, C4, R10, AND J5 ARE OPTIONAL.
4. PROGRAM U2 WITH 'DATAGEN' FUNCTION.

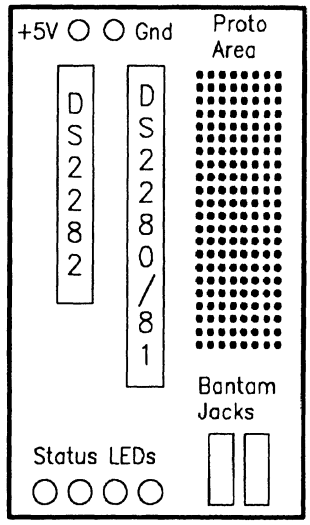
DALLAS SEMICONDUCTOR

DS2280DK
T1 LINE CARD Stik™ DESIGN KIT

FEATURES

- Demonstrates Dallas Semiconductor's entire T1 chip set via the DS2280 T1 Line Card Stik and the DS2282 FDL Controller/Monitor Stik
- Contains software that will enable a IBM- compatible PC to communicate with either the DS2280 or DS2282
- Contains SIP Stik connectors for the DS2280 and DS2282
- Eurocard size; can be mounted in the DS9005 Eurocard Enclosure
- Easily accessible test points
- Prototyping wire-wrap area for user customization
- Can also be used with the DS2281 CEPT Line Card Stik
- Powered by a single +5V supply

KIT LAYOUT



NOTE:
The DS2280DK does not contain the DS2280, DS2281, or DS2282.

DESCRIPTION

The DS2280DK allows the user to evaluate Dallas Semiconductor's line of T1 products. The design kit is set up to demonstrate the DS2280 T1 Line Card Stik and the DS2282 T1 FDL Controller/Monitor. It is arranged to provide maximum flexibility and is easily customized to meet the user's needs. Software is provided to allow an IBM PC or compatible to communicate with the DS2280 and DS2282. Since the DS2281 CEPT Line Card Stik shares the same pinout as the DS2280, the DS2280DK can be used to evaluate the DS2281 as well as the DS2280. Please contact the factory for more information about this product.

APPLICATION NOTES

9

DALLAS
SEMICONDUCTOR

T-CARRIER CHIP SET APPLICATION NOTE

T-CARRIER CHIP SET ADAPTS TO CHANGING NETWORK STANDARDS

As T1 gains mainstream acceptance as the backbone of high-speed communications, ICs that meet the timing, control and compatibility demands of T1 electronics are becoming a necessity.

The interconnection of personal computers, terminals and telephones in the business environment is experiencing explosive growth. T1 is a cost effective means of linking such automated offices, and serves as an alternative to high speed modems in the data transport environment. T1 is a high-speed digital network (1.544 MHz) developed by AT&T in the early 1960s to support long-haul pulse-code modulation (PCM) voice transmission. Although twisted-pair copper wire is the primary transmission medium, multiple T1 networks are supported by optical fiber, microwave and satellite links. T1 (also known as DS1) is the primary interface between the local telephone operating companies and long distance carriers such as MCI, LDS and AT&T. The local operating companies also utilize T1 in subscriber line carrier systems (SLC-96) to connect remote subscribers to the central office.

As the development of support ICs for T1 networks becomes a crucial design issue, three major design challenges for T1 electronics have emerged: framing and synchronization, control and status monitoring and backplane compatibility. A new chip set from Dallas Semiconductor, which consists of the DS2180 Serial T1 Transceiver and DS2176 T1 Receive Buffer, addresses all three challenges. This chip set, implemented in low-power CMOS technology, is compatible with both North American and Far East T-carrier networks. It supports a wide variety of features, including D4 framing, extended framing, bipolar eight zero substitution (B8ZS) and total transparency zero suppression modes. In addition, the DS2180 eliminates the substantial off-board logic necessary to interface to system control circuitry.

STANDARDS AND SERVICES

Many large corporations have utilized leased T1 lines for point-to-point data networks. These lines are higher speed cousins of the traditional leased-line modem networks. The nonswitched networks are often incompatible with each other and with the Bell system equipment, and are becoming increasingly obsolete.

The competitive atmosphere generated by divestiture has reduced the cost of T1 connections and has accelerated the introduction of special data services based on T1. These new switched services require equipment compatible with Bell system equipment, and offer performance superior to leased-line alternatives. Customer controlled reconfiguration (CCR) is one such service in which cost is based on the percentage of link utilization. CCR is cost effective at data rates that use 20 to 25 percent of the available T1 bandwidth.

The existing T1 network must be upgraded to handle the demands of increasing data traffic. These upgrades include full data transparency and extended framing. Transparency eliminates the data corruption caused by existing signaling and zero suppression techniques. Extended framing provides the network with a 4-kbit data channel, which is used for alarm and error-rate monitoring. The data channel lets the network police itself, providing superior line-fault analysis.

T1 networks can also be used on-site as an alternative to LANs in the office environment. Currently, two computer-to-PABX interface specifications based on T1 technology exist. The Digital Multiplexed Interfaced (DMI) standard is supported by AT&T Information Systems and Hewlett-Packard. The Computer-Peripheral-Interface (CPI) standard is backed by Northern Telecom and Digital Equipment Corp. This widespread acceptance of T1 as a prime mover of voice and data is turning it into the "RS-232" of telecommunications.

Companies developing T-carrier equipment include those specializing in PCM switching and transmission, office automation, modem and communications networks and private automatic branch exchanges (PABX) with data capability.

FRAMING AND SYNCHRONIZATION

The first challenge in designing ICs for T1 is framing and synchronization. In the Dallas Semiconductor chip set, the DS2180 transceiver handles these functions. It supports extended framing, D4 framing and derivatives of D4, such as SLC-96. In addition, features such as bit 7 stuffing (a zero suppression technique), bipolar eight zero substitution (B8ZS) and total transparency zero suppression modes are included in the device. The transceiver has autonomous transmit and receive sides. An on-board serial port links the device to a host microprocessor/microcontroller for supervision and control.

The transmit side of the DS2180 is made up of six major functional blocks: a timing and clock generator, a yellow alarm circuit, an F-bit data section (F-bit refers to the first bit transmitted), a cyclic redundancy check (CRC) section and a data selector bipolar coder. The timing and clock-generation circuit develops all on-chip and output clocks from three signal inputs (TCLK, TFSYNC and TMSYNC). The output clocks identify robbed-bit signaling (which indicates the telephone on/off-hook status) and link-data frames, making them useful for data conditioning and decoding. The rising edge of the sync inputs must be aligned with the transmit clock. Data inputs are sampled on the falling edge of the clock signal, while updated outputs occur on the rising edge. The timing inputs on the transmit side may be slaved to receive side outputs for use in drop-and-insert applications. This timing sequence is compatible with most combo-codecs.

The yellow alarm circuitry generates mode-dependent alarms for transmission into the network. The F-bit data block develops the synchronization pattern that is embedded in the outgoing data stream. The CRC circuitry subsection produces check-sum codes that are utilized in extended framing. These three subsections feed into the data selector, which builds the outgoing serial data stream via bit selection and insertion. The bipolar coder reformats the data selector output into an alternative mark inversion (AMI) format and inserts the selected zero suppression techniques. The bipolar coder also supports an on-chip loopback feature.

The heart of the receiver is the synchronizer/sync monitor, which monitors the incoming data stream for loss of frame or multiframe alignment, and searches for new alignment when synchronization loss is detected. The synchronizer uses a sophisticated, memory-intensive frame-search algorithm. Unlike earlier devices, this algorithm displays no sensitivities to emulators of the framing pattern sequence, such as digital milliwatt. It also rejects randomly induced patterns generated by network testing equipment that mimic synchronization patterns.

The Receive Control Register allows the user to tailor the characteristics of the sync algorithm to unique applications. Typical synchronization times are 4 ms (D4 framing) and 8 ms (extended framing). The resynchronization sequence occurs off-line. (The receive output timing "rolls" at the "old" alignment until the sync search is completed.) When the new frame and multiframe alignments are identified, the output timing set is jammed to the timing position of the next multi-frame boundary. When synchronization is established, the synchronizer is disabled to save power.

The output timing on the receive side is identical to the transmit timing; the bipolar decoder, yellow alarm detector and CRC circuitry are complements of those blocks used on the transmit side of the device. Alarm conditions detected on the receive side (loss of synchronization, carrier loss, framing error) appear as outputs and are reported to the status and error-count registers. The Receive Mark Register allows idle or digital milliwatt codes to be selectively inserted over incoming channels. This feature can be used in channel-unit applications for channel-level adjustment and field service.

CONTROL AND STATUS MONITORING

A major disadvantage of most first-generation transceivers is that they require substantial off-board logic to interface to system control, or they support rigid control protocols which limit the host control options of the designer. The DS2180's on-board serial port utilizes a simple synchronous protocol and interfaces directly to popular microprocessors/microcontrollers, such as the 8051. Sixteen registers establish the device's operating characteristics and report error status and alarm conditions. This flexible control architecture eliminates support hardware and minimizes processor overhead.

The read/write timing for the port used to access the registers is independent of the transmit and receive timing. This read/write timing is compatible with the 8051 on-board serial port operating in mode 0. With a master clock of 12 MHz, the 8051 can write or read a single register in less than 25 *us*. In addition, a burst mode allows all registers to be consecutively read or written.

The basic operational control characteristics of the transceiver are established by the Common Control, Transmit Control and Receive Control Registers (CCR, TCR and RCR). The CCR establishes frame, zero suppression and yellow alarm modes. A local loopback, which internally ties the transmit clock and data outputs to the receive clock and data inputs, is also enabled by the CCR. The TCR supports blue (unframed "I's") and yellow alarm transmission. Robbed-bit signaling and D4 framing insertion modes are also selected by the TCR. The RCR establishes synchronizer characteristics and selects the code word type that may be inserted in each outgoing channel.

Three other register sets are used to eliminate the off-chip control hardware that is used in existing designs. The Transmit Idle Register (TIR) allows the user to insert an idle code sequence into any outgoing channel data. The Transmit Transparency Registers (TTR) are used to disable robbed-bit signaling insertion and bit seven zero suppression on a per-channel basis. The Receive Mark Registers (RMR) replace selected incoming DS0 channels with a digital milliwatt or idle code (as selected by the RCR).

Status monitoring is handled by the Receive Status Register, which reports alarm conditions, such as a loss of synchronization, yellow alarm, carrier loss, blue alarm and error-count saturation. Unless disabled by the Receive Mask Register, any one of these events will generate an interrupt. On-board error event counters allow the device to log error events, such as bipolar violations and frame bit errors. When the error counters exceed a preprogrammed threshold, they will also generate an interrupt (unless masked). This logging capability eliminates the need for off-chip error counting logic and minimizes processor overhead. Error-event service routines may be poll or interrupt-based, depending on the system requirements.

The DS2180 also has the ability to operate in hardware mode. For preliminary system prototyping or for applications which do not require serial port features, the transceiver may be reconfigured into a hardware mode. This disables the port, clears all internal registers and redefines all serial port pins as mode control inputs. This mode allows device retrofit into existing applications where mode control and alarm conditioning are performed with discrete logic. The mode control inputs establish device framing, zero suppression, alarm and F-bit insertion characteristics.

BACKPLANE COMPATIBILITY

The Dallas Semiconductor DS2176 T1 Receive Buffer is the first T-carrier product which lets the user link transceivers to a variety of system backplanes. The DS2176 compensates for jitter and wander in the receive clock, serves as a rate buffer for backplane frequencies other than 1.544 MHz, interfaces directly to serial or parallel backplanes and supervises robbed-bit signaling.

Although the received T1 data stream averages 1.544 MHz, the data displays significant high-frequency jitter and low-frequency wander. These characteristics result from

the less-than-perfect transmission characteristics of a repeated T1 span line. An elastic store, based on first-in, first-out (FIFO) memories and discrete contention logic, is required to interface transceivers to system backplanes.

The DS2176 uses an on-chip PCM buffer to synchronize incoming data to system backplane frequencies, eliminating the need for the elastic store. The buffer depth is two frames (386 bits), which is more than adequate for most applications in which short-term jitter and wander compensation is required. This buffer "slips" whenever it is completely emptied or filled, recentering its depth to one frame. (The buffer can also be externally recentered.) Slip occurrences are reported at the SLIP output. In addition, a set of signals (System Multiframe Sync and Receive Multiframe Sync) can be used to monitor buffer depth in real time.

SIGNALING SUPERVISION

Signaling data embedded in the PCM data stream is extracted and output by the DS2176. The signaling buffer in the DS2176 allows the device to freeze the signaling outputs during slip or alarm conditions. This meets the Bell system requirements for prohibiting updates when sync or carrier signals are lost.

Signaling integration is another important feature of the DS2176. When selected, it minimizes the impact of random noise on the signaling information. For signaling integration, the channel signaling data must be in the same state for two or more multiframes before being updated at the signaling outputs. For the DS2176, two inputs are used to select the degree of integration or totally bypass the feature. The processed signaling data is not re-merged with the outgoing channel word. This maintains data integrity in mixed voice-data or data-only environments.

A T1 TUTORIAL

T1 transmission is based on twisted pair wiring, with separate pairs used for the transmit and receive sides. T1 links require a repeater circuit every 6,000 feet to regenerate the attenuated signal; an "office repeater" is required when a loop terminates into station electronics. Higher rate transmission systems based on optical fibers are gaining widespread use. DS3 is one such system; at 45 MHz, it is made up of 28 T1 (DS1) lines.

In T1, data is transmitted in an alternate mark inversion (AMI) format, which allows clock signals to be derived from data, eliminating the need for separate clock transmission. The clock signal is extracted from the AMI waveform using phase-locked loops or LC tank circuitry. Clock extraction circuitry requires a minimum density of "1's" to operate correctly. To meet this density requirement—networks cannot transmit a code consisting solely of zeros—existing T-carrier equipment changes bit 7 of any channel consisting solely of "0's" to 1. Bit 7 stuffing does not affect the quality of voice transmission, but it does corrupt data significantly. An alternative to bit 7 stuffing is bipolar eight zero substitution (B8ZS), which replaces any transmitted zero octet with a B8ZS code word. If the last "1" transmitted was positive, the inserted word is 000 + -0- + . If the last "1" transmitted was negative, the code word inserted is 000 – + 0 + – . Bipolar violations occur in the fourth and seventh bit positions, but these are ignored by the receive alarm circuitry when B8ZS is enabled. The receive side detects the code word and replaces it with all zeros.

Framing refers to the format for data signaling, alarm and synchronization information on the T1 trunk. A frame of data is made up of 193 bits, and is transmitted every 125 *us*. The first bit transmitted is known as the F-bit. The F-bit position is used for synchronization, alarm and network data link. The F-bit is followed by 24 voice or data channels, each channel being eight bits wide. These channels (known as DS0 channels) each have a data rate of 64 kbits/s.

Multiple frames make up a superframe (multiframe). One Extended Superframe consists of 24 frames. Twelve frames make up one D4 superframe.

Signaling information (telephone on-hook/off-hook status, known as robbed-bit signaling) is written over the least significant bit (LSB) of each channel every six frames. Newer systems avoid this type of data corruption by moving all signaling information to a separate DS0 channel. The use of common-channel signaling and newer zero suppression techniques such as B8ZS enhance the network's ability to carry data. This capability is known as "clear channel."■

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DS2180
SUPERVISORY SOFTWARE APPLICATION NOTE

INTERFACING THE DS2180 T1 TRANSCEIVER TO 8051/31 MICROCONTROLLERS

This application note provides users of the DS2180 T1 Transceiver with some 8051 software examples. All of the software presented makes use of the serial control port of the DS2180, which allows access to 16 internal registers devoted to device control, configuration and status monitoring. The serial port consists of 5 pins: SDI, SDO (serial data in and out), SCLK (serial data clock in), $\overline{CS}$ (chip select) and $\overline{INT}$ (interrupt output). Although the port is very general-purpose, this application note concentrates on interfacing specifically with an 8051 processor. When configured in mode 0, the serial port of the 8051 mates perfectly with the serial port of the DS2180, requiring no external logic. This circuit hook-up is shown in Figure 1.

Circuit operation is very straightforward. RXD on the 8051 is a bi-directional serial bus for data in and out of the part. The TXD pin provides a serial data clock to the DS2180, allowing the transceiver to sample data on rising clock edges. A normal port pin (P1.0) enables the DS2180's port by transitioning low. The remaining connection, INT0, processes interrupt requests from the DS2180's $\overline{INT}$ output. Because this output is open-collector, a resistor pull-up is necessary to define the high state. Use of the $\overline{INT}$ output is strictly up to the user and usually depends on whether processor control is polled or interrupt-based.

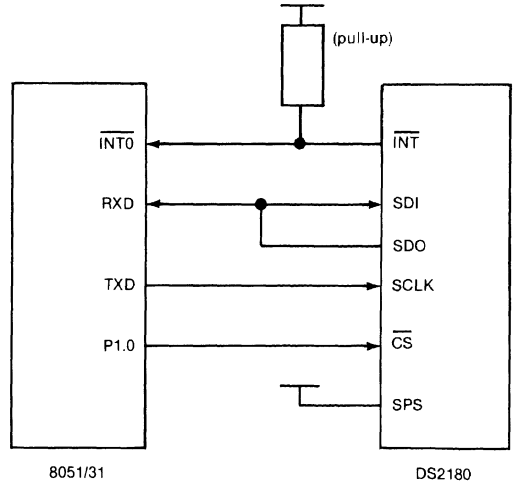
Speed through the port can be very rapid and is determined by the processor internal clock. For example, if the 8051 is running at 12 MHz, then the serial clock output at TXD will be 1 MHz (a ÷ 12 of the master clock), which leads to typical read/write times of less than 25 *u*sec. Because of the $\overline{CS}$ input, several DS2180s can be supervised by the same processor by tying the clock and data lines together, and selecting each DS2180 by its $\overline{CS}$ input.

The first two software examples concentrate on how to transfer data between the 8051 and the DS2180 using the serial port. Both methods of transfer—burst and random—are supported. (Burst mode means all registers are accessed consecutively, while random mode means accessing one specific register.) The third and last example shows how DS2180-generated interrupts might be handled, specifically those interrupts caused by on-chip counter saturations. This software is useful when the user is building code to calculate BERs (bit-error-rate) for bipolar violations, CRC-6 checksum errors, loss-of-sync occurrences (OOFs) etc. Note that the software using the DS2180 internal counters obsoletes the need for external error count logic, reducing board area and cost.

Finally, this software is not meant to be a stand-alone program: it simply illustrates subroutines that may be incorporated into a larger program.

DS2180/8051 SUGGESTED HOOK-UP

Figure 1



SERIAL PORT READ ROUTINES Example 1
Purpose: Read registers from the 2180 via the serial port

Arguments: Burst mode
RO Count of bytes to receive (16)
DPTR External memory location

Random Access mode
R1 T1 register address (0-15)
ACC Data returned from DS2180

```
;
; Process burst read request
;
T1_BURST_READ:    PUSH    DPL             ;save data pointer low
                  PUSH    DPH             ;save data pointer high
                  MOV     R1,#81H         ;burst read command byte
                  SJMP    T1_RD           ;begin serial byte transfer
;
T1_RANDOM_READ:   PUSH    DPL             ;save data pointer low
                  PUSH    DPH             ;save data pointer high
                  MOV     R0,#1H          ;only 1 byte to transfer
                  MOV     DPTR,#FFFFH     ;point to dummy location
                  XCH     A,R1            ;get the T1 reg address
                  ANL     A,#0F           ;mask out invalid bits
                  RL      A               ;shift left one bit
                  ORL     A,#1H           ;indicate a read function
                  XCH     A,R1            ;....and save the result
;
; Begin reading data from the serial port (RXD, TXD)
;
T1_RD:            SETB    P1.0            ;disable DS2180
                  CLR     P1.0            ;enable DS2180
                  PUT_SERIAL_PORT R1 (write command byte)
;
T1_RLP:           GET_SERIAL_PORT A (read data byte)
                  MOVX    @DPTR,A         ;store this byte
                  INC     DPTR            ;point to next destination byte
                  DJNZ    R0,T1_RLP       ;continue until all reg done
                  SETB    P1.0            ;set DS2180 CS pin high
                  RET                     ;return to caller
```

MACRO DEFINITIONS

```
.MACRO          PUT_SERIAL_PORT         REG
                CLR         SCON.REN    ;disable serial receive
                CLR         SCON.T1     ;clear transmit done flag
                MOV         SBUF, REG   ;write serial byte
          LBL1: JNB         SCON.T1,LBL1 ;wait until transfer complete
                CLR         SCON.T1     ;clear transmit done flag

.MACRO          GET_SERIAL_PORT         REG
                SETB        SCON.REN    ;enable serial receive
                CLR         SCON.R1     ;read serial byte
          LBL2: JNB         SCON.R1,LBL2 ;wait until transfer complete
                MOV         REG,SBUF    ;fetch the byte just read
                CLR         SCON.REN    ;disable serial receive
```

SERIAL PORT WRITE ROUTINES Example 2
Purpose: Write registers to the 2180 via the serial port

```
Arguments:   Burst mode
         RO  Count of bytes to transmit (16)
       DPTR  External memory location

             Random Access mode
         R1  T1 register address (0-15)
        ACC  Data value for transfer
;
; Process burst write request
;
T1_BURST_WRITE:  PUSH        DPL         ;save data pointer low
                 PUSH        DPH         ;save data pointer high
                 PUSH        ACC         ;save caller's accumulator
                 MOV         R1,#80H     ;burst mode command byte
                 MOVX        A,@DPTR     ;get first data byte
                 SJMP        T1_WT       ;begin actual transfer
;
; Process random write request
;
T1_RANDOM_WRITE: PUSH        DPL         ;save data pointer low
                 PUSH        DPH         ;save data pointer high
                 PUSH        ACC         ;save caller's accumulator
                 MOV         R0,#1H      ;only 1 byte to transfer
                 MOV         DPTR,#FFFFH ;point to dummy location
                 XCH         A,R1        ;retrieve DS2180 address
                 ANL         A,#0FH      ;mask out invalid bits
                 RL          A           ;shift left 1 bit
                 XCH         A,R1        ;....and save the result
```

```
;
; Begin writing data out to the serial port
;
T1_WT:      SETB    P1.0            ;disable DS2180
            CLR     P1.0            ;enable DS2180
            PUT_SERIAL_PORT R1 (write command byte)
;
T1_WLP:     PUT_SERIAL_PORT A (write data byte)
            INC     DPTR            ;point to next byte
            MOVX    @DPTR,A         ;store this byte
            DJNZ    R0,T1_WLP       ;continue until all reg done
            SETB    P1.0            ;disable DS2180
            RET                     ;return to caller
```

SOFTWARE FOR PROCESSING COUNTER-GENERATED INTERRUPTS FROM THE DS2180 Example 3

This routine processes interrupts on the INT0 line (Pin 12 of the 8051), generated by the $\overline{INT}$ output of the DS2180. In general any alarm bit set in the receive status register (RSR) will cause the $\overline{INT}$ pin to go low if the corresponding bit in the receive interrupt mask register (RIMR) is also set. This software example responds to interrupts generated by either a BVCS (bipolar count saturation) or an ECS (error count saturation) event. While the BVC counter is a full 8-bit counter, the ECR consists of two separate 4-bit counters in the same register. The high nibble increments on loss-of-sync occurrences and the low nibble increments on F-bit errors (the type of F-bit errors are mode-dependent). Saturation of either 4-bit counter will set the ECS bit in the RSR register.

Program flow is as follows: when an interrupt occurs, the RSR register is read to determine which counter saturated. The memory location mapping to the appropriate saturated counter is then incremented to keep a running tab of saturation occurrences. The counter in question is reloaded with a user-determined threshold before the routine returns control to the main program. This routine assumes that RIMR.7 and RIMR.6 have already been set high to allow counter-generated interrupts to occur.


```
;
; Define the external memory addresses used by this routine
;
T1_BVC_RELOAD = #0H             ;bipolar count threshold
T1_ECR_RELOAD = #1H             ;error count threshold
T1_BVC_ERRORS = #2H             ;bipolar sat count
T1_ESF_ERRORS = #3H             ;low nibble ECR sat count
T1_OOF_ERRORS = #4H             ;high nibble ECR sat count
;
; Read the T1 receive status register (RCR)
;
ERRCHK:  MOV    R1,#T1_RSR          ;load register address
         LCALL  T1_RANDOM_READ      ;read one T1 register
         JB     A.7,BVCS            ;process bipolar count sat
         JB     A.6,ECS             ;process error count sat
         SJMP   INTO_R              ;....or terminate interrupt
```

```
;
; Process a bipolar violation count saturation by first reloading the user-defined count thresh-
; old and then incrementing the running count memory location (T1_BVC_ERRORS).
;
BVCS:   MOV     DPTR,#T1_BVC_RELOAD
        MOVX    A,@DPTR             ;fetch BVC count threshold
        MOV     R1,#T1_BVCR         ;fetch BVCR address
        LCALL   T1_RANDOM_WRITE     ;write one T1 register
        MOV     DPTR,#T1_BVC_ERRORS
        MOVX    A,@DPTR             ;fetch running count
        INC     A                   ;increment count by 1
        MOVX    @DPTR,A             ;put new count back
;
; Now check for any other counter saturation
;
        SJMP    ERRCHK
;
; Process error count saturation by a similar procedure except that we must determine which
; nibble of the ECR is affected. Then only the counter saturated is reset to the user-specified
; value.
;
ECS:    MOV     R1,#T1_ECR          ;load register address
        LCALL   T1_RANDOM_READ      ;read one T1 register
        MOV     RO,A                ;store ECR count in RO
        ANL     A,#0FH              ;mask to get low nibble
        XRL     A,#0FH              ;xor to see if saturated
        JNZ     ECS_OOF             ;if not, must be high nibble
        MOV     A,RO                ;restore ECR count
        ANL     A,#F0H              ;mask to save high nibble
        MOV     RO,A                ;save high nibble
        MOV     DPTR,#T1_ECR_RELOAD
        MOVX    A,#DPTR             ;get ERC threshold value
        ANL     A,#0FH              ;mask to get low nibble
        ORL     A,RO                ;or high and low nibbles
        MOV     RO,A                ;save as new ERC count
;
; Now increment the low nibble (T1_ESF_ERRORS) running count
;
        MOV     DPTR,#T1_ESF_ERRORS
        MOVX    A,@DPTR             ;fetch ESF running count
        INC     A                   ;increment count by 1
        MOVX    @DPTR,A             ;put new count back
```

```
;
; Now check for high nibble (OOF counter) saturation and process this event similarly.
;
ECS_OOF: MOV     A,RO                    ;restore ECR count value
         ANL     A,#F0H                  ;mask to get OOF count
         XRL     A,#F0H                  ;xor to see if saturated
         JNZ     ERRCHK                  ;if not, then we are done
         MOV     A,RO                    ;restore ECR count value
         ANL     A,#0FH                  ;mask to save low nibble
         MOV     RO,A                    ;save low nibble
         MOV     DPTR,#T1_ECR_RELOAD
         MOVX    A,@DPTR                 ;get ECR threshold values
         ANL     A,#F0H                  ;mask to save high nibble
         ORL     A,RO                    ;or high and low nibble
         MOV     RO,A                    ;save as new ECR count
         MOV     DPTR,#T1_OOF_ERRORS
         MOVX    A,@DPTR                 ;get OOF running count
         INC     A                       ;....and increment by 1
         MOVX    @DPTR,A                 ;put new count back
;
; Finally, write new value of ECR back into the T1 (DS2180) Transceiver.
;
ECS_WT:  MOV     A,RO                    ;transfer new count to ACC
         MOV     R1,#T1_ECR              ;load T1 ECR address
         LCALL   T1_RANDOM_WRITE         ;write one T1 register
INTO_R   RET                             ;return to main program
```

DALLAS
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DS2180/DS2176
T1 DEMO KIT
APPLICATION NOTE

DS2180/DS2176 T1 DEMO KIT

This application note describes the Dallas Semiconductor DS2180/DS2176 T1 demonstration kit. The DS2180 T1 Transceiver is a single-chip CMOS device that integrates all the digital control circuitry necessary for supervising T1 lines operating at 1.544 Mbits/sec. The DS2176 Receive Buffer is a companion part (also CMOS) that integrates the elastic store and robbed-bit signaling buffer functions typically required for a T1 line card. Used together, they provide an optimum, efficient solution for complicated T1 interface problems.

T1 KIT CONTENTS

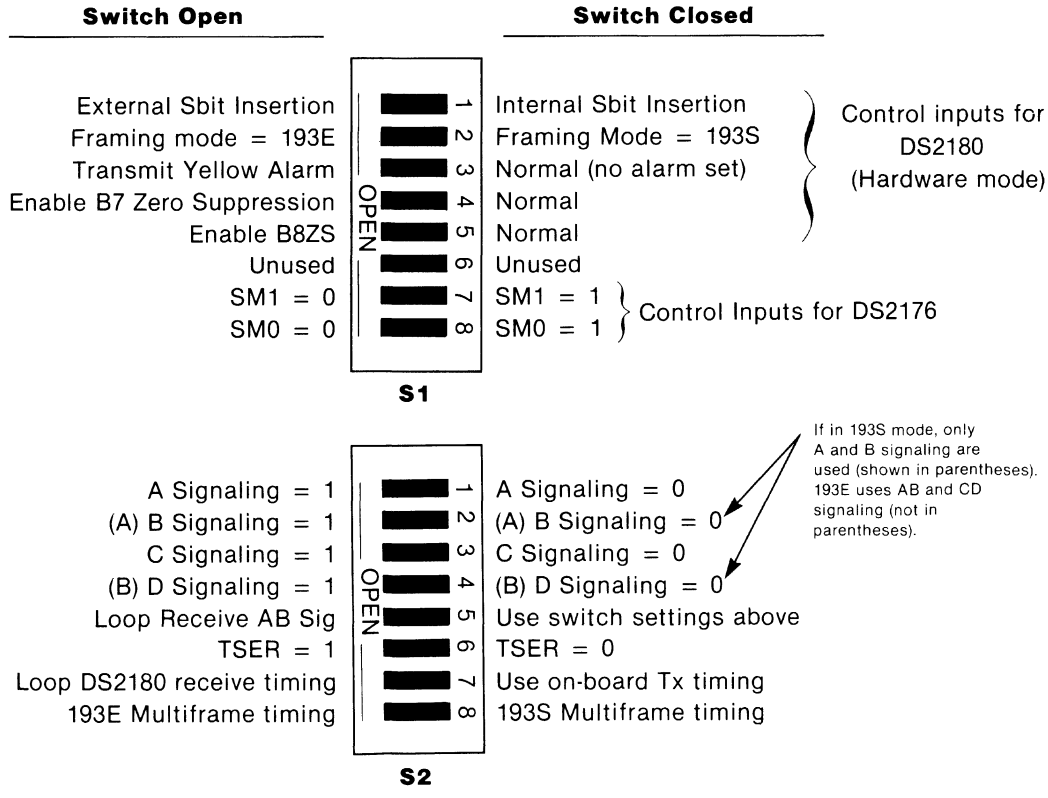
The kit contains a printed-circuit board which permits easy evaluation of the DS2180/DS2176 parts. On-board circuitry generates all the different timing necessary for operation of the transmit side of the DS2180. The user also has the ability to insert ABCD robbed-bit signaling into the transmit T1 data stream and/or to loop the receive-side timing and data to the transmit-side of the DS2180 for emulating drop-and-insert applications.

The kit also includes a 1.544 MHz crystal, resistor pull-ups, HCMOS logic parts, the DS1231 Power Monitor and, of course, samples of the DS2180 and DS2176. Remaining components may be obtained from a local electronics distributor. The parts list for these items appears at the back of this document.

PCB DESCRIPTION

The PCB contains the digital logic necessary for generating transmit timing and for multiplexing internal signals. Two banks of switches are used for selecting operating modes, signaling states, and timing configuration.

Figure 1 **BOARD SWITCH SETTINGS**



Holes in the board are intended for the user to insert banana plugs for VDD and GND and BNC connectors for unipolar NRZ data and clock. For adding additional circuitry (such as a line interface), a small wire-wrap area is provided.

In order to stuff the board, silkscreening shows the locations of all the components specified in the parts list. Brief mnemonics on the switch locations should help in selecting options; however, a full switch explanation is shown in Figure 1 and can also be inferred from the board schematic shown in Figure 2. Although not numbered, decoupling capacitors on all ICs are recommended and their locations are outlined on the board, usually at the top of the IC (near Pin 1).

TRANSMIT TIMING AND DATA

The master clock for transmit is generated by a 1.544 MHz Pierce crystal oscillator whose buffered output is available at U8-6 (Pin 6). From this clock the frame and multiframe sync pulses are derived. Frame sync is a one-clock-wide pulse with a frequency of 8 KHz. Multiframe sync is also a one-clock-wide pulse but with a period of either 12- or 24-frame sync pulses, depending upon the state of switch S2-8 (193E/193S). 12-frames-per-multiframe is used in D4 systems while 24-frames-per-multiframe is used in the emerging ESF format. *It is important that this selection be compatible with the DS2180 framing mode selected by switch S1-2.*

U12 is a multiplexor chip that determines which timing set is fed to the DS2180 transmit sync inputs (TMSYNC, TFSYNC, TCLK): either the normal crystal-derived timing mentioned above or the receive-side output timing signals of the DS2180. Also selected is the data origin for transmit data into the DS2180 (TSER): either switch S2-6 or looped from the receive data output of the DS2180 (RSER).

Please note that the transmit frame and multiframe pulses are not required by the DS2180 and are only included on the board to allow testing of all possible timing applications. In fact, by tying the TMSYNC and TFSYNC input low, the internal counters will derive both of these signals. (The internal multiframe sync will be indicated by TMO.) Please refer to the DS2180 data sheet for full details on transmit timing operation.

TRANSMIT SIGNALING INSERTION

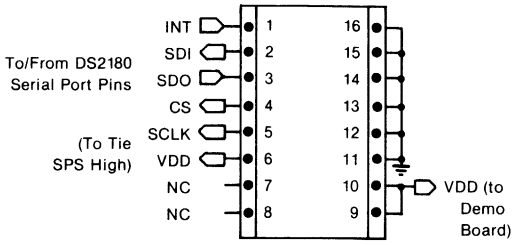
Robbed-bit signaling is input to the DS2180 at Pin TABCD and comes from the output of U13, another multiplexer chip. 4- or 16-state signaling (AB in D4 mode and ABCD in ESF mode) can be programmed by S2-1 through S2-4. Alternately, the user may loop receive-side buffered AB signaling from the DS2176 into the TABCD input. (Looping of 16-state signaling is not supported on the board.) S2-5 (RABCD/MAN SIG) determines which signaling configuration is selected.

DS2180 OPERATING MODES

If switch S1 is used on the demo board, it will configure the DS2180 transceiver in the hardware mode, where operating modes are selected by tying pins high or low. This is in contrast to the DS2180's serial-port mode whereby a serial port interface allows access to internal registers that determine those same operating modes as well as many others. Tying the SPS pin (Pin 19) low selects the hardware mode, while tying it high activates the serial-port interface. Note on the schematic that using S1 automatically ties SPS low.

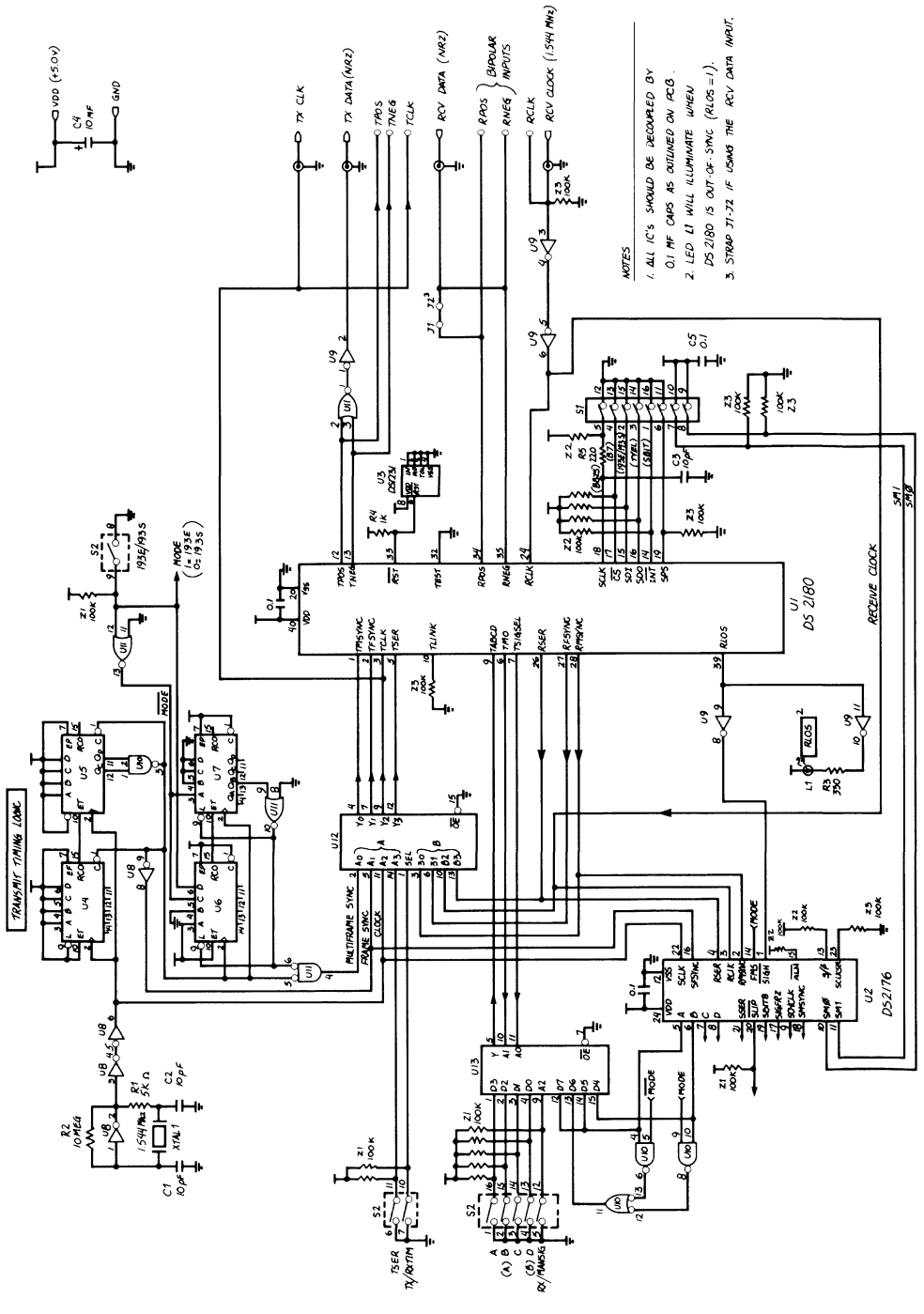
To evaluate the serial port operation of the DS2180, the user may use a 16-pin header connected via a ribbon cable to his software development station. The header would then fit into the socket vacated by S1. The required pinout for header is shown in Figure 3 and is also implied on the schematic. Note that power and ground are assumed to origi-

Figure 3
SERIAL PORT HEADER PINOUT (S1)



Pinout shows assignment of port signals when S1 is not used and ribbon cable header is connected from User Development Station.

Figure 2 **DS2180/DS2176 DEMO BOARD SCHEMATIC**



nate from the development station instead of the banana plugs. Power is required on Pin 6 of the header in order to tie SPS high. The low-pass filter formed by R5 and C3 may be necessary to minimize excessive undershoot and ringing caused by long ribbon cables. Please refer to the DS2180 data sheet for a full explanation of the serial port interface and its required timing.

DS2180 INTERFACE FORMAT

Transmit and receive data can be handled in two different ways on the demo board. For applications using the NRZ unipolar format, data and clock can be supplied to and from the BNC connectors. To use the BNC connector path for RCV DATA, jumper pads J1 and J2 must be strapped together. However, in order to interface to bipolar digital data, some solder pads are provided for accessing the bipolar inputs and outputs of the DS2180. The transmit bipolar pads are TPOS and TNEG while the receive bipolar inputs are RPOS and RNEG.

Clocking for transmit data out is available at either the BNC connector or the solder pad labeled TCLK. Data present at TPOS and TNEG or at the BNC connector is updated on rising edges of transmit TCLK. Receive data present at either the RCV DATA connector or at the bipolar inputs is sampled by falling edges of RCV CLOCK (or RCLK if using the solder pad).

DS2180 SYNC INDICATOR

When the DS2180 is in a resync mode, searching for the framing pattern, the RLOS pin will go high. This will illuminate L1, a small red LED. When the part has established proper sync, RLOS will return low and the LED will go out.

DS1231 POWER MONITOR/POWER-ON RESET

Initialization of the DS2180 is accomplished by tying the $\overline{RST}$ input low for some brief time when power is first applied. The DS1231 performs this task and also monitors power for voltage glitches that a simple RC network would otherwise miss. Power-on reset for the DS1231 nominally lasts 500 msec, during which time the DS2180 will be out-of-sync.

DS2176 OPERATION

The main job of the DS2176 is to synchronize the incoming T1 line frequency to the system data clock. Long-term differences in frequency are resolved by the use of controlled slips, whereby a frame of data is either deleted or repeated. On the demo board, the T1 clock line is RCLK and the system clock is the crystal-derived transmit clock. Slip occurrences can be monitored at the SLIP pin on the DS2176.

By default on the board, the DS2176 receive buffer is configured in the serial data ($S/\overline{P} = 1$) and the 1.544 MHz system clock modes (SCLKSEL = 0). However, the type of signaling buffer configuration can be changed by use of switches S1-7 and S1-8 (which tie SM0 and SM1 high or low). Please consult the DS2176 data sheet for details on proper selection for your application.

TEST POINTS

Surrounding both the DS2180 and the DS2176 are open pads in which small test pins may be soldered for conveniently attaching scope probes.

PARTS LIST FOR DS2180/2176 DEMO BOARD

	ITEM #	P/N	DESCRIPTION	QTY
*	U1	DS2180	Single-chip T1 transceiver	1
*	U2	DS2176	T1 Receive buffer	1
*	U3	DS1231	Power monitor/Power-on reset circuit	1
*	U4-U7	HC163	4-Bit presettable counters	4
*	U8, U9	HC04	Hex inverters	2
*	U10	HC00	Quad 2-input NAND gates	1
*	U11	HC02	Quad 2-input NOR gates	1
*	U12	HC257	Quad 2-input data selector/multiplexer	1
*	U13	HC251	8-input data selector/multiplexer	1
*	XTAL	MP-2	M-TRON 1.544 MHz crystal	1
	R1	—	5KΩ resistor, 5%	1
	R2	—	10 Meg, 5%	1
	R3	—	330Ω, 5%	1
	R4	—	1KΩ, 5%	1
	R5	—	220Ω, 5%	1
*	Z1	710A104	Allen-Bradley SIP resistor packs (10), 100KΩ	1
*	Z2, Z3	708A104	Allen-Bradley SIP resistor packs (8), 100KΩ	2
	C1-C3	—	10 pF capacitors, 10%	3
	C4	—	10 *u*F decoupling capacitor	1
	C5	—	0.1 *u*F decoupling capacitors (on all ICs)	13
	S1, S2	76SB08	Grayhill rocker DIP switches	2
	L1	—	Red LED	1

* Indicates parts are shipped with T1 Demo Kit.

DALLAS SEMICONDUCTOR

DS2165
TIME SLOT RESTRICTIONS APPLICATION NOTE

The DS2165 ADPCM processor can input and output data in various time slots. However, since the X and Y channels share the same DSP engine, there are some restrictions on those time slots. The restrictions arise when the processor is asked to input data into both X and Y channels at the same instant of time. For example, if the frame syncs for both channels were tied together, this would occur when the X and Y channels were programmed to have the same input time slots. In applications where the X and Y channels operate asynchronously, the frame syncs to both channels have no fixed timing relationship between them. Hence, occasionally, the processor will be asked to input data into both channels at the same time, and the restrictions that will be described need to be adhered to at all times. NOTE: All the restrictions described in this application note assume that CLKX and CLKY are running at either 1.544MHz (U - Law) or 2.048MHz (A - Law). Clock rates different than these will produce different restrictions.

CASE 1

conditions:	- both X and Y channels in the compress mode - input PCM time slots for both channels are the same
restriction in U - Law:	- the output ADPCM time slots on both channels must follow the input PCM timeslot by less than 23 ADPCM (11.5 PCM) time slots
restriction in A - Law:	- the output ADPCM time slots on both channels must follow the input PCM time slot by less than 31 ADPCM (15.5 PCM) time slots
example:	- CLKX = CLKY = 1.544MHz - FSX = FSY - both X and Y channels programmed to U - Law - input PCM time slot for both X and Y channels is 2 - available output ADPCM time slots are 4 to 28

X AND Y CHANNEL PCM INPUT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

AVAILABLE X AND Y CHANNEL ADPCM OUTPUT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47

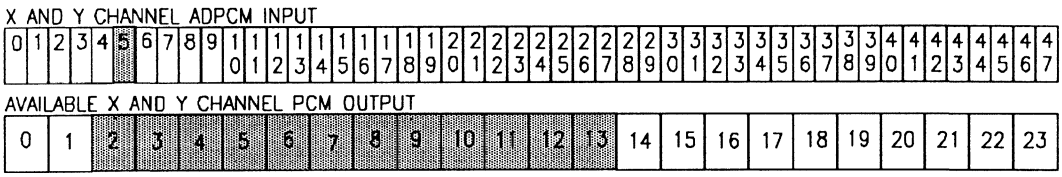
CASE 2

conditions:
- both X and Y channels in the expand mode
- input ADPCM time slots for both channels are the same

restriction in U - Law:
- the output PCM time slots on both channels must follow the input ADPCM time slot by less than 11 PCM (22 ADPCM) timeslots

restriction in A - Law:
- the output PCM time slots on both channels must follow the input ADPCM time slot by less than 15 PCM (30 ADPCM) time slots

example:
- CLKX = CLKY = 1.544MHz
- FSX = FSY
- both X and Y channels programmed to U - Law
- input ADPCM time slot for both X and Y channels is 5
- available output PCM time slots are 2 through 13



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CASE 3A

condtions:
- channel X is in the expand mode
- channel Y is in the compress mode
- input ADPCM time slot for the X channel is in the latter nibble of the input PCM time slot for the Y channel

restriction in U - Law:
- for channel X, see Case 2
- for channel Y, see Case 1

restriction in A - Law:
- for channel X, see Case 2
- for channel Y, see Case 1

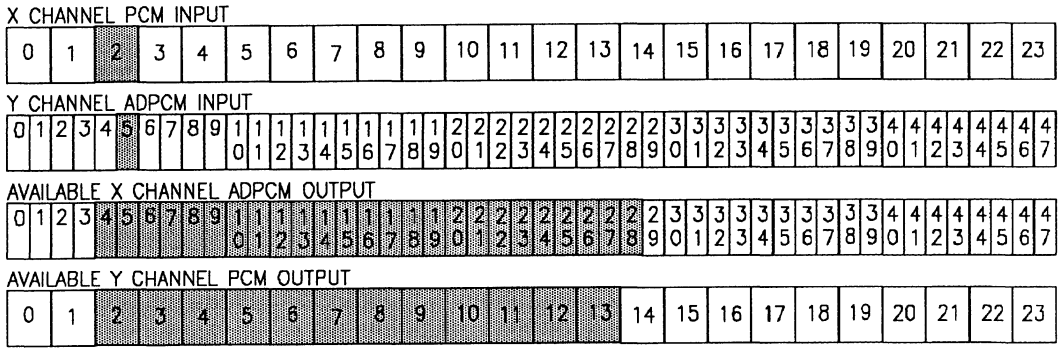
CASE 3B

conditions:
- channel X is in the compress mode
- channel Y is in the expand mode
- input ADPCM time slot for the Y channel is in the latter nibble of the input PCM time slot for the X channel

restriction in U - Law:
- for channel X, see Case 1
- for channel Y, see Case 2

restriction in A - Law:
- for channel X, see Case 1
- for channel Y, see Case 2

example:
- CLKX = CLKY = 1.544MHz
- FSX = FSY
- both X and Y channels programmed to U - Law
- input PCM time slot for channel X is 2
- input ADPCM time slot for channel Y is 5 (see Note 1)



NOTE 1: If the input ADPCM time slot for channel Y was 4 instead of 5, then there would be no restrictions on the output time slots for either channel.

CASE 4

conditions:

- channel X is in the compress mode
- channel Y is either idled or set into bypass with an input time slot that is not equal to the input time slot on the X channel

or

- channel Y is in the compress mode
- channel X is either idled or set into bypass with an input time slot that is not equal to the input time slot on the Y channel

restriction in U - Law:

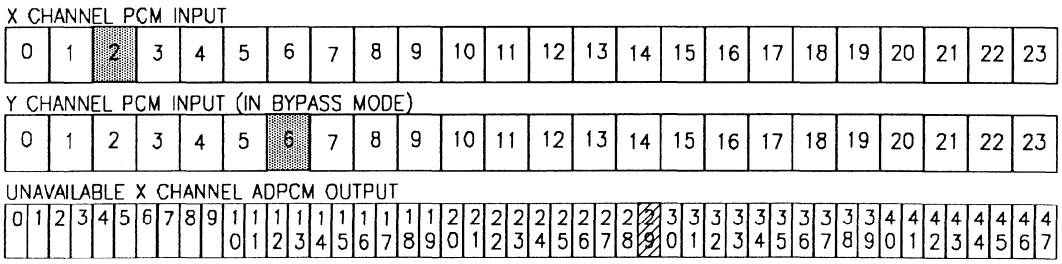
- the output ADPCM time slots cannot be 24 ADPCM time slots following the input PCM time slot.

restriction in A - Law:

- the output ADPCM time slots cannot be 32 ADPCM time slots following the input PCM time slot.

example:

- CLKX = CLKY = 1.544MHz
- channel X is programmed to U - Law
- input PCM time slot for channel X is 2
- channel Y is set to bypass with an input time slot of 6
- restricted APDCM time slot output is 29



CASE 5

conditions:

- channel X is in the expand mode
- channel Y is either idled or set into bypass with an input time slot that is not equal to the input timeslot on the X channel

or

- channel Y is in the expand mode
- channel X is either idled or set into bypass with an input time slot that is not equal to the input time slot on the Y channel

restriction in U - Law:

- the output PCM time slots cannot be 12 PCM time slots following the input ADPCM time slot.

restriction in A - Law: - the output PCM time slots cannot be 16 PCM timeslots following the input ADPCM time slot.

example:
- CLKX = CLKY = 1.544MHz
- channel X is programmed to U - Law
- input ADPCM time slot for channel X is 15
- channel Y is set to bypass with an input timeslot of 20
- restricted output PCM time slot is 19

X CHANNEL ADPCM INPUT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47

Y CHANNEL ADPCM INPUT (IN BYPASS MODE)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47

UNAVAILABLE X CHANNEL PCM OUTPUT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

CASE 6

conditions:
- channel X is in the expand or compress mode
- channel Y is set into bypass with an input time slot that is equal to the input time slot on the X channel

or

- channel Y is in the expand or compress mode
- channel X is set into bypass with an input time slot that is not equal to the input time slot on the Y channel

restriction in U - Law: - the output time slot of the bypassed channel must not follow the input time slot by less than 12 PCM (24 ADPCM) timeslots

restriction in A - Law: - the output time slot of the bypassed channel must not follow the input time slot by less than 16 PCM (32 ADPCM) timeslots

example:
- CLKX = CLKY = 1.544MHz
- channel X is programmed to U - Law
- input PCM time slot for channel X is 2
- channel Y is set to bypass with an input timeslot of 2
- restricted Y channel output time slots are 2 through 14

X CHANNEL PCM INPUT

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

Y CHANNEL PCM INPUT (IN BYPASS MODE)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

UNAVAILABLE Y CHANNEL PCM OUTPUT (IN BYPASS MODE)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

DALLAS SEMICONDUCTOR

DS2180A-BASED SLC-96 SYSTEM APPLICATION NOTE

DS2180A-BASED SLC-96 SYSTEM

SLC-96 is a T1-based, digital subscriber loop system developed by AT&T which utilizes a modified D4 framing format on 1 (or more) of 4 T1 lines in a 96 subscriber configuration. The system periodically "steals" the Fs framing bit present in the D4 framing pattern and replaces it with a low speed data link. A SLC-96 data link frame is 9ms in length and is made up of six D4 multiframes. Please refer to the DS2180A data sheet for details about the D4 (193S) framing pattern.

The 36 Fs framing bits in the SLC-96 data link frame include a "normal" 12-bit Fs reframe pattern (000111000111) and a 24-bit data link pattern which is arranged as follows:

- bits 1 through 11 are the Concentration Field (C-Field)
- bits 12 through 14 are a fixed Spoiler Pattern (010)
- bits 15 through 17 are the Maintenance Field (M-Field)
- bits 18 through 19 are the Alarm Data Link Field (A-Field)
- bits 20 through 23 are the Protection Line Switch Field (S-Field)
- bit 24 is a 1-bit Spoiler Pattern (1)

The spoiler bits are used to align the data link timing with the multiframe timing established by the reframe pattern. Please see BellCore document TR-TSY-000008 for more details.

Transmit Data Link

External logic must be combined with the DS2180A to support the SLC-96 data link in the transmit path. (See Figure 1.) D4 framing (CCR.4=0) and external Fs bit insertion (TCR.2=1) must be selected on the DS2180A. The reframe pattern as well as the SLC-96 data link pattern is multiplexed into the DS2180A via the TLINK input. Output signals from the DS2180A such as TLCLK and TMO can be used to simplify this task.

Multiframe Synchronization

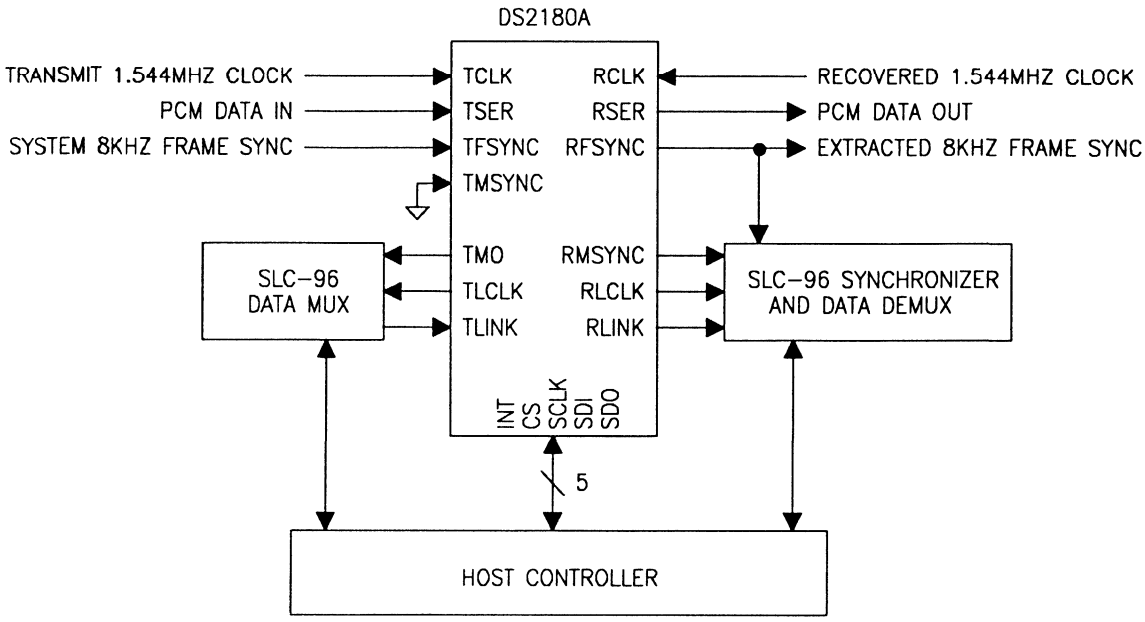
The receive synchronizer of the DS2180A must be programmed to the Ft/Fs cross-coupling mode (RCR.3=1) and to the minimum sync time (RCR.2=0) in order for the DS2180A to properly frame at the multiframe level to a framing pattern that contains SLC-96. The transceiver will frame up to the reframe pattern that is present in the SLC-96 stream. The DS2180A will frame to the SLC-96 stream in at most 10ms.

NOTE: The user may find it necessary to have the DS2180A programmed to expect yellow alarms in the Fs bit (CCR.3=1) in order for the DS2180A to frame to SLC-96. If this is the case, once the DS2180A has achieved multiframe synchronization, the D4 yellow alarm select bit (CCR.3) can be used normally. Of course the CCR.3 bit will have to be set to a one for subsequent resynchronizations.

SLC-96 Data Link Synchronization

Synchronization to the SLC-96 data link must be performed externally. (See Figure 1.) Output signals from the DS2180A such as RLINK, RLCLK, RFSYNC, and RMSYNC can be used to synchronize to the SLC-96 stream and demultiplex its data fields.

SLC-96 SYSTEM BLOCK DIAGRAM Figure 1



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NOTE: This simplified block diagram does not show all DS2180A I/O; it indicates only one of several control options available to the SLC-96 system designer.

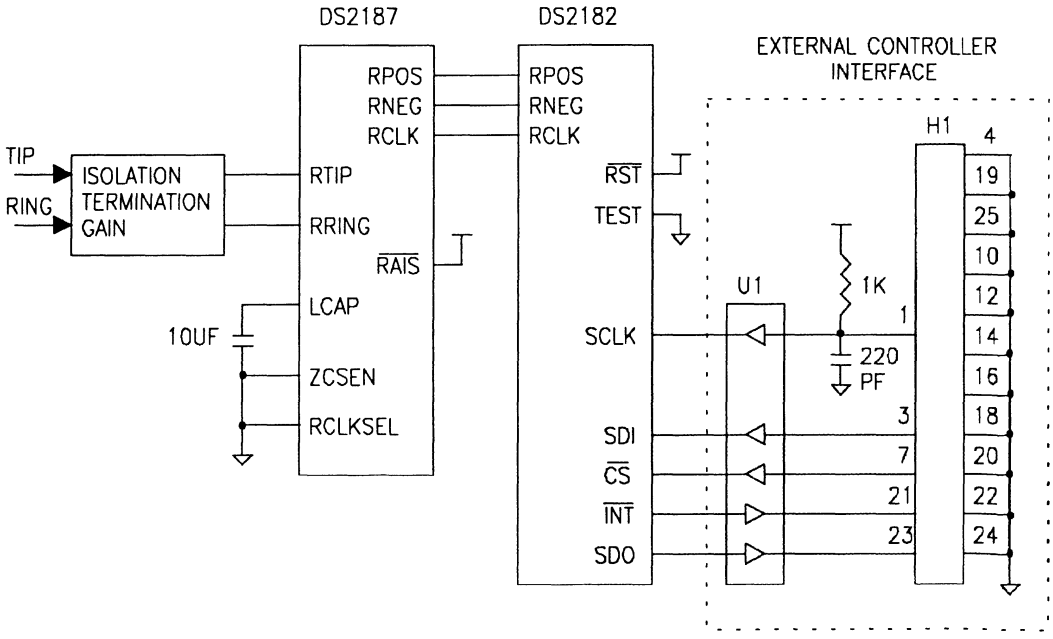
DALLAS
SEMICONDUCTOR

DS2182/DS2187
T1 LINE MONITORING APPLICATION NOTE

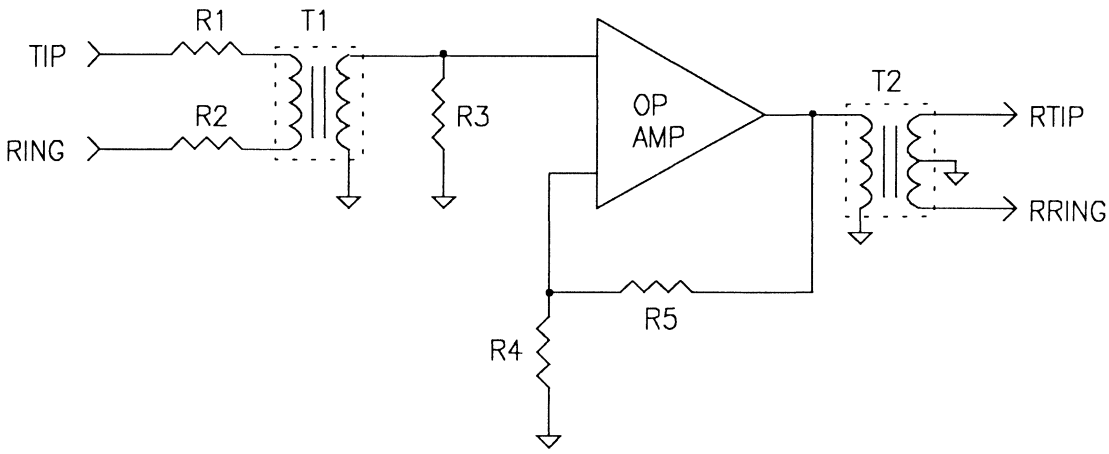
MONITORING A T1 LINE USING THE DS2182 AND DS2187

The DS2182 and DS2187 can be used in tandem to unobtrusively monitor the status of a T1 line in real time. The DS2187 will recover clock and data from the line and provide it to the DS2182 which will frame to the signal and extract performance information from it. The performance information gathered by the DS2182 can then be collected by an external controller. The circuit in Figure 1 details such an arrangement. Unobtrusive monitoring requires that the impedance presented to the T1 line be much greater than the nominal termination of 100 ohms. Termination impedances between 1K ohm and 10K ohm are typical. High termination impedances will reduce the level of the bipolar T1 signal seen by the DS2187. Since the DS2187 has an input sensitivity of about 700mV peak, the incoming T1 signal may have to be amplified. The amplification can be done using an op amp with a moderate amount of bandwidth. A simple arrangement is shown in Figure 2. Transformer 1 in Figure 2 is needed in order to provide the necessary isolation from the T1 line. Resistors R1, R2, and R3 determine the effective input impedance of the monitor circuit. The amount of amplification that the op amp needs to provide is determined by three factors: (1) the termination impedance, (2) the winding ratios of both transformers T1 and T2, and (3) the signal requirements of 700mV peak needed by the DS2187. As long as the monitor is to be placed within 1000 feet of the source, no Automatic Line Build Out (ALBO) needs to be performed on the incoming T1 signal before it is presented to the DS2187.

T1 LINE MONITOR USING DS2182 AND DS2187 Figure 1



SIMPLE PREAMPLIFY STAGE FOR THE DS2187 Figure 2



In order to set the DS2182 to the proper configuration and collect data from it, an external controller is required. The external controller communicates to the T1 monitor through a simple serial port on the DS2182. The controller can take many forms, such as an IBM PC or some type of microcontoller like the DS5000 Soft Microcontroller. An example of how to interface an 8051/31 to the DS2182 can be found in the DS2180A-Supervisory Software Application Note. This application note covers both hardware and software issues. Since the DS2182 has large onboard counters, a single controller can collect data on many T1 lines. The counters on the DS2182 are large enough that the controller needs only to retrieve data every half second or so. Exact half second reads not only provide for a convenient manner in which to calculate Errored Seconds and Severely Errored Seconds, but they ensure that none of the four counters on the DS2182 will have a chance to overflow. Precise time intervals can be obtained from the signals provided by the DS2182. For example, in the ESF framing, RMSYNC will transition high every 3ms.

Under normal circumstances where no interrupts need to be serviced, only five registers need to be read. It takes 48 SCLK periods to read all the five registers (BVCR1, BVCR2, CRCCR, OOFCR, and FECR) in the burst mode. With a SCLK of 1MHz, this translates to a read time of only 48us.

The Auto Counter Reset feature (RCR1.4 = 1) in the DS2182 serves two functions. First, it eliminates some overhead processing time that would be necessary in the controller to clear the count registers once they are read. Second and more importantly, it ensures that error counts in the count registers will not be accidently cleared. This situation might occur if the ACR feature is disabled (RCR1.4 = 0) and errors appear on the T1 line between the time the count registers are read and subsequently cleared.

Figure 3 shows how a single controller can handle a number of DS2182s. The connections between the DS2182s and the controller are simplified by the shared serial port bus structure.

MULTIPLE DS2182 CONNECTION SCHEME Figure 3

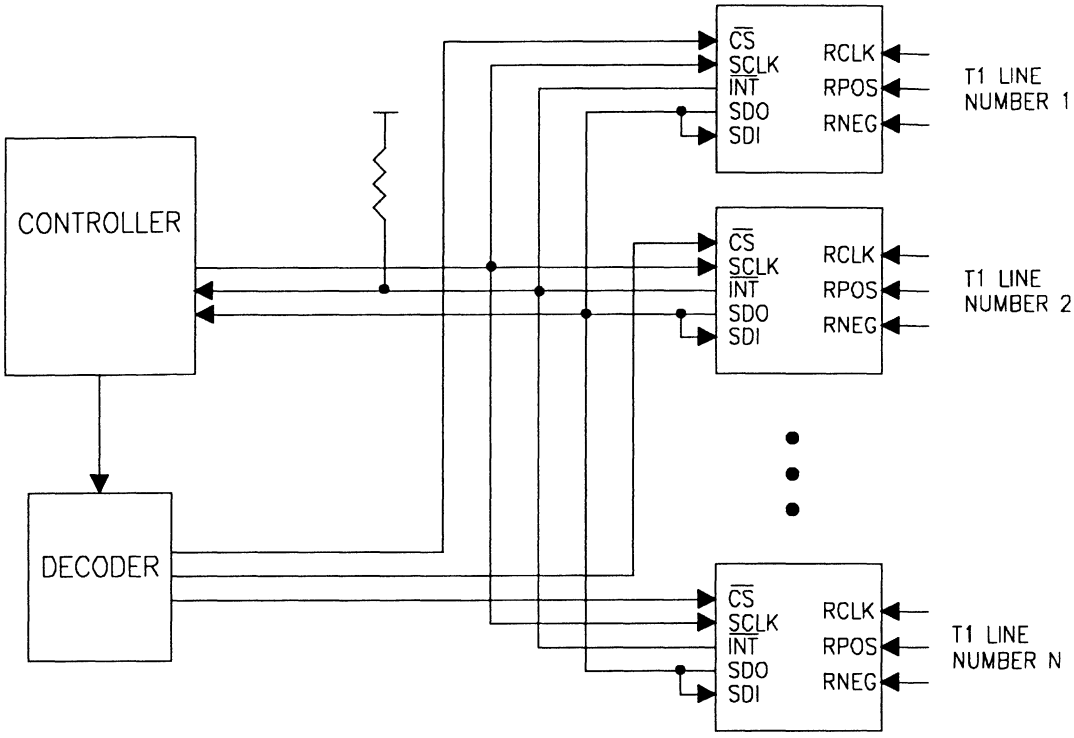


Table 1 is a quick reference for the DS2182. It details the various alarms and errors that the DS2182 can supply and where they can be found.

DS2182 QUICK REFERENCE Table 1

Yellow Alarm	RSR1.4 and Pin 7
Blue Alarm	RSR1.1
Frame Bit Errors	RSR2.4, Frame Error Count Register, and Pin 26
CRC Error Events	CRC Count Register and Pin 26
OOF Events	OOF Count Register
Bipolar Violations	BPV Count Registers and Pin 25
B8ZS Code Word Detect	RSR1.2
Loss of Sync	RSR1.3 and Pin 27
Change of Frame Alignment	RSR1.0
Receive Carrier Loss	RSR1.5 and Pin 24
Eight Zero Detect	RSR1.7
Sixteen Zero Detect	RSR1.6

NOTE:
RSR is the Receive Status Register.

APPENDIX A: EXTERNAL CONTROLLER EXAMPLE

The controller interface shown in Figure 1 is designed to directly connect the DS2182 to the parallel printer port of an IBM PC or compatible computer. The PC will set up the DS2182 into the proper configuration via the serial port and it will retrieve data collected by the DS2182 on command. For more information on how to go about writing such a program, please contact the factory.

The following components are recommended for the computer interface shown in Figure 1:

H1	26-pin right-angle header receptacle (example: 3M No. 3429)
U1	74HCT244 octal buffer

The DS2182 can be connected to the computer's parallel printer port by a cable with a 26-pin header connector on one end and a DB-25 male connector on the other. The connections are:

Controller Interface	26-pin Header	DB-25 Connector	Parallel Port on the PC
SCLK	1	1	strobe/
-	2	14	auto feed/
SDI	3	2	D0
GND	4	15	error/
-	5	3	D1
-	6	16	init/
CS/	7	4	D2
-	8	17	select in/
-	9	5	D3
GND	10	18	ground
-	11	6	D4
GND	12	19	ground
-	13	7	D5
GND	14	20	ground
-	15	8	ground
GND	16	21	ground
-	17	9	D7
GND	18	22	ground
GND	19	10	ack/
GND	20	23	ground
INT/	21	11	busy
GND	22	24	ground
SDO	23	12	paper end
GND	24	25	ground
GND	25	13	select
-	26	-	-

DALLAS SEMICONDUCTOR

DS2181
CEPT TRANSCEIVER APPLICATION NOTE

NOTES ON THE DS2181 CEPT TRANSCEIVER

This Application Note covers five topics concerning the DS2181 CEPT Transceiver. The first section provides a detailed explanation of exactly how the DS2181 syncs to an incoming data stream. This section also defines the transceiver's resync criteria and how a resync is performed. The second section explains how the DS2181 can be set up to sync to a data stream when it is not known beforehand, whether CAS and/or CRC4 multiframes are present in the data stream. The third section shows how a user can determine what frame or multiframe level caused a loss of synchronization. The fourth section demonstrates how the RFER pin on the DS2181 can be decoded. Finally, the fifth section is a short tutorial on CEPT frame and multiframe structures.

SECTION 1: HOW THE DS2181 SYNCS AND RESYNCS

In a CEPT environment, the data stream will always contain the Frame Alignment Signal (FAS) and it may contain either one or both of the two kinds of multiframe, namely Cyclic Redundancy Check 4 (CRC4) and Channel Associated Signaling (CAS). The following discussion will cover exactly how the DS2181 handles synchronization and resynchronization under FAS, CRC4, and CAS levels. Please refer to Figure 1 as a supplement to the discussion.

FAS Sync

The DS2181 always begins a sync or resync with a search for the FAS. The DS2181 considers that it has found the FAS when it has located a correct FAS word (X0011011), followed by a non-FAS with bit 2 set to a one (X1XXXXXX), followed by another correct FAS word. If a proper FAS sequence exists in the incoming data stream, then the DS2181 will sync to it in at most four frames or 500us. If a resync is occurring (i.e., the part has previously obtained FAS sync), the DS2181 begins a bit-by-bit search for the FAS word in the timeslot following the one it had previously been aligned to. This reduces the chance of the framer resyncing onto the same emulator. If both CAS and CRC4 are disabled, and once the FAS sync criteria are met, then the DS2181 will enter a sync condition and the RLOS pin will go low. If either CAS or CRC4 is enabled, then the DS2181 will perform a search for their respective multiframe alignment signals before a sync condition is asserted. If both CAS and CRC4 are enabled, then the searches are performed in parallel after the FAS sync criteria have been met.

CAS Multiframe Sync

If CAS is enabled (RCR.5 = 0), then the DS2181 uses the frame alignment created by the FAS sync to locate timeslot 16. The framer then begins searching timeslot 16 for the multiframe alignment word (0000XXXX). If the DS2181 finds the frame alignment word and the previous timeslot 16 did not contain the multiframe alignment word, then CAS multiframe sync is declared. The user has the option of making the CAS sync criteria more rigid by setting RCR.4 to a one. If RCR.4 is set, then the DS2181 will look for two additional multiframe alignment words before it declares sync. If the DS2181 cannot find CAS multiframe alignment in 12 to 14ms (i.e., over 6 full multiframes), then it will set the MFSERR bit (RCR.2) to a one and initiate a resync at the FAS level.

CRC4 Multiframe Sync

If CRC4 is enabled (CCR.2 = 1), then the DS2181 will search for the CRC4 multiframe alignment word (001011XX) in bit 1 of time slot zero of the non-align frames. If two valid multiframe alignment words are found in 12 to 14ms, then sync is declared. Otherwise, the DS2181 will initiate a resync at the FAS level.

FAS Resync Criteria

Once sync is declared (RLOS is low and RSR.1 = 0), then the DS2181 automatically monitors the FAS words for errors. If the FAS word is received in error three consecutive times, then the FSERR bit (RSR.3) is set to a one and a resync will be intiated if RCR.1 is cleared. The user can make the resync criteria softer by setting RCR.2 to a one. If RCR.2 is set, then the DS2181 will monitor bit 2 in timeslot zero of the non-align frames as well as the FAS words for

errors. If either bit 2 or the FAS word (or both) is incorrect on three consecutive occasions, then a resync is initiated.

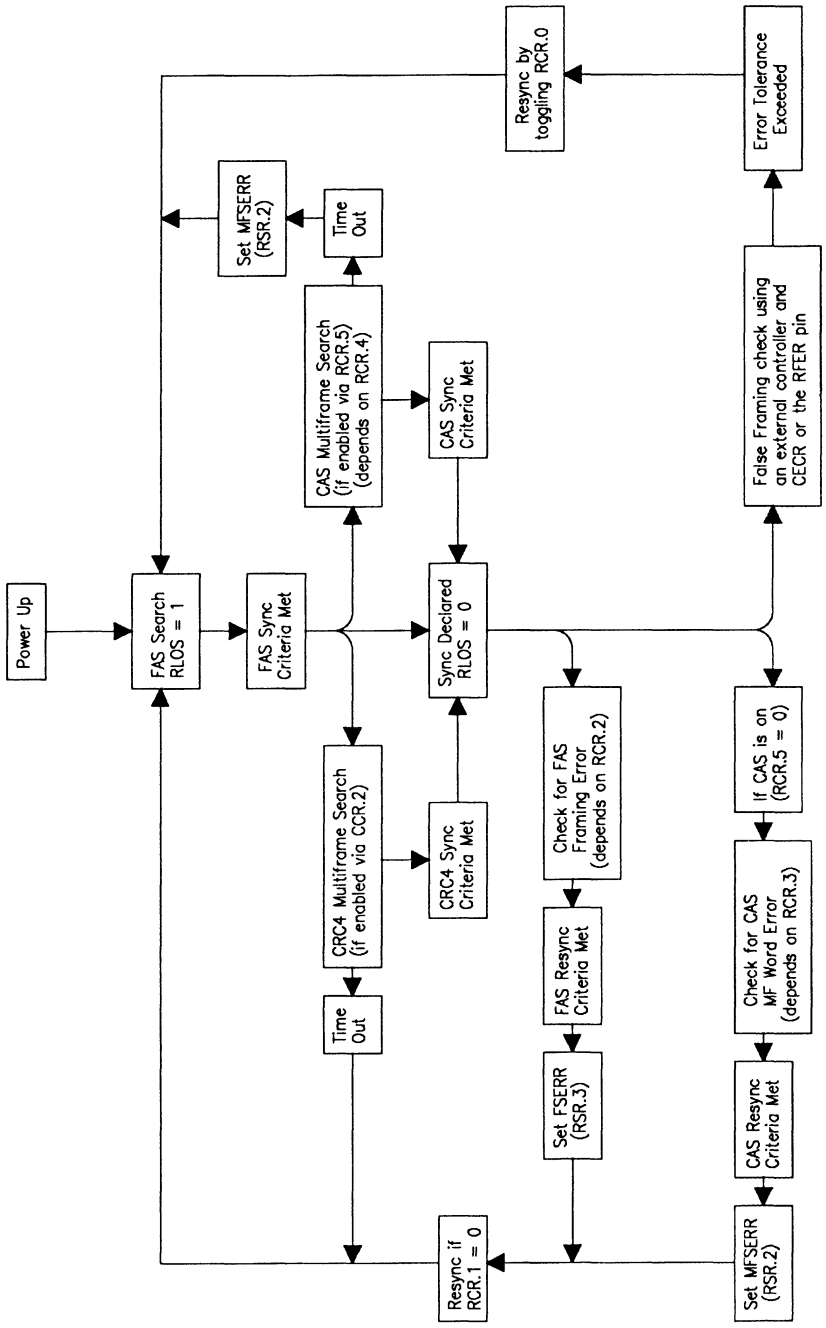
CAS Resync Criteria

If CAS is enabled (RCR.5 = 0), then the DS2181 will monitor timeslot 16 for errors in the multiframe alignment word. If two consecutive multiframe alignment words are received in error, then the MFSERR bit (RSR.2) is set to a one and, if RCR.1 is cleared, then a resync at the FAS level will be initiated. The CAS resync criteria can be softened by setting RCR.3 to a one. If RCR.3 is set, then the DS2181 will resync if it gets two incorrect multiframe alignment words in a row or if it ever receives two consecutive timeslot 16 words with zeros in the first four MSB bit positions (0000XXXX).

CRC4 Resync Criteria

Once the DS2181 has achieved sync, if CRC4 is enabled, then it will begin recording CRC4 code word errors in the CRC4 Count Error Register (CECR) and at the RFER pin. CCITT recommends that if more than 914 CRC4 errors are received out of a block of 1000 code words, it is to be assumed that the framer has falsely locked onto an emulator. The user can monitor CRC4 code word errors in the CECR or at the RFER pin and initiate a resync in the DS2181 by toggling RCR.0 from a zero to a one or by doing a hardware reset.

DS2181 SYNC/RESYNC FLOWCHART Figure 1



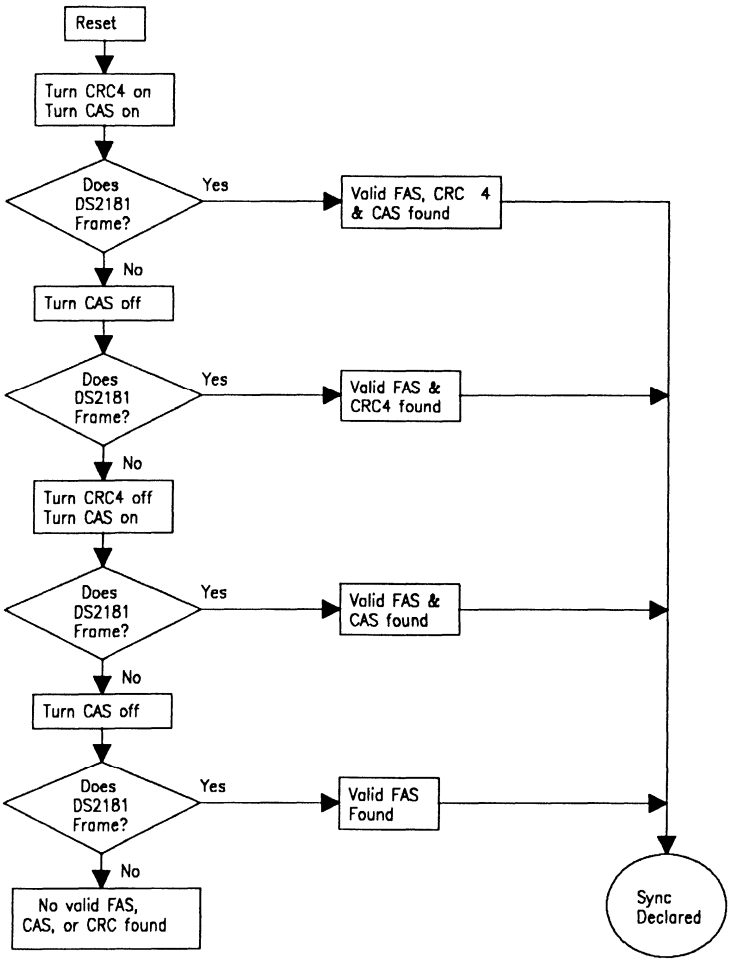
SECTION 2: USE OF DS2181 TO DETERMINE CEPT FRAME/MULTIFRAME CONDITIONS

The DS2181 CEPT Transceiver can be used to determine whether or not the incoming data stream contains any of the following:

1. Channel Associated Signaling (CAS) multiframe structure
2. Cyclical Redundancy Check 4 (CRC4) multiframe structure
3. Frame Alignment Signal (FAS) frame structure

In order to establish which of the three are present, the user must selectively enable and disable the various multiframe modes of the DS2181. One possible method of performing this function is shown in the flowchart in Figure 2. The flowchart suggests that the user initally enable both CAS and CRC4 multiframes and try to achieve sync. If sync cannot be obtained, first CAS is disabled, and then CRC4 is disabled. If sync still cannot be obtained, then the FAS structure must not be present. Users can implement the flowchart outlined in Figure 2 with the DS2181 in either the hardware or software mode.

FLOWCHART TO DETERMINE FRAME/MULTIFRAME Figure 2



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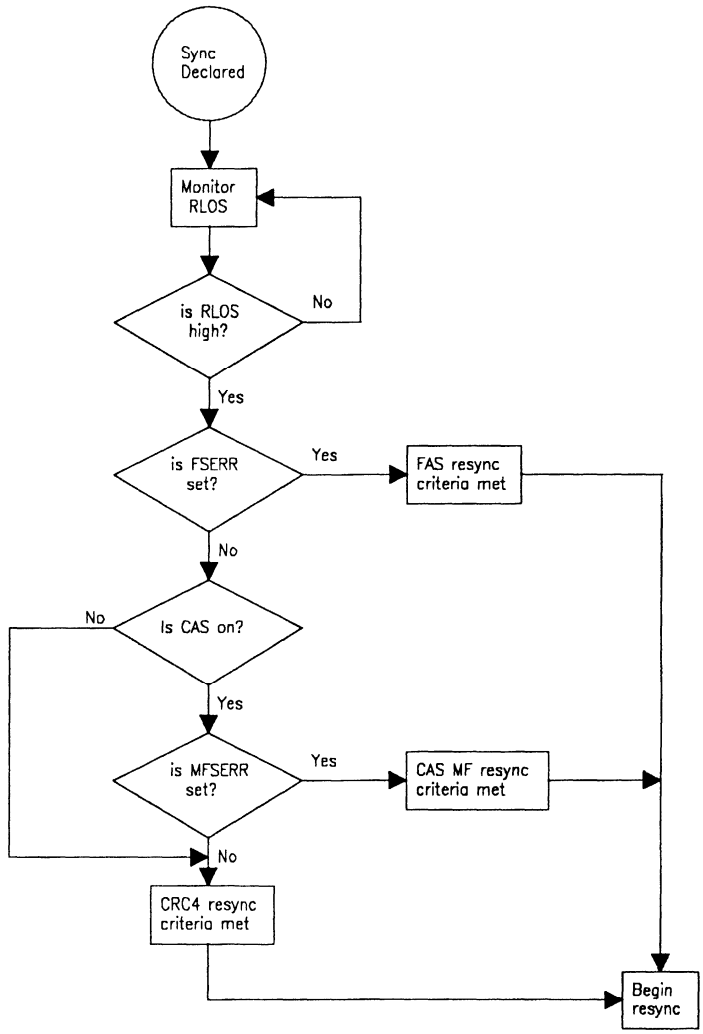
SECTION 3: HOW TO DETERMINE WHAT CAUSED RESYNC

If the DS2181 is used in the software mode, then the Receive Status Register (RSR) can be monitored to determine what event triggered a loss of synchronization. One possible method of performing this task is shown in the form of a flowchart in Figure 3. The flowchart suggests that the user monitor the RLOS bit (RSR.1) or pin to ascertain when a loss of synchronization occurs. Once a loss of synchronization has occurred, then the FSERR bit (RSR.3) and the MFSERR bit (RSR.2), along with the known configuration of the transceiver, can be used to establish the event that evoked the loss of synchronization.

DS2181 FLOWCHART FOR CAUSE OF LOSS OF SYNC Figure 3



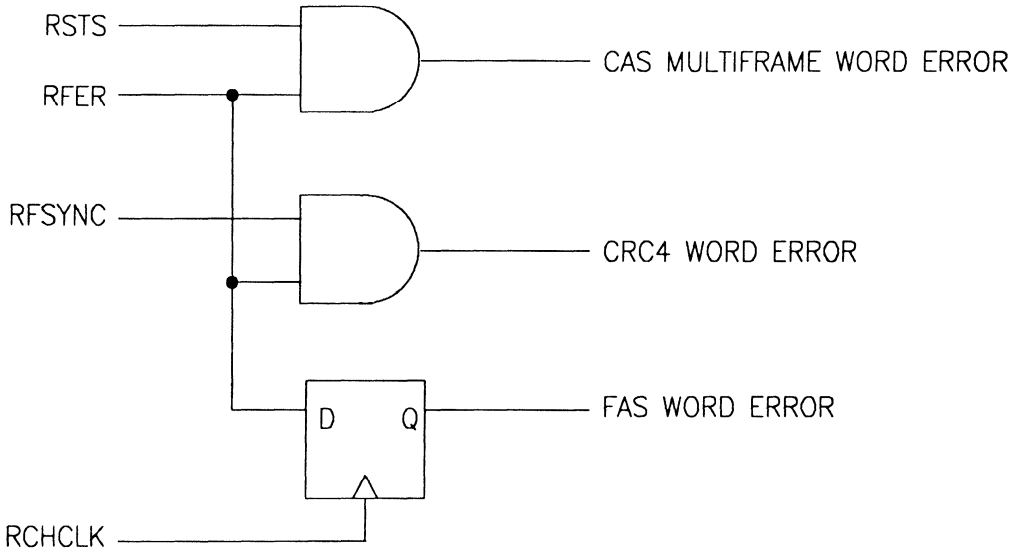
SECTION 4: HOW TO DECODE THE RFER PIN ON THE DS2181

Three types of errors in the received data stream are reported in real time at the RFER pin. They are:

1. Errors in the Frame Alignment Signal (FAS) word
2. Errors in the Channel Associated Signaling (CAS) multiframe alignment word
3. Errors in the Cyclical Redundancy Check 4 (CRC4) code word

The user can determine the type of error reported at the RFER pin by externally decoding the pin with two AND gates and a D-type flip-flop as shown in Figure 4. A rising edge out of either the AND gates or the D flip-flop indicates that a particular error event has occurred.

EXTERNALLY DECODING THE RFER PIN Figure 4



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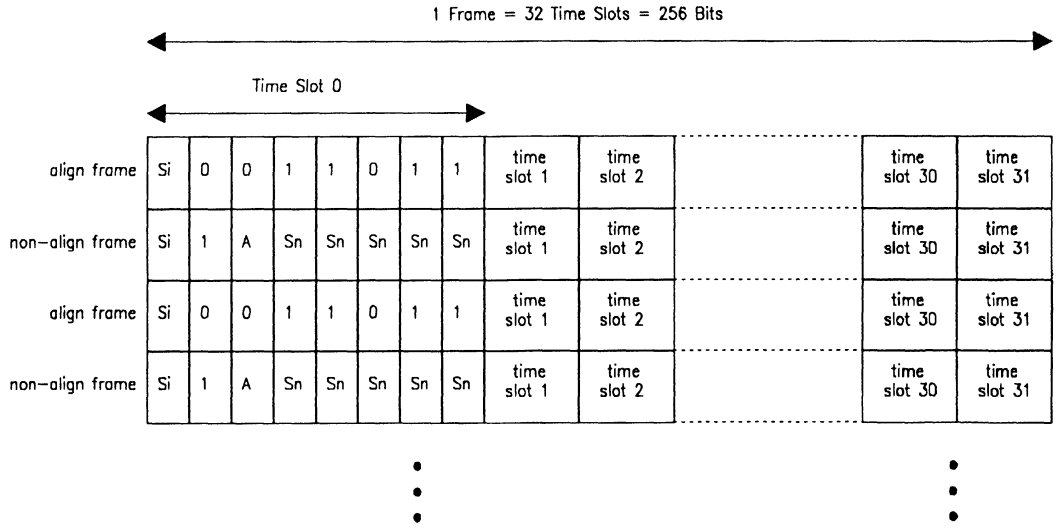
SECTION 5: CEPT FRAME AND MULTIFRAME STRUCTURES

CEPT Frame Structure

The 2.048MHz CEPT (PCM - 30) environment consists of a frame structure of 256 bits that is repeated at an 8KHz rate. Each frame consists of 32 eight-bit timeslots that are numbered from 0 to 31. The first eight-bits of every frame (timeslot 0) are used mainly to provide framing information. Every other timeslot 0 contains a fixed seven-bit pattern known as the Frame Alignment Signal (FAS). See Figure 5. As its name suggests, the FAS pattern (X0011011) identifies timeslot 0, from which the other timeslots can be readily ascertained. In frames that do not begin with the FAS (non-align frames), bit 2 of the timeslot is fixed at a one to ensure that it does not emulate the FAS pattern. Besides framing information, time slot 0 contains two sets of spare bits and an alarm. One spare bit per frame is intended for international use and it is designated Si in Figure 5. Five spare bits per frame are available for national usage and they are designated Sn in Figure 5. Bit 3 of the non-align frames is used to indicate whether the remote unit is in alarm or not. If the Alarm bit is set to a one, then an alarm condition exists at the remote. If it is zero, then no alarm condition exists.

CEPT FRAME STRUCTURE Figure 5



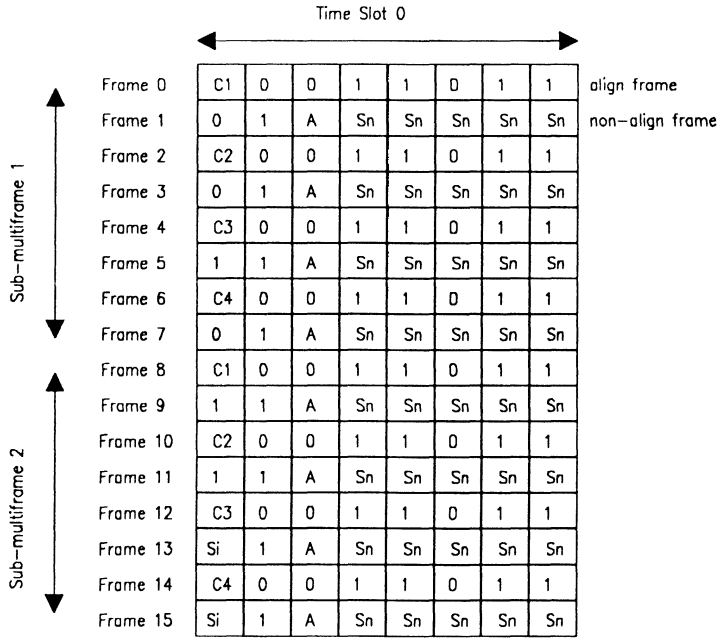
CEPT Multiframe Structure

Two separate multiframe structures exist in CEPT environments: Cyclical Redundancy Check 4 (CRC4) and Channel Associated Signaling (CAS). Both of these multiframes are based on the FAS framing level but they are used independently of each other for different purposes. Although both multiframes consist of a set of 16 consecutive frames, they need not be aligned nor must they both be present in a data stream.

CRC4 Multiframe Structure

The multiframe structure of CRC4 is shown in Figure 6. The CRC4 multiframe consists of a multiframe alignment word and two 4-bit code words. The CRC4 multiframe always begins on an align frame and it utilizes the spare international bit (bit 1 of both align and non-align frames) location. The CRC4 multiframe alignment word is a repeating 6-bit code (001011) which is located in odd frames 1 through 11. Each CRC4 multiframe is divided into two sub-multiframes (SMF). Each SMF consists of eight frames and it contains one 4-bit CRC4 code word. Each code word represents a data check on eight frames of data (8 frames X 256 bits/ frame = 2048 bits). Each eight frame set is called a block. Hence each SMF is equivalent to one block. The two 4-bit code words are located in the even frames. The CRC4 multiframe is used primarily to assist in validating alignment at the FAS level but it could also be used to monitor error performance. CCITT recommends that whenever more than 914 CRC4 blocks out of 1000 are received in error, then it should be assumed that a false alignment at the FAS level has occurred.

CRC4 MULTIFRAME STRUCTURE Figure 6



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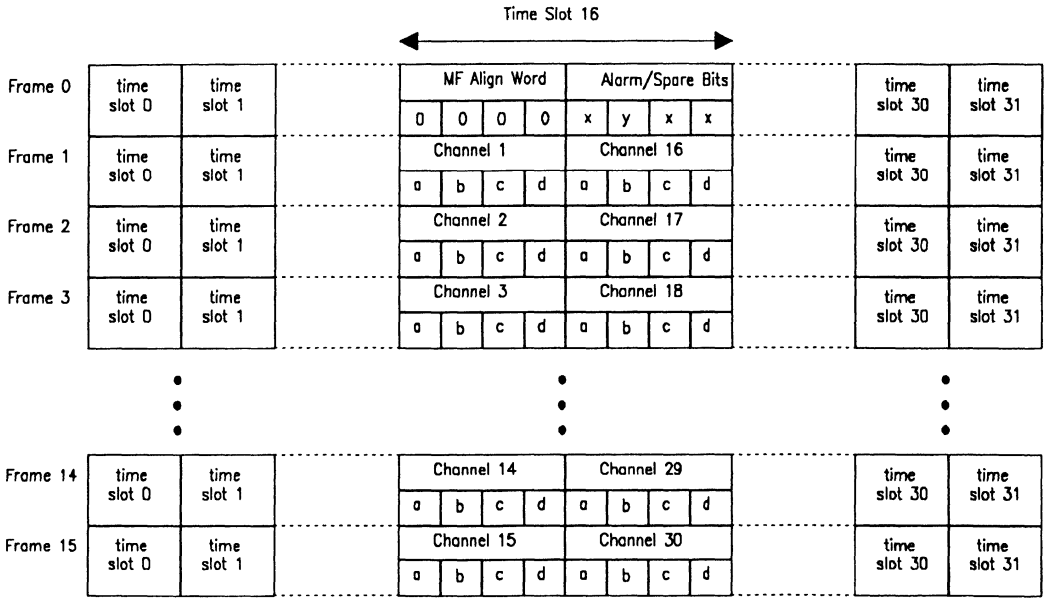
CEPT CAS Multiframe Structure

The CAS multiframe structure is shown in Figure 7. It is made up of 16 frames and it can begin on either an align or a non-align frame. The CAS multiframe always resides in timeslot 16. The first frame contains a multiframe alignment word (0000) in the upper nibble and a set of spare and alarm bits (xyxx) in the lower nibble. The spare bits are denoted as "x" in Figure 7 and they should be set to a one if they are not being used. The alarm bit is denoted as a "y" in Figure 7 and it will be set to a one if CAS multiframe alignment is lost. The other 15 frames contain 30 channels of signaling data as demonstrated in Figure 7. If the b,c, and d bits are not used, then they should be set to 1, 0, and 1, respectively.

CAS MULTIFRAME STRUCTURE Figure 7



More information on CEPT frame and multiframe structures can be found in the CCITT Recommendations G.704, G.706, and G.732.

DALLAS
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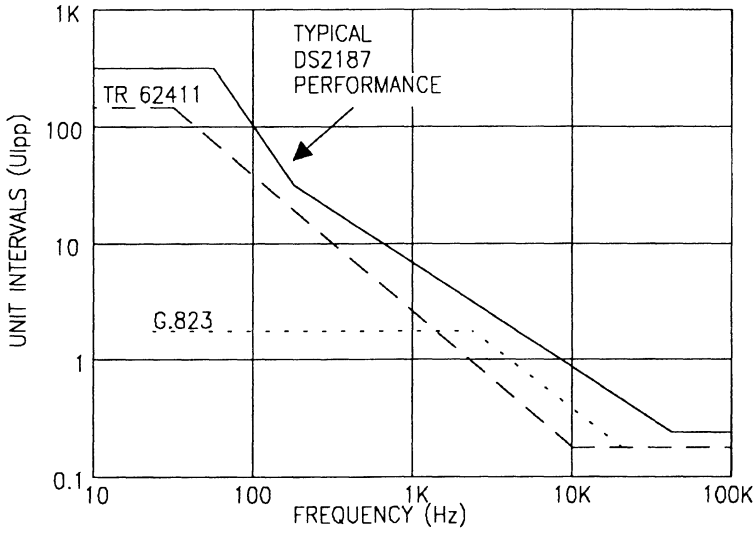
DS2186/DS2187
LINE INTERFACING APPLICATION NOTE

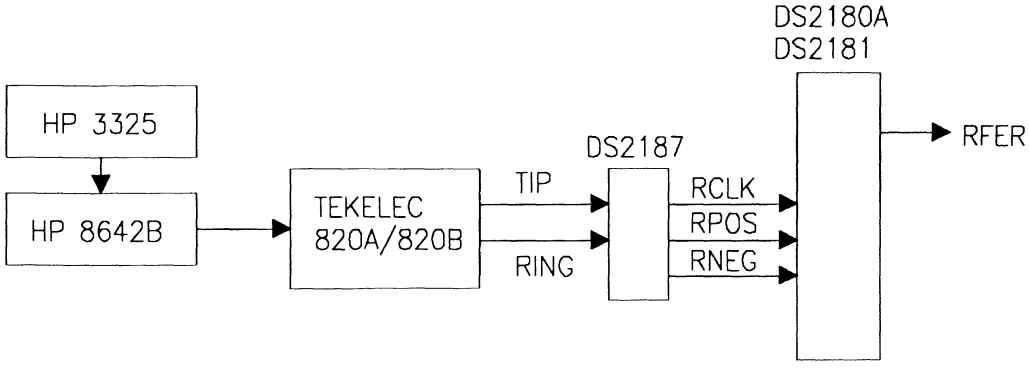
Jitter Tolerance of the DS2187

Figure 1 displays the input jitter tolerance of the DS2187 Receive Line Interface. The DS2187 has approximately the same jitter tolerance whether it is operated in the T1 or CEPT mode. The jitter measurements shown in Figure 1 were made using the setup shown in Figure 2. For the T1 measurements, the clock source was a precise 1.544MHz and the data pattern was the standard QRSS (2^{20}-1 pattern with 15 zero suppression). For the CEPT measurements, the clock source was a precise 2.048MHz and the data pattern was as described in CCITT Recommendation O.171 (2^{15}-1 pattern). In both measurements, no zero code suppression techniques were used. The DS2187 was considered able to handle a particular level of input jitter if it was able to receive data without errors for 30 seconds.

JITTER TOLERANCE OF DS2187 Figure 1



DS2187 JITTER MEASUREMENT SETUP Figure 2

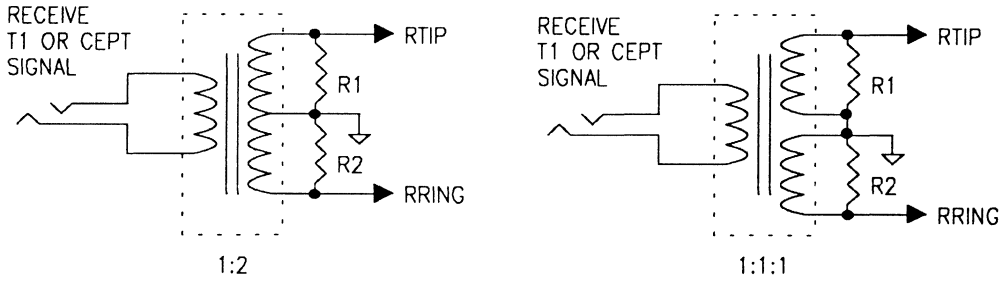


Transformer Selection for DS2187
The DS2187 is very insensitive to the transformer used to couple it to the line. Table 1 lists some recommended transformer specifications. Figure 3 shows how to connect a 1:1:1 transformer and a 1:2 transformer to the DS2187. R1 and R2 should be equal in value and twice the magnitude of the nominal line impedance. For example, for a 100 ohm T1 line, R1 and R2 should be 200 ohms.

DS2187 TRANSFORMER SPECIFICATIONS Table 1

Turns Ratio	1:2 or 1:1:1
Inductance	60uhy to 1.2mhy
Leakage Inductance	1.3uhy max
Interwinding Capacitance	30pf max
DC Resistance	2.0 ohms max

DS2187 TRANSFORMER CONNECTION Figure 3



DS2186

Transformer Selection for DS2186
The DS2186 is more sensitive to the particular transformer chosen to couple to the line than the DS2187, but there is a wide selection of transformers available. Table 2 lists a set of recommended transformer specifications and Table 3 lists some specific models that have been characterized with the DS2186 at the factory.

DS2186 TRANSFORMER SPECIFICATIONS Table 2

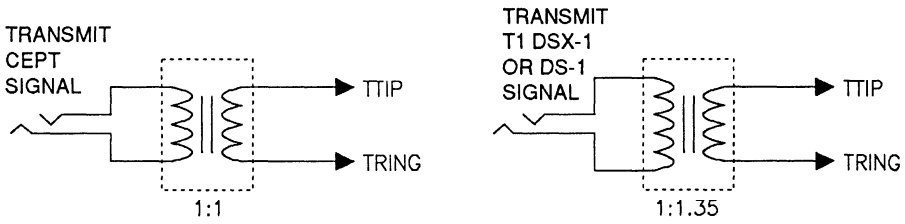
Turns Ratio	1:1 or 1:1.35
Inductance	60uhy to 1.2mhy
Leakage Inductance	1.3uhy max
Interwinding Capacitance	30pf max
DC Resistance	2.0 ohms max

SUGGESTED DS2186 TRANSFORMERS Table 3

VENDOR	1 : 1 Model	1 : 1.35 Model
Pulse Engineering	PE-64931 PE-64951	PE-62251
Schott	67109300 67112060	67121090
AIE Magnetics	318-0720 318-0696	318-0809
AT&T	2662K	2662C
Magcomp	MC-5300	MC-5306

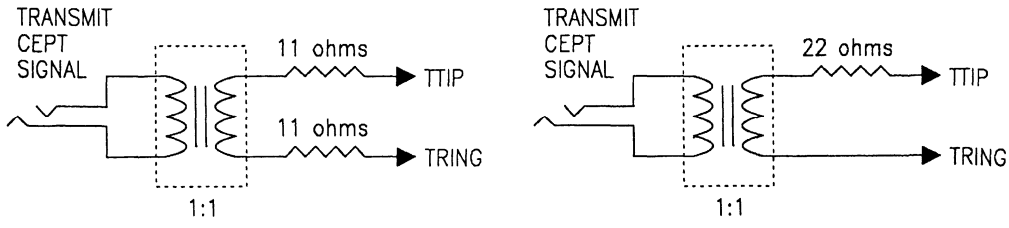
The specifications and transformers listed in Tables 2 and 3 are meant to be used as guidelines; they are not requisite. The 1:1 Transformer winding ratios are meant for CEPT applications, and the 1:1.35 ratios are meant for T1 applications. Figure 4 shows how to connect a transformer to the DS2186.

DS2186 TRANSFORMER CONNECTION Figure 4



In CEPT applications with a 75 ohm interface, a resistor is needed in each leg of the transformer in order to meet the output level requirement of 2.37Vpeak. (See Figure 5.) No external resistors are needed with the 120 ohm interface. The 1:1 connection as shown in Figure 4 is acceptable.

CEPT 75 OHM INTERFACE FOR DS2186 Figure 5



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